Using the UCC2897A-EVM

User's Guide

Literature Number: SLUU357
November 2009

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48-V to 3.3-V Forward Converter with Active Clamp Reset Using the UCC2897A Active Clamp Current Mode PWM Controller

1 Introduction

The UCC2897A evaluation module (EVM) is an active clamp reset forward converter providing a 3.3-V regulated output at 30 A of load current, operating from a 48-V input. The design operates over the full 36-V to 72-V telecom input range, and is able to fully regulate down to zero load current. The module uses the UCC2897A Current Mode Active Clamp PWM Controller for effectively demonstrating the active clamp transformer reset technique.

Benefits of the active clamp include a control driven transformer reset scheme allowing zero voltage switching (ZVS) to increase overall efficiency, lower drain-to-source voltage stress, extended duty cycle beyond 50% and reduced electromagnetic radiated emissions. Combined with synchronous rectification, the design operates at 250 kHz and exhibits a peak efficiency of 93%, with a full load efficiency of over 91%. The design displays many features that might be typical of a more complex design, yet its compact board layout and low component count make it elegantly simple

2 Description

The UCC2897A controller provides advanced active clamp control features such as programmable maximum duty cycle clamp, programmable dead time between the two primary switches and the ability to drive a P-channel MOSFET in a low-side active clamp configuration. The UCC2897A also allows the ability to start-up directly from the 48-V telecom bus voltage, eliminating the need for external start-up circuitry. It includes programmable soft start, internal slope compensation for peak current mode control, internal low-line and high-line voltage sensing, internal bi-directional synchronizable clock input, cycle-by-cycle current limiting and short circuit current protection, and a robust 2-A sink/source TrueDrive™ internal gate drive circuit. The result is a highly efficient design loaded with features, requiring very few external components.

The TrueDrive™ output architecture of UCC2897A uses TI’s unique TrueDrive™ Bipolar/CMOS hybrid output. To the user, this simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region.

The UCC2897A is available in a 20-pin TSSOP package for applications where absolute minimal board space is required.

The UUCC2897A-EVM highlights the many benefits of using the UCC2897A Active Clamp Current Mode PWM Controller. The following user guide provides the schematic, component list, assembly drawing, artwork and test set up necessary to evaluate the UCC2897A in a typical telecom application.

The user should note that overcurrent protection is not incorporated in this design.

2.1 Typical Applications

Isolated telecom 48-V input systems requiring high efficiency and high power density for very low output voltage, high current converter applications, including:

- Server Systems
- Datacom
- Telecom
- DSP’s, ASIC’s, FPGA’s

2.2 Features

- ZVS transformer reset using active clamp technique in forward converter.
- All surface mount components, double sided half brick (2.2” x 2.28” x 0.5”).
- Low-side active clamp with programmable dead time for ZVS.
- Current-Mode Control with bi-directional sync function.
- Internal PWM slope compensation.
- Start up directly from telecom input voltage.
- Synchronous rectifier output stage allows high efficiency operation.
- Programmable soft start.
- Up to 30 A_{DC} output current.
- Regulation to zero load current.
- Non-latching, cycle-by-cycle over-current and short circuit protection.
- Non-latching, Input under-voltage protection.
- Non-latching, Input over-voltage protection.
- 1500-V isolation primary to secondary.

3 Electrical Performance Specifications

Table 1. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Input voltage range		36	48	72	V
No load input current	V_{IN} = 36 V, I_{OUT} = 0 A		75	100	mA
Input undervoltage limit			35		V
Input overvoltage limit			73		
Max input current	V_{IN} = 36 V, I_{OUT} = 30 A		3	3.25	A
Input voltage ripple	V_{IN} = 72 V, I_{OUT} = 30 A		1.5	1.75	Vpp
Output Characteristics					
Output voltage	36 V < V_{IN} < 72 V, 0 A < I_{OUT} < 30 A	3.25	3.3	3.35	V
Output voltage regulation	Line reg (36 V < V_{IN} < 72 V, I_{OUT} = 0 A)		0.00%	0.01%	-
	Load reg (0 A < I_{OUT} < 30 A, V_{IN} = 48 V)		0.06%	0.10%	
Output voltage ripple	V_{IN} = 48 V, I_{OUT} = 30 A		30	35	mVpp
Output load current	36 V < V_{IN} < 72 V	0		30	A
Output current limit		32			
Short circuit protection	Not provided				
Systems Characteristics					
Switching frequency		225	250	265	kHz
Control loop bandwidth	36 V < V_{IN} < 72 V, I_{OUT} = 10 A	5		7	
Phase margin		50		60	°
Peak efficiency	V_{IN} = 36 V		93%		-
Full load efficiency	V_{IN} = 48 V, I_{OUT} = 30 A		91%		

4 Schematic

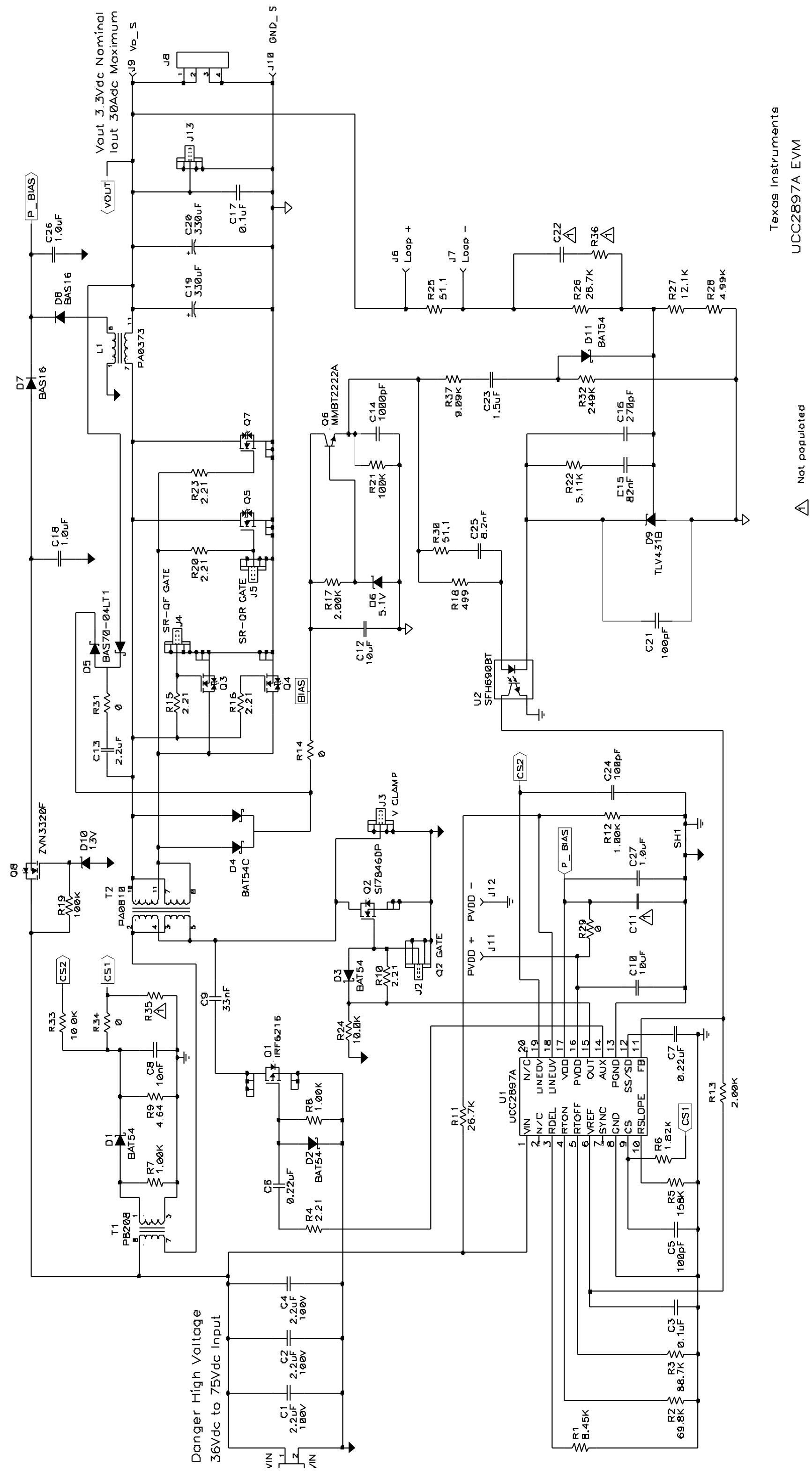

Figure 1. UCC2897A-EVM Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source, VIN: The input voltage shall be a variable DC source capable of supplying between 0 V_{DC} and 75 V_{DC} at no less than 3.5 A_{DC}, and connected to J1 and A1 as shown in Figure 2. For fault protection to the unit, good common practice is to limit the source current to no more than 3.5 A_{DC} for a 36-V input. A DC ammeter, A1 should also be inserted between VIN and J1 as shown in Figure 2. For highest accuracy, such as gathering efficiency data, V_{IN} should be measured directly across the input capacitor.

External PVDD DC Power Supply (Optional): The design allows for separate VDD and PVDD, allowing the gate drive voltage amplitude to be separately biased from the rest of the device. By removing R29, the gate drive voltage for Q1 and Q2 can be derived from an external DC power supply applied to J11 and J12. Be cautious not to exceed the maximum gate-to-source voltage rating ($V_{GS(max)}$ = 20 V) of Q1 and Q2. Do not connect an external DC power supply to J11 and J12 when R29 is installed

Output Load, LOAD1: For the output load to V_{OUT}, a programmable electronic load set to constant current mode and capable of sinking 0 A_{DC} to 30 A_{DC}, shall be used. For convenience, V_{OUT} can be monitored by connecting a DC voltmeter, V2, to J9 and J10. For highest accuracy, such as gathering efficiency data, V_{OUT} should be measured directly across the output capacitor at J13.

Network Analyzer (Optional): A network analyzer can be connected directly to J6 and J7. The UCC2897 reference design provides a 51.1-Ω resistor (R25) between the output and the voltage feedback to allow easy non-invasive measurement of the control to output loop response

Fan: Most power converters include components that can be hot to the touch when approaching temperatures of 60°C. Because this design is not enclosed to allow probing of circuit nodes, a small fan capable of 200 LFM to 400 LFM is recommended to reduce component temperatures when operating at or above 50% maximum rated load current

Recommended Wire Gauge: The connection between the source voltage, V_{IN} and J1 can carry as much as 3.25 A_{DC}. The minimum recommended wire size is AWG #20 with the total length of wire less than 8 feet (4 feet input, 4 feet return). The connection between J8 and LOAD1 can carry as much as 30 A_{DC}. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4 feet output, 4 feet return).

5.2 Recommended Test Setup

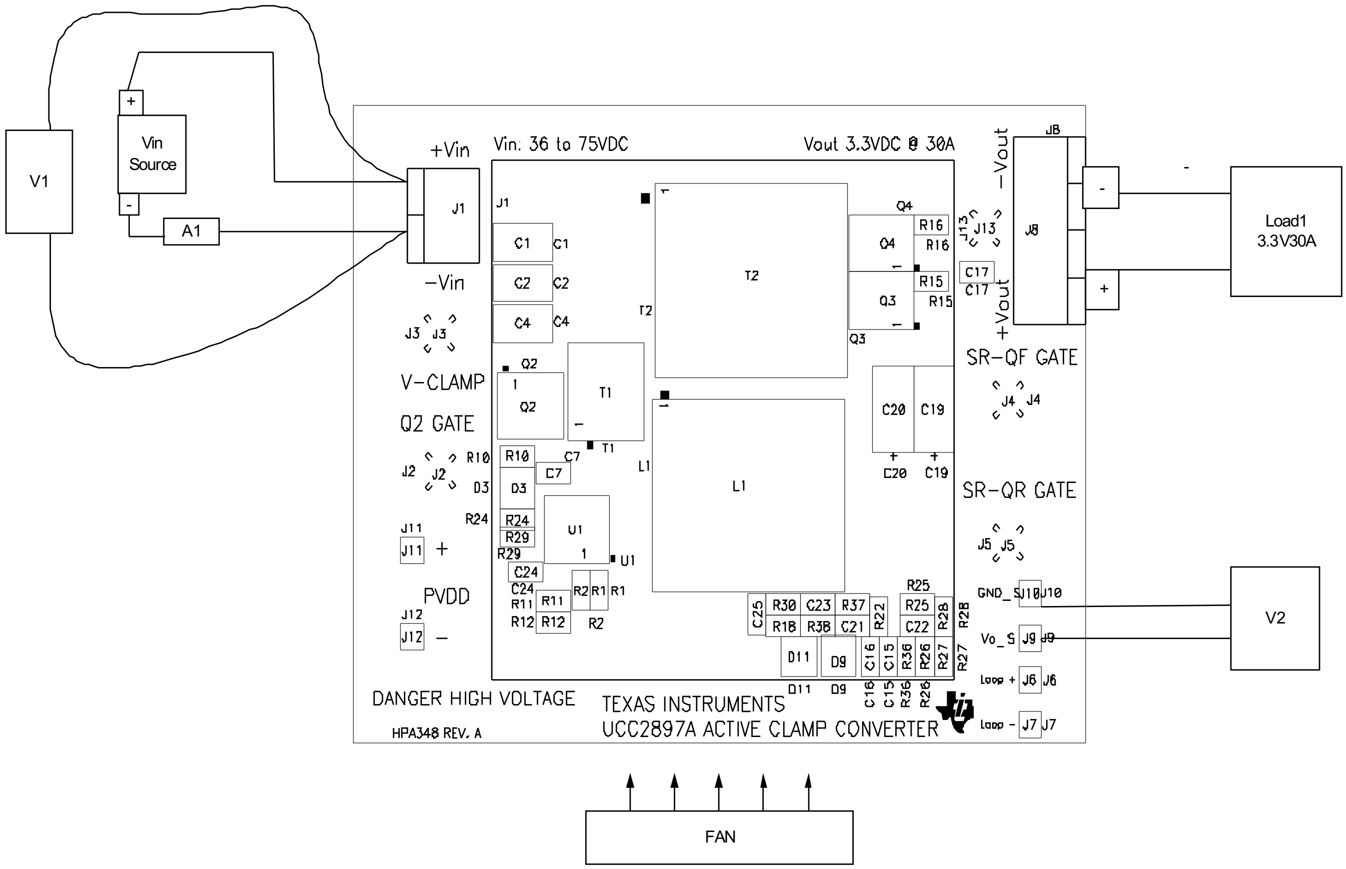

Figure 2. Recommended Test Set Up

6 Power Up/Down Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the unit. electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 3.5 A maximum. Make sure V_{IN} is initially set to 0 V and connected to J1 as shown in Figure 2.
3. Connect the ammeter A1 (0 A to 10 A range) between V_{IN} and J1 as shown in Figure 2.
4. Connect voltmeter (can optionally use voltmeter from V_{IN} source if available), V1 across V_{IN} as shown in Figure 2.
5. Connect LOAD1 to J8 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{IN} is applied.
6. Connect voltmeter, V2 across J9 and J10 as shown in Figure 2.
7. Increase V_{IN} from 0 V to 36 V_{DC}.
8. Observe that V_{OUT} is regulating when V_{IN} is at 36 V.
9. Increase V_{IN} to 48 V.
10. Increase LOAD1 from 0 A to 15 A_{DC}.
11. Turn on fan making sure to blow air directly on the unit.
12. Increase LOAD1 from 15 A_{DC} to 30 A_{DC}.
13. Decrease LOAD1 to 0 A.
14. Decrease V_{IN} from 48 V_{DC} to 0 V.
15. Shut down V_{IN}

7 Performance Data and Typical Characteristic Curves

through present typical performance curves for UCC2897A-EVM.

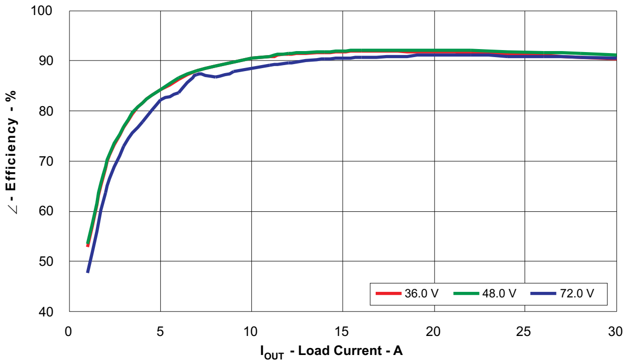

Figure 3. UCC2897A-EVM Efficiency

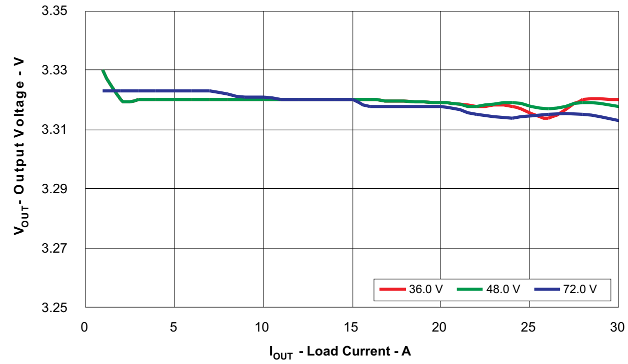

Figure 4. Line and Load Regulation

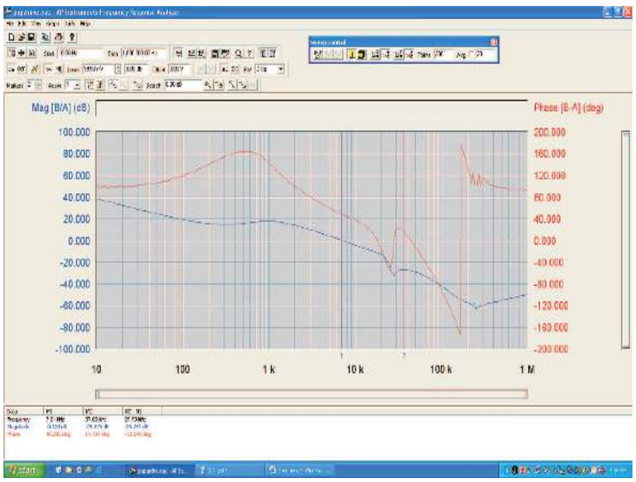

Figure 5. Loop Response Gain and Phase 36 V in 0-A Load

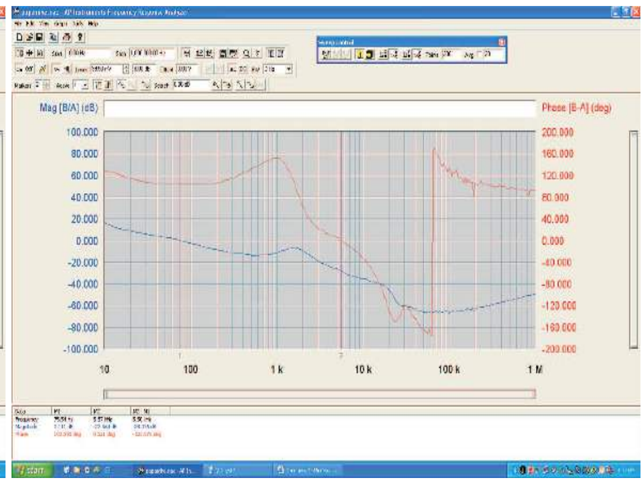

Figure 6. Loop Response Gain and Phase 36 V in 30 A Load

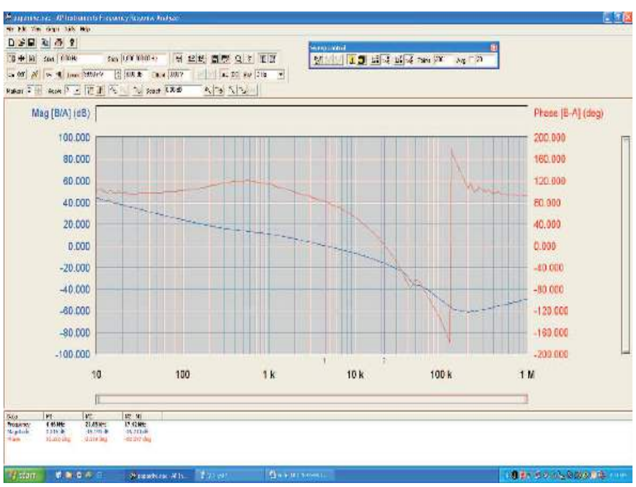

Figure 7. Loop Response Gain and Phase 72 V in 30-A Load

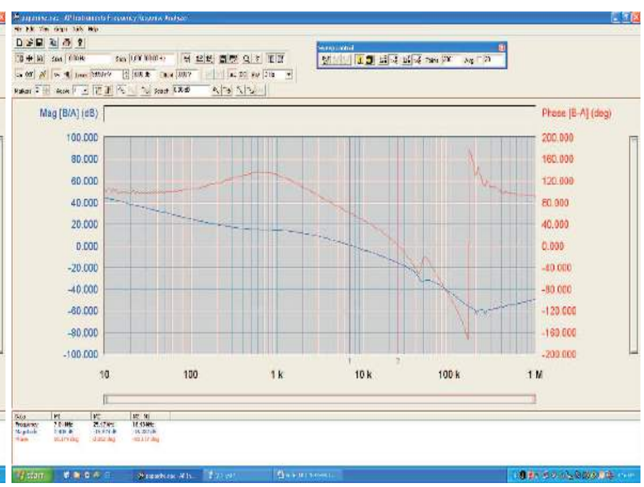

Figure 8. Loop Response Gain and Phase 72 V in 0-A Load

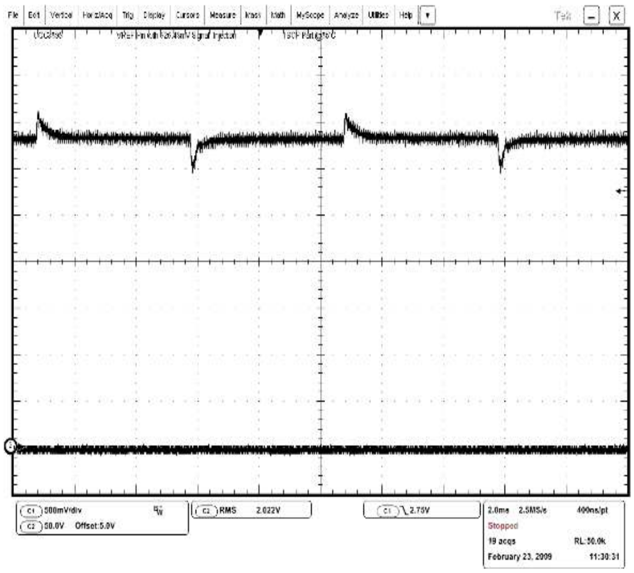

Figure 9. 10-A Load with 5-A Transient

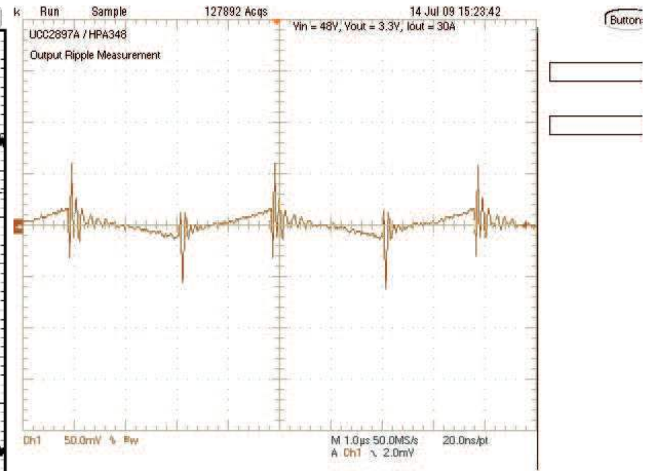

Figure 10. Output Ripple, (24mVpp, noise 151.2mVpp)

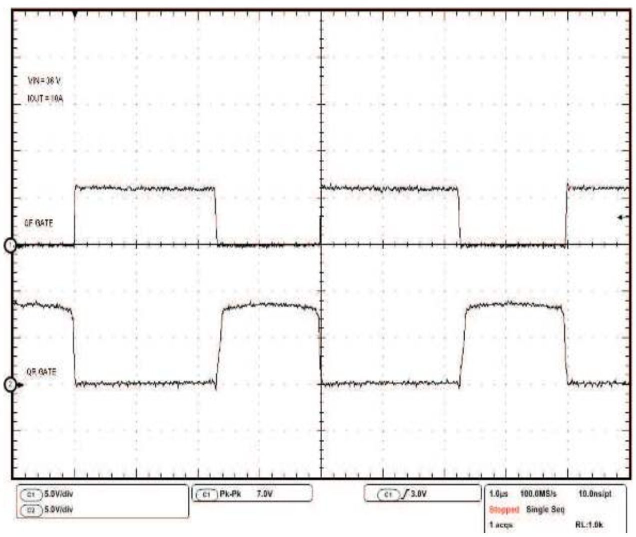

Figure 11. Synchronous Rectifier Gate Drive (V_{IN} = 36 V)

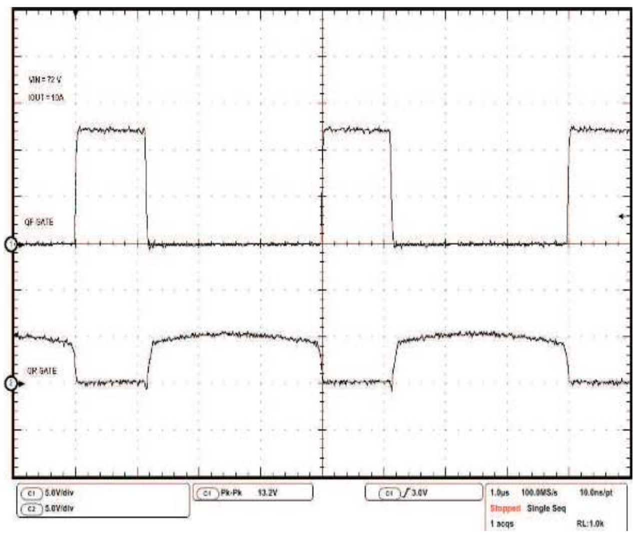

Figure 12. Synchronous Rectifier Gate Drive (V_{IN} = 72 V)

Figure 13. Turn-On Waveform 30 V in a 30-A Load

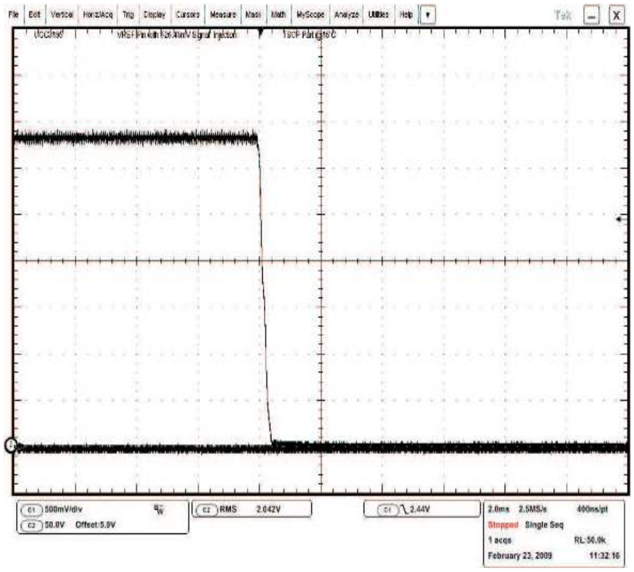

Figure 14. Power Off Waveform

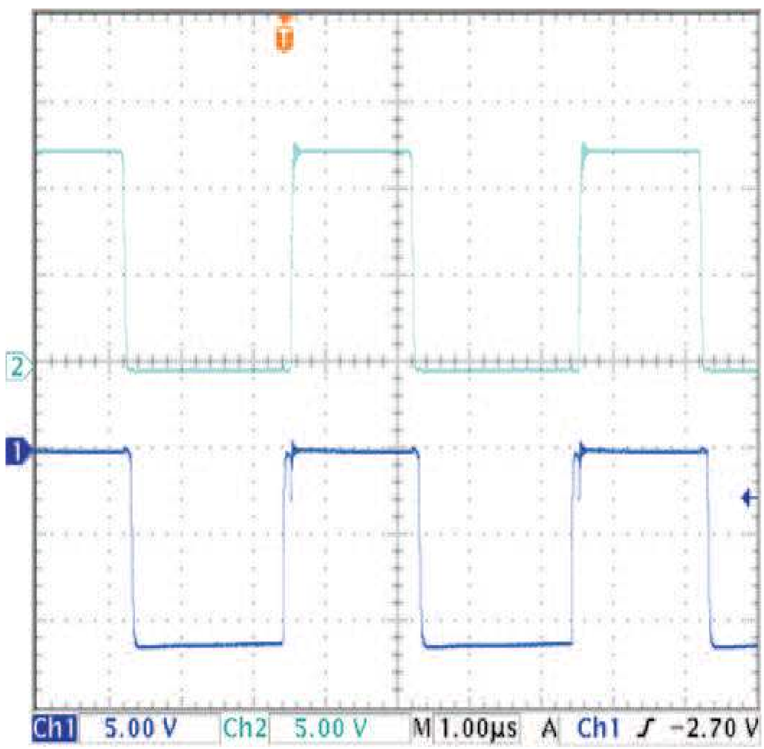

Figure 15. Q1 and Q2 Gate to Source Voltage VIN = 48 V, I_{OUT} = 10 A

8 EVM Assembly Drawing and PCB Layout

Figures Figure 16 through Figure 21 show the design of the UCC2897A-EVM printed circuit board. The PCB is a four-layer board using 4-oz copper on all layers.

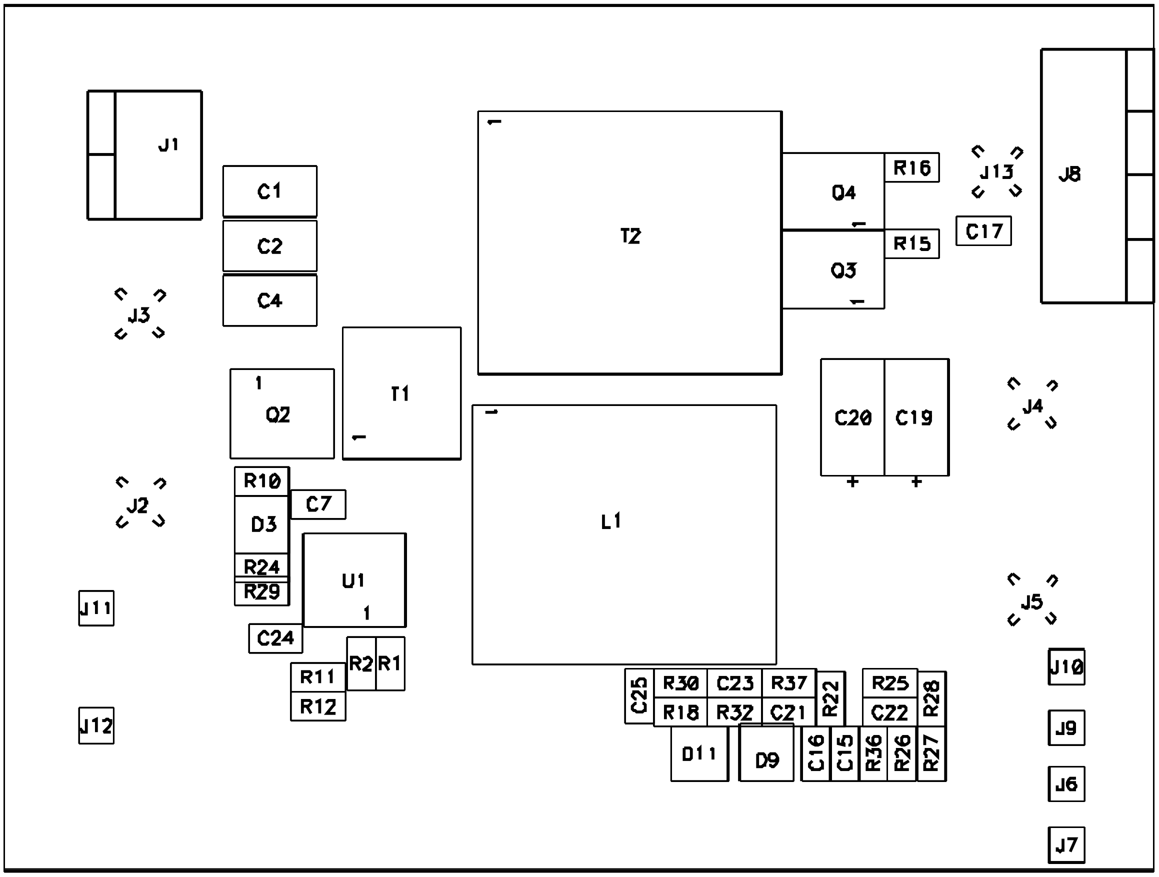

Figure 16. Top Layer Assembly Drawing (top view)

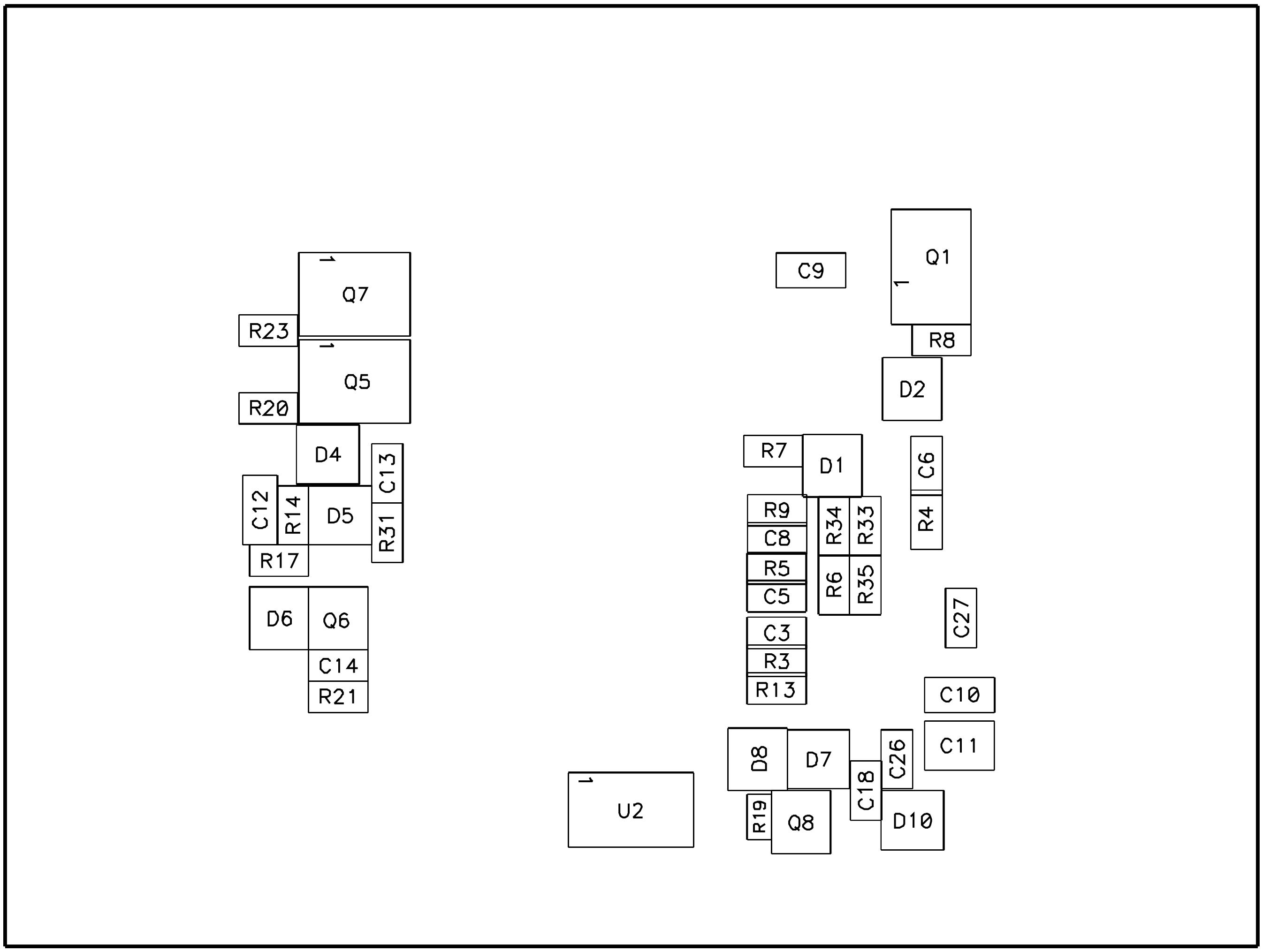

Figure 17. Bottom Assembly Drawing (bottom view)

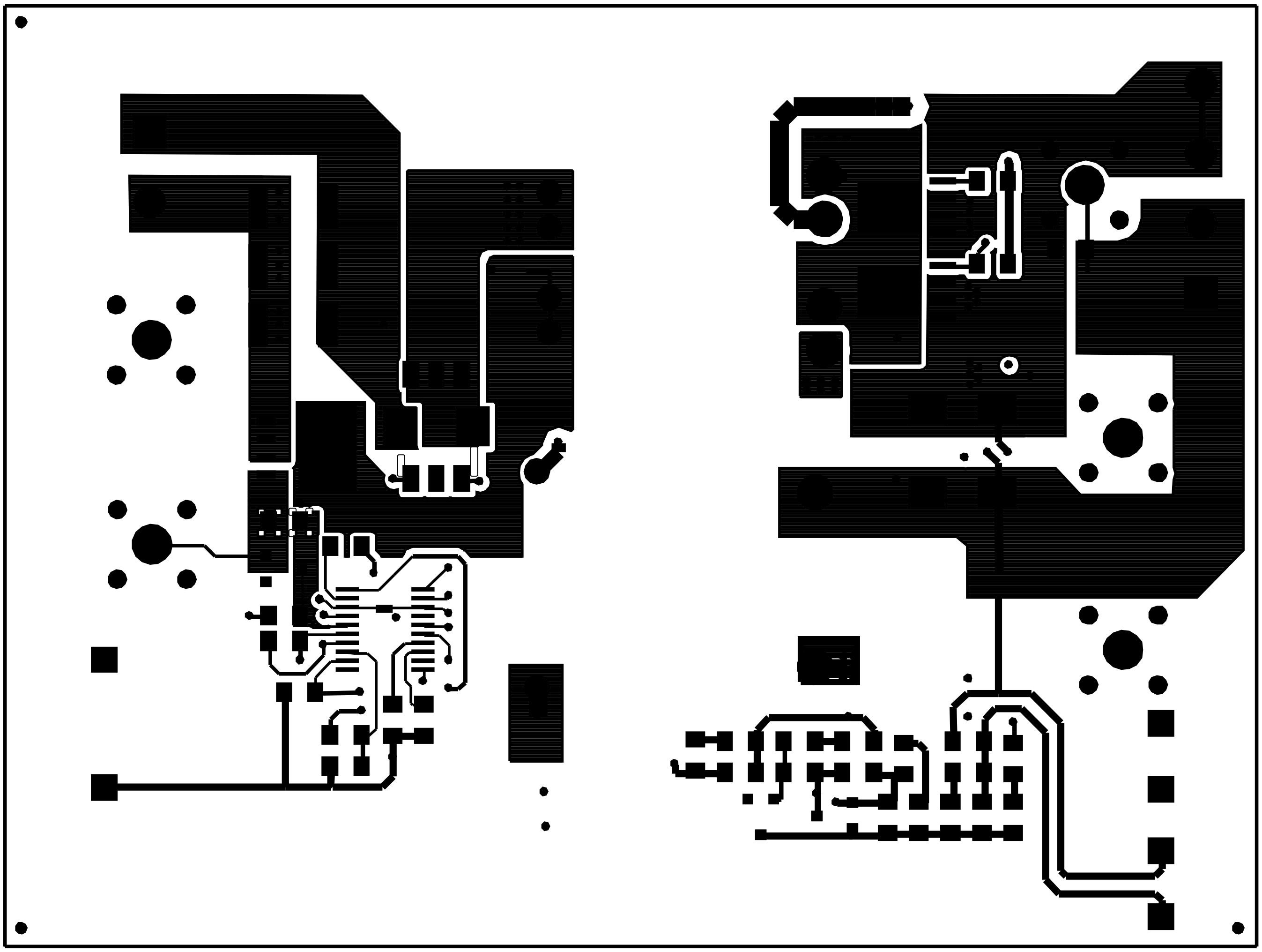

Figure 18. Top Copper (top view)

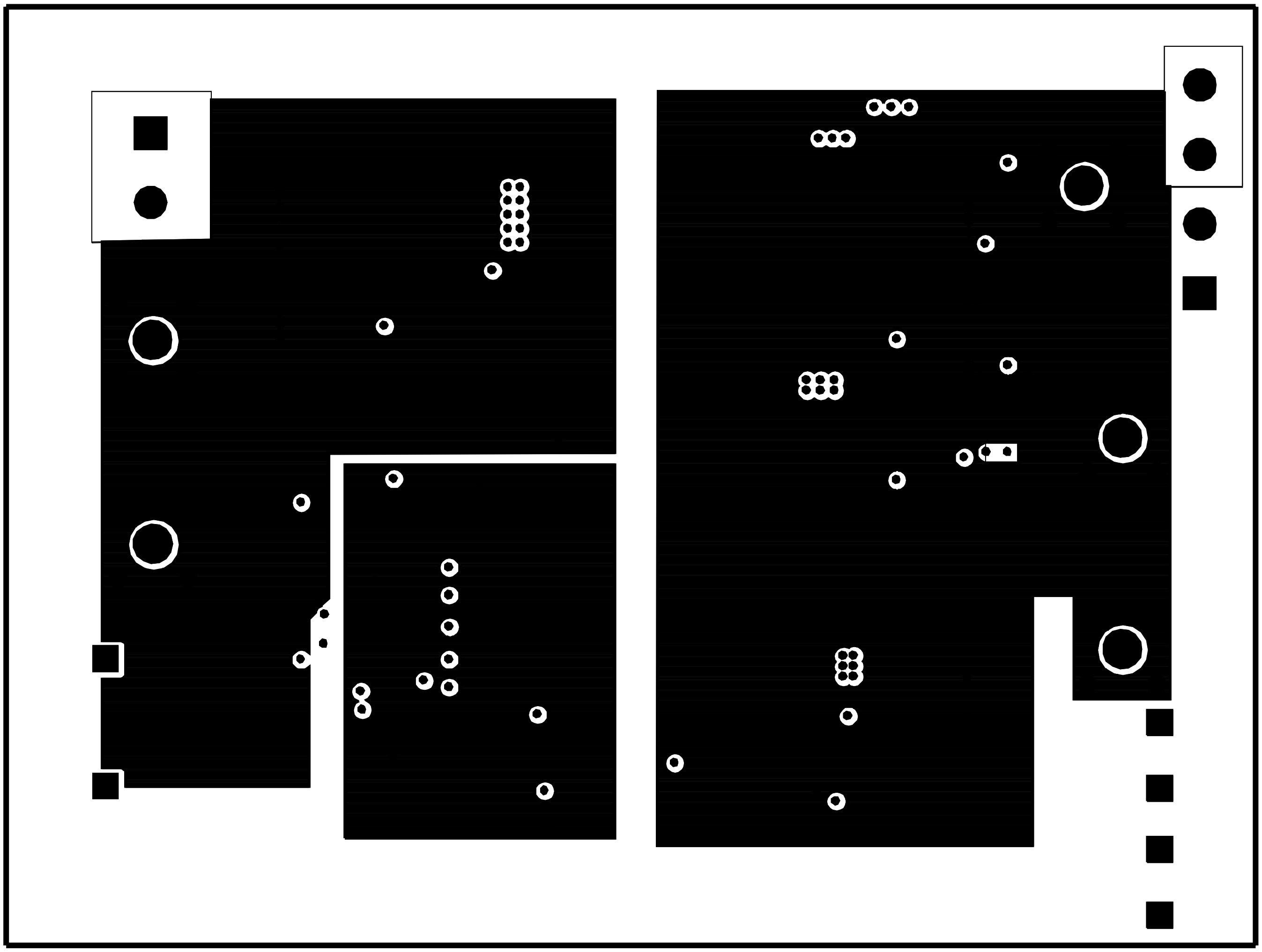

Figure 19. Internal Layer 1 (top view)

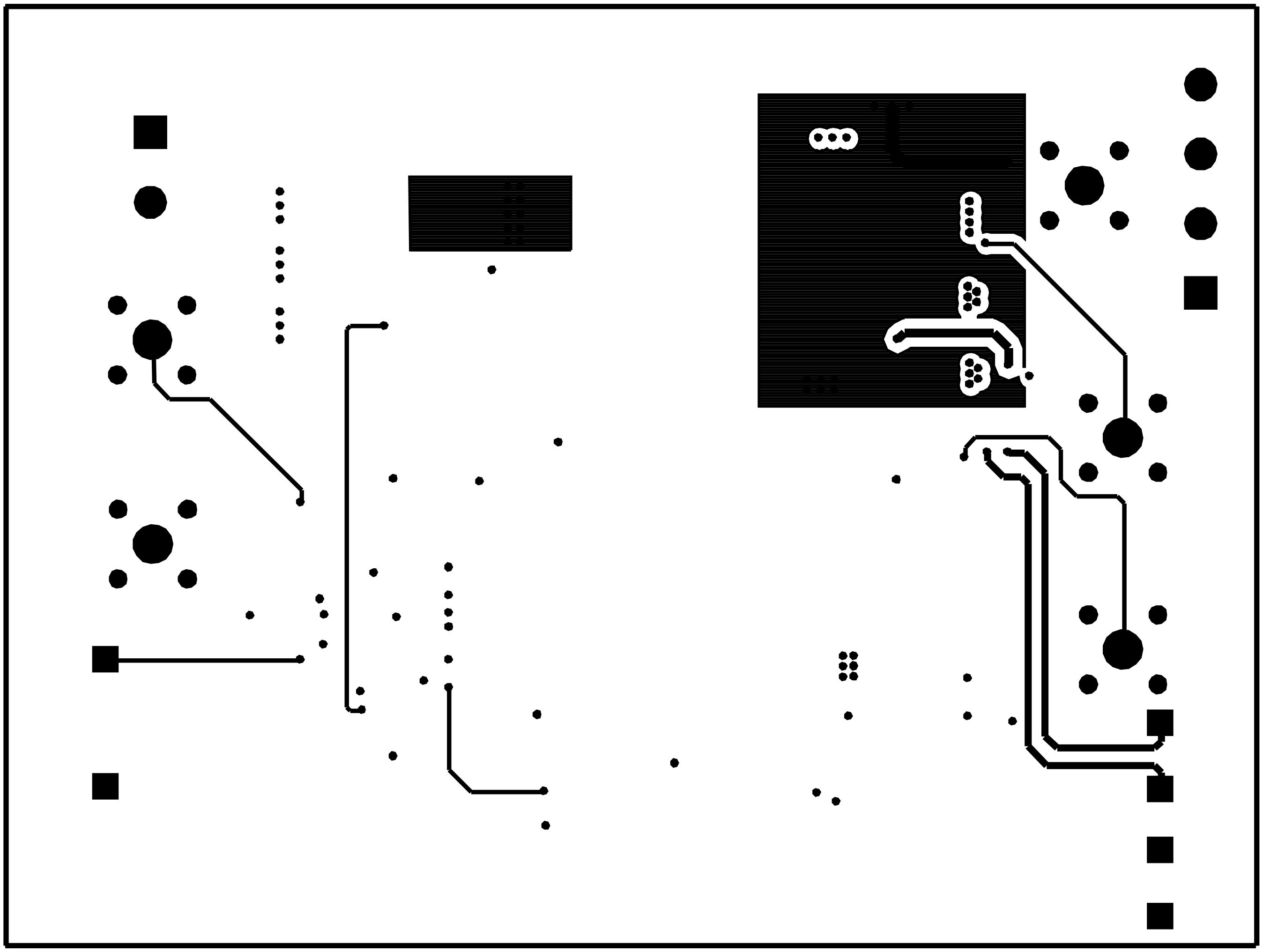

Figure 20. Internal Layer 2 (top view)

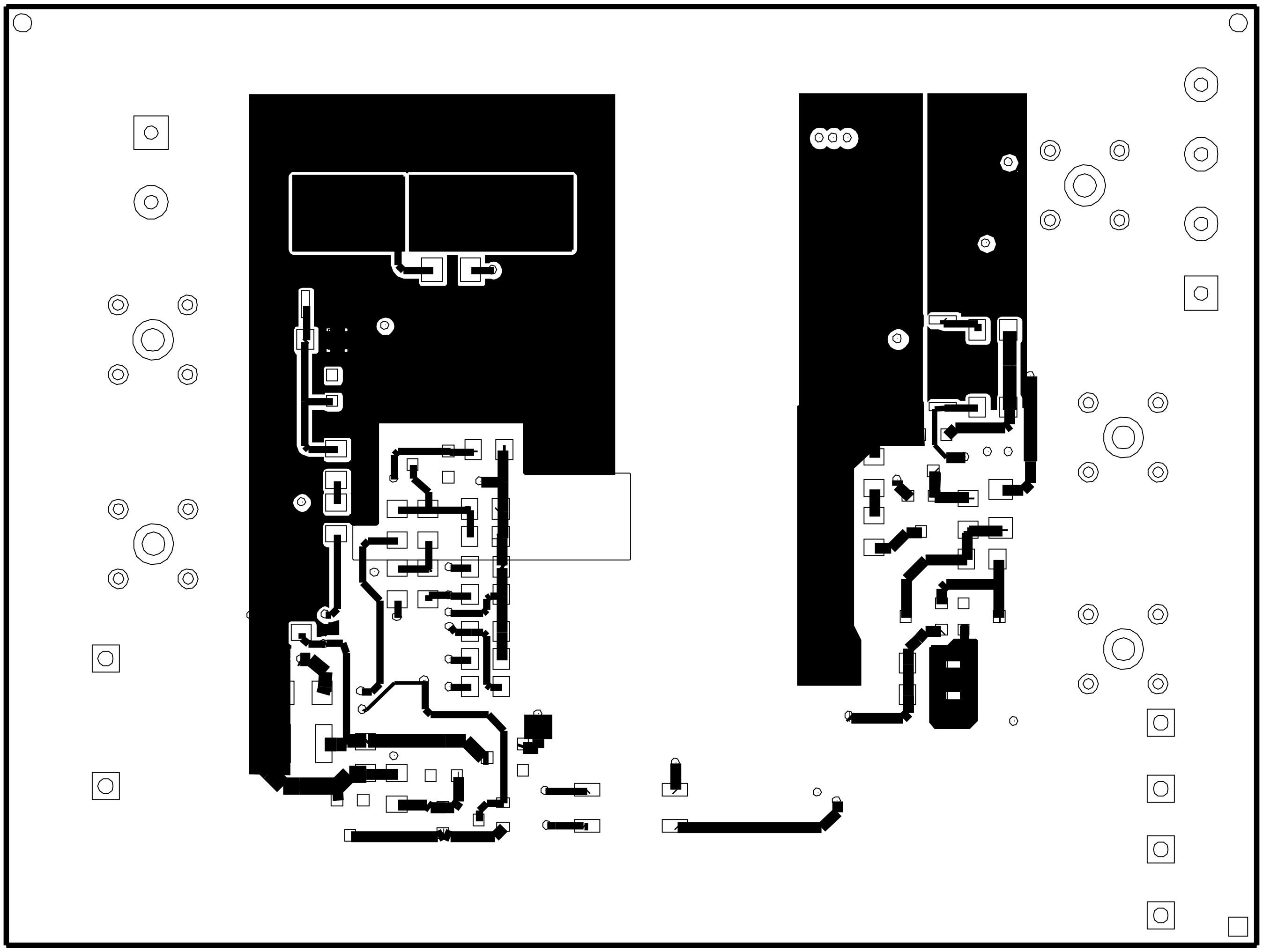

Figure 21. Bottom Copper (top view)

9 List of Materials

Table 2. EVM Components (shown in Figure 1)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
3	C1, C2, C4	Capacitor, ceramic, 2.2 µF, 100 V, X7R, 20%, 1812	C4532X7R2A225M	TDK
2	C10, C12	Capacitor, ceramic, 16 V, X5R, 20%, 10 µF, 1206	std	std
0	C11	Capacitor, ceramic, vvV, [temp], [tol], open, 1210	Std	Vishay
1	C13	Capacitor, ceramic, 25 V, X5R, 10%, 2.2 µF, 0805	std	std
1	C14	Capacitor, ceramic, 50 V, X7R, 20%, 1000 pF, 0805	std	std
1	C15	Capacitor, ceramic, 50 V, X7R, 10%, 82 nF, 0805	std	std
1	C16	Capacitor, ceramic, 50 V, X7R, 10%, 270 pF, 0805	std	std
3	C18, C26, C27	Capacitor, ceramic, 25 V, X7R, 10%, 1.0 µF, 0805	std	std
2	C19, C20	Capacitor, POSCAP, 9.0 mΩ, 6.3 V, 20%, 330 µF, 7343 (D)	6TPF330M9L	Sanyo
0	C22	Capacitor, ceramic, 50 V, X7R, 10%, open, 0805	std	std
1	C23	Capacitor, ceramic, 16 V, X7R, 10%, 1.5 µF, 0805	std	std
1	C25	Capacitor, ceramic, 50 V, X7R, 10%, 8.2 nF, 0805	std	std
2	C3, C17	Capacitor, ceramic, 50 V, X7R, 20%, 0.1 µF, 0805	std	std
3	C5, C21, C24	Capacitor, ceramic, 50 V, NPO, 10%, 100 pF, 0805	std	std
2	C6, C7	Capacitor, ceramic, 50 V, X7R, 20%, 0.22 µF, 0805	std	std
1	C8	Capacitor, ceramic, 50 V, X7R, 20%, 10 nF, 0805	std	std
1	C9	Capacitor, ceramic, 250 V, X7R, 10%, 33 nF, 1206	std	std
4	D1, D2, D3, D11	Diode, Schottky, 200 mA, 30 V, SOT23	BAT54	Vishay
1	D10	Diode, Zener, 13 V,150 mW, 13 V, SOT23	BZX84C13-7-F	Diodes
1	D4	Diode, dual Schottky, 200 mA, 30 V, SOT23	BAT54C	Vishay
1	D5	Diode, dual series Schottky, 70 V, SOT23	BAS70-04LT1	On Semi
1	D6	Diode, Zener, 5.1 V, 350 mW, 5.1 V, SOT23	BZX84C5V1	Vishay
2	D7, D8	Diode, switching, 200 mA, 85 V, 350 mW, SOT23	BAS16	Fairchild
1	D9	Adjustable precision shunt regulator, 0.5%, SOT23	TLV431BQDBZT	TI
1	J1	Terminal block, 2 pin, 15 A, 5.1 mm, V_{IN}, 0.40 x 0.35	ED500/2DS	OST
5	J2, J3, J4, J5, J13	Adaptor, 3.5-mm probe clip (or 131-5031-00), 3.5 mm	131-4353-00	Tektronix
6	J6, J7, J9, J10, J11, J12	Printed circuit pin, 0.043 hole, 0.3 length, test pin, 0.043	3103-1-00-15-00-00-08-0	Mill-Max
1	J8	Terminal block, 4 pin, 15 A, 5.1 mm, V_O, 0.80 x 0.35	ED500/4DS	OST
1	L1	Inductor, 2 µH, 1 pri, 1 sec, 0.920x0.78	PA0373	Pulse
1	Q1	MOSFET, P-channel, 150 V, 2.2 A, 240 mΩ, SO8	IRF6216PBF	IR
1	Q2	MOSFET, N-channel, 150 V, 6.7 A, 50 mΩ, S08	Si7846DP	Vishay
4	Q3, Q4, Q5, Q7	MOSFET, N-channel, 30 V, 60 A, 1.6 mΩ LFPAK	RJK0328DPB	Renesas
1	Q6	Bipolar, NPN, 40 V, 600 mA, 225 mW, SOT23	MMBT2222A	Vishay
1	Q8	MOSFET, N-channel, 200 V, 60 mA, 25 Ω, SOT23	ZVN3320F	Zetex
1	R1	Resistor, chip, 1/8 W, 1%, 8.45 kΩ, 0805	std	std
1	R11	Resistor, chip, 1/8 W, 1%, 26.7 kΩ, 0805	std	std
2	R13, R17	Resistor, chip, 1/8 W, 1%, 2.00 kΩ, 0805	std	std
4	R14, R29, R31, R34	Resistor, chip, 1/8 W, 1%, 0 Ω, 0805	Std	Std
1	R18	Resistor, chip, 1/8 W, 1%, 499 Ω, 0805	std	std
1	R19	Resistor, chip, 1/10 W, 1%, 100 kΩ, 0603	std	std
1	R2	Resistor, chip, 1/8 W, 1%, 69.8 kΩ, 0805	std	std
1	R21	Resistor, chip, 1/8 W, 1%, 100 kΩ, 0805	std	std
1	R22	Resistor, chip, 1/8 W, 1%, 5.11 kΩ, 0805	std	Std
2	R24, R33	Resistor, chip, 1/8 W, 1%, 10.0 kΩ, 0805	std	std

Table 2. EVM Components (shown in Figure 1) (continued)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
2	R25, R30	Resistor, chip, 1/8 W, 1%, 51.1 Ω, 0805	std	std
1	R26	Resistor, chip, 1/8 W, 1%, 28.7 kΩ, 0805	std	std
1	R27	Resistor, chip, 1/8 W, 1%, 12.1 kΩ, 0805	std	std
1	R28	Resistor, chip, 1/8 W, 1%, 4.99 kΩ, 0805	std	std
1	R3	Resistor, chip, 1/8 W, 1%, 88.7 kΩ, 0805	std	std
1	R32	Resistor, chip, 1/8 W, 1%, 249 kΩ, 0805	std	std
0	R35, R36	Resistor, chip, 1/8 W, 1%, open, 0805	std	std
1	R37	Resistor, chip, 1/8 W, 1%, 9.09 kΩ, 0805	std	std
6	R4, R10, R15, R16, R20, R23	Resistor, chip, 1/8 W, 1%, 2.21 Ω, 0805	std	std
1	R5	Resistor, chip, 1/8 W, 1%, 158 kΩ, 0805	std	std
1	R6	Resistor, chip, 1/8 W, 1%, 1.82 kΩ, 0805	std	std
3	R7, R8, R12	Resistor, chip, 1/8 W, 1%, 1.00 kΩ, 0805	std	std
1	R9	Resistor, chip, 1/8 W, 1%, 4.64 Ω, 0805	std	std
1	T1	Transformer, current sense, 10 A, 1:100, SMD	P8208	Pulse
1	T2	Transformer, High Frequency Planar	PA0810	Pulse
1	U1	Current-Mode Active Clamp PWM Controller, PW20	UCC2897APW	TI
1	U2	Phototransistor, CTR 100%-300%, SOP4	SFH690BT	Vishay
1	--	PCB, 3.6 In x 2.7 In x 0.062 In	HPA348	Any
4	--	Rubber bumpon transparent, 0.44"x0.2", bumpon	SJ5303	3M

Table 3. EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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Table 4. FCC Warning

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Table 5. EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 36 V_{DC} to 75 V_{DC} and the output voltage of 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60 °C. The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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