

D3SP28081XH18AC

Specifications

| | | | |
|--------------------------|------------|-----------------------|-------------|
| Density: | 1GB | Data Rate: | 1066 Mbps |
| Pin Count: | 204-pin | CAS Latency: | 7 |
| Version: | Unbuffered | Voltage: | 1.5V |
| Type: | SO-DIMM | PCB Layers: | 6 |
| Speed: | PC3-8500 | ECC : | Non-ECC |
| Component Config: | 128Meg x 8 | Module Ranks : | Single Rank |

Features

- Data rate:1066Mbps
- Power supply: VDD= 1.5V \pm 0.075V
- Interface: SSTL_15
- /CAS Latency(CL):5,6,7,8,9
- /CAS write latency(CWL):5,6,7
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- DM masks write data-in at the both rising and falling edges of the data strobe
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Refresh: Auto-Refresh, Self-Refresh
- On Die Thermal Sensor supported(JEDEC optional)
- 8 bit pre-fetch
- Lead-Free Products are RoHS compliant
- Average Refresh Period 7.8us at $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
3.9us at $85^{\circ}\text{C} < \text{TC} \leq 95^{\circ}\text{C}$

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Description

The D3SP28081XH18AC is 128M words X 64 bits, 1 ranks . Unbuffered Small Outline Dual In-Line Memory Module (SO-DIMM) .DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Speed Grade & Key Parameters

| Speed | DDR3-800 | DDR3-1066 | DDR3-1333 | Unit |
|-------------|----------|-----------|-----------|------|
| CL-tRCD-tRP | 6-6-6 | 7-7-7 | 9-9-9 | |
| tCK(min) | 2.5 | 1.875 | 1.5 | ns |
| CAS Latency | 6 | 7 | 9 | tCK |
| tRCD(min) | 15 | 13.13 | 13.5 | ns |
| tRP(min) | 15 | 13.13 | 13.5 | ns |
| tRAS(min) | 37.5 | 37.5 | 36 | ns |
| tRC(min) | 52.5 | 50.625 | 49.5 | ns |
| tRCF(min) | 110 | 110 | 110 | ns |
| tRRD(min) | 10 | 7.5 | 6.0 | ns |
| tFAW(min) | 40 | 37.5 | 30 | ns |

Address Configuration

| | 512MB | 1GB | 1GB | 2GB | 2GB |
|----------------|----------|-----------|-----------|-----------|-----------|
| Organization | 64M X 64 | 128M X 64 | 128M X 72 | 256M X 64 | 256M X 72 |
| Refresh Method | 8K/64ms | 8K/64ms | 8K/64ms | 8K/64ms | 8K/64ms |
| Row Address | A0-A12 | A0-A13 | A0-A13 | A0-A13 | A0-A13 |
| Column address | A0-A9 | A0-A9 | A0-A9 | A0-A9 | A0-A9 |
| Bank Address | BA0-BA2 | BA0-BA2 | BA0-BA2 | BA0-BA2 | BA0-BA2 |
| Auto Precharge | A10 | A10 | A10 | A10 | A10 |
| # of Rank | 1 | 1 | 1 | 2 | 2 |
| # of DRAMs | 4 | 8 | 9 | 16 | 18 |

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Absolute Maximum ratings

| Parameter | Symbol | Rating | Units | Notes |
|-------------------------------------|-------------------|-----------------|-------|-------|
| Voltage on VDD pin relative to Vss | VDD | -0.4V ~ +1.975V | V | |
| Voltage on VDDQ pin relative to Vss | VDDQ | -0.4V ~ +1.975V | V | |
| Input voltage | Vin | -0.4V ~ +1.975V | V | |
| Output voltage | VOUT | -0.4V ~ +1.975V | V | |
| Storage Temperature | T _{STG} | -55 to +100 | °C | 1 |
| Operating case temperature | T _{oper} | 0 to 95 | °C | 2,3 |
| Storage Humidity | H _{STG} | 5 to 95 | % | |
| Power dissipation | PD | 9 | W | |
| Short circuit output current | I _{OUT} | 50 | mA | |

Note:

1. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh(tREFI to 7.8us) in the Extended Temperature Range.
 - b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability(MR2A6=0b and MR2A7=1b) or enable the optional Auto Self-Refresh mode(MR2A6=1b and MR2A7=0b)

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Recommended DC Operating Conditions(SSTL-15)

| Symbol | Parameter | Rating | | | Units | Notes |
|------------|--------------------------------|-----------|-----------|-----------|-------|-------|
| | | Min. | Typ. | Max | | |
| VDD | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| VDDQ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V | 1,2 |
| VSS | Supply Voltage | 0 | 0 | 0 | V | 1 |
| VDDSPD | Supply Voltage | 3.0 | 3.3 | 3.6 | V | |
| VREFCA(DC) | Input reference voltage | 0.49xVDDQ | 0.50xVDDQ | 0.51xVDDQ | V | 1 |
| VREFDQ(DC) | Input reference voltage for DQ | 0.49xVDDQ | 0.50xVDDQ | 0.51xVDDQ | V | 1 |

Note:

1. DDR3 SDRAM component specification.
2. Under all conditions VDDQ must be less than or equal to VDD.

Pin Description

| Pin Name | Description | Pin Name | Description |
|----------------------|-----------------------------------|------------------|---|
| A0~A9,A11 A13-A15 | Address input | VREFCA VREFDQ | Input/Output voltage reference |
| A10(AP) | Auto precharge | /CK0,/CK1 | SDRAM differential clock input |
| A12(/BC) | Bust chop | CK0,CK1 | SDRAM clocks input |
| /RAS | SDRAM Row address strobe | SCL | Clock input for serial PD |
| /CAS | SDRAM Column address strobe | SDA | Data input/output for serial PD |
| /WE | SDRAM write enable | SA0-SA1 | Serial address select input |
| /CS0-/CS1 | Chip select | VDD* | SDRAM core power supply |
| CKE0,CKE1 | SDRAM clock enable | VDDQ* | SDRAM I/O Driver power supply |
| ODT0,ODT1 | On-die termination control | VREF | SDRAM I/O reference supply |
| DQ0-DQ63 | Data input/output | VSS | Ground |
| BA0-BA2 | SDRAM bank addresses | VDDSPD | Serial EEPROM positive power supply |
| DQS0-DQS7 | Input and output data strobe | NC | No connection |
| DM0-DM7 | SDRAM data mask /high data strobe | /RESET | Set DRAM to known state |
| /DQS0-/DQS7 | Input and output data strobe | TEST | Used by memory bus analysis tools(unused on memory DIMMs) |
| VTT | SDRAM I/O termination supply | /EVENT | Temperature event pin |

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Pin Configuration

| Pin | Front | Pin | Front | Pin | Front | Pin | Front | Pin | Front | Pin | Front |
|-----|-------|-----|-------|-----|--------|-----|--------|-----|--------|-----|-------|
| 1 | VREFD | 2 | Vss | 71 | Vss | 72 | Vss | 139 | Vss | 140 | DQ38 |
| 3 | Vss | 4 | DQ4 | KEY | | | | 141 | DQ34 | 142 | DQ39 |
| 5 | DQ0 | 6 | DQ5 | 73 | CKE0 | 74 | CKE1 | 143 | DQ35 | 144 | Vss |
| 7 | DQ1 | 8 | Vss | 75 | VDD | 76 | VDD | 145 | Vss | 146 | DQ44 |
| 9 | Vss | 10 | /DQS0 | 77 | NC | 78 | A15 | 147 | DQ40 | 148 | DQ45 |
| 11 | DM0 | 12 | DQS0 | 79 | BA2 | 80 | A14 | 149 | DQ41 | 150 | Vss |
| 13 | Vss | 14 | Vss | 81 | VDD | 82 | VDD | 151 | Vss | 152 | /DQS5 |
| 15 | DQ2 | 16 | DQ6 | 83 | A12/BC | 84 | A11 | 153 | DM5 | 154 | DQS5 |
| 17 | DQ3 | 18 | DQ7 | 85 | A9 | 86 | A7 | 155 | Vss | 156 | Vss |
| 19 | Vss | 20 | Vss | 87 | VDD | 88 | VDD | 157 | DQ42 | 158 | DQ46 |
| 21 | DQ8 | 22 | DQ12 | 89 | A8 | 90 | A6 | 159 | DQ43 | 160 | DQ47 |
| 23 | DQ9 | 24 | DQ13 | 91 | A5 | 92 | A4 | 161 | Vss | 162 | Vss |
| 25 | Vss | 26 | Vss | 93 | VDD | 94 | VDD | 163 | DQ48 | 164 | DQ52 |
| 27 | /DQS1 | 28 | DM1 | 95 | A3 | 96 | A2 | 165 | DQ49 | 166 | DQ53 |
| 29 | DQS1 | 30 | /RESE | 97 | A1 | 98 | A0 | 167 | Vss | 168 | Vss |
| 31 | Vss | 32 | Vss | 99 | VDD | 100 | VDD | 169 | /DQS6 | 170 | DM6 |
| 33 | DQ10 | 34 | DQ14 | 101 | CK0 | 102 | CK1 | 171 | DQS6 | 172 | Vss |
| 35 | DQ11 | 36 | DQ15 | 103 | /CK0 | 104 | /CK1 | 173 | Vss | 174 | DQ54 |
| 37 | Vss | 38 | Vss | 105 | VDD | 106 | VDD | 175 | DQ50 | 176 | DQ55 |
| 39 | DQ16 | 40 | DQ20 | 107 | A10/AP | 108 | BA1 | 177 | DQ51 | 178 | Vss |
| 41 | DQ17 | 42 | DQ21 | 109 | BA0 | 110 | /RAS | 179 | Vss | 180 | DQ60 |
| 43 | Vss | 44 | Vss | 111 | VDD | 112 | VDD | 181 | DQ56 | 182 | DQ61 |
| 45 | /DQS2 | 46 | DM2 | 113 | /WE | 114 | /S 0 | 183 | DQ57 | 184 | Vss |
| 47 | DQS2 | 48 | Vss | 115 | /CAS | 116 | ODT0 | 185 | Vss | 186 | /DQS7 |
| 49 | Vss | 50 | DQ22 | 117 | VDD | 118 | VDD | 187 | DM7 | 188 | DQS7 |
| 51 | DQ18 | 52 | DQ23 | 119 | A13 | 120 | ODT1 | 189 | Vss | 190 | Vss |
| 53 | DQ19 | 54 | Vss | 121 | /S 1 | 122 | NC | 191 | DQ58 | 192 | DQ62 |
| 55 | Vss | 56 | DQ28 | 123 | VDD | 124 | VDD | 193 | DQ59 | 194 | DQ63 |
| 57 | DQ24 | 58 | DQ29 | 125 | TEST | 126 | VREFCA | 195 | Vss | 196 | Vss |
| 59 | DQ25 | 60 | Vss | 127 | Vss | 128 | Vss | 197 | SA0 | 198 | NC |
| 61 | Vss | 62 | /DQS3 | 129 | DQ32 | 130 | DQ36 | 199 | VDDSPD | 200 | SDA |
| 63 | DM3 | 64 | DQS3 | 131 | DQ33 | 132 | DQ37 | 201 | SA1 | 202 | SCL |
| 65 | Vss | 66 | Vss | 133 | Vss | 134 | Vss | 203 | VTT | 204 | VTT |
| 67 | DQ26 | 68 | DQ30 | 135 | /DQS4 | 136 | DM4 | | | | |
| 69 | DQ27 | 70 | DQ31 | 137 | DQS4 | 138 | Vss | | | | |

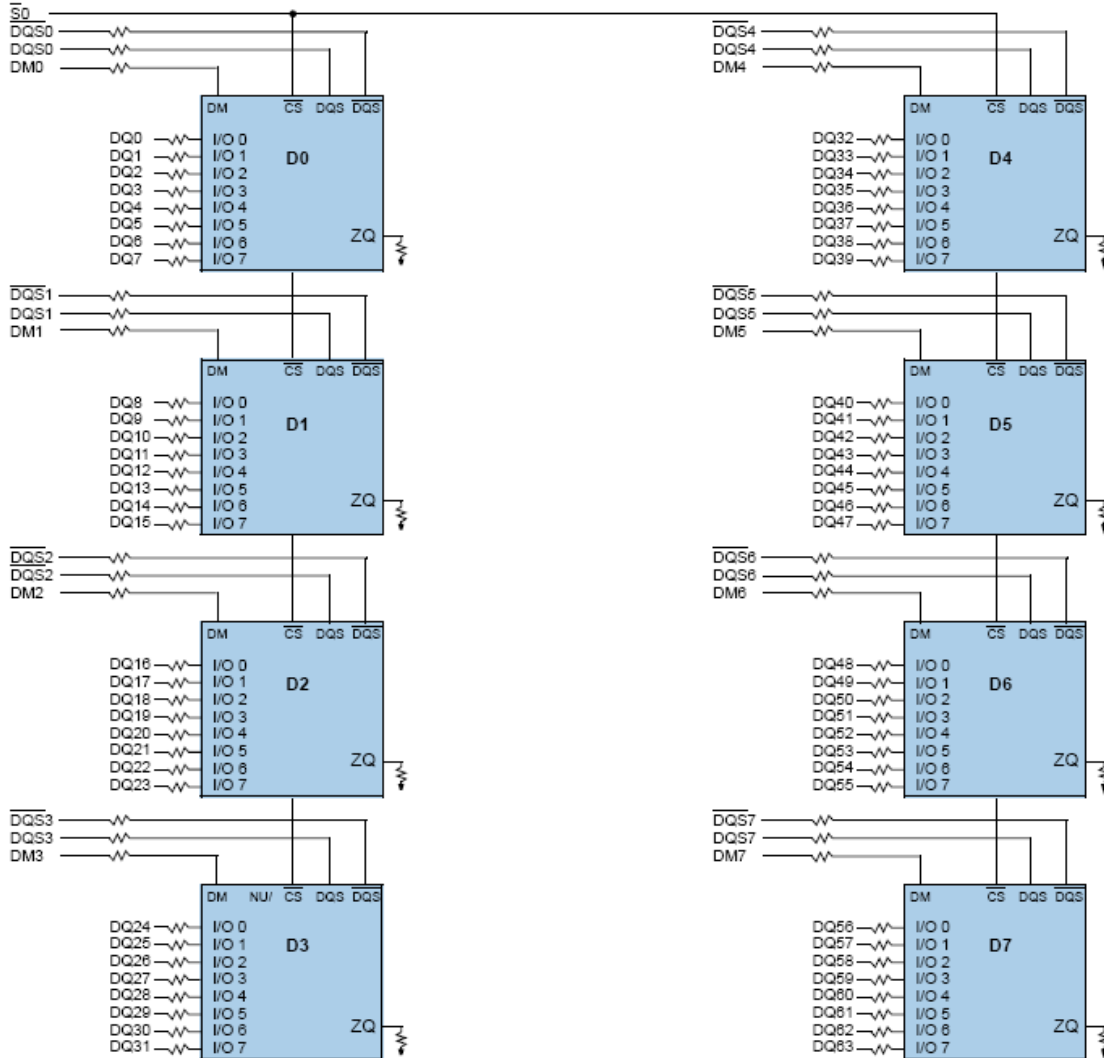
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Input/Output Functional Description

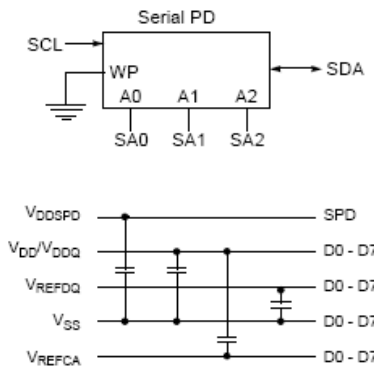
| Symbol | Type | Function |
|--|--------|---|
| CK0-CK1 /CK0-/CK1 | Input | The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operation is synchronized to the input clock. |
| CKE0,CKE1 | Input | Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clock, CKE low initiates the Power Down mode, or the Self-Refresh mode. |
| /S0,/S1 | Input | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new command are ignored but previous operations continue. Rank0 is selected by /S0;Rank1 is selected by /S1 |
| /RAS,/CAS,/WE | Input | \overline{RAS} , \overline{CAS} , and \overline{WE} (ALONG WITH /S) define the command being entered. |
| ODT0-ODT1 | Input | When high, termination resistance is enabled for all DQ, DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS). |
| VREFDQ | Supply | Reference voltage for SSTL 15 I/O Inputs. |
| VREFCA | Supply | Reference voltage for SSTL 15 command/address inputs. |
| VDDQ | Supply | Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins. |
| BA0-BA2 | Input | Selects which SDRAM bank of eight is activated. |
| A0-A9 A10(AP) A11 A12(/BC) A13-A15 | Input | During a Bank Activate command cycle, Address input defines the row address(RA0-RA13) During a Read or Write command cycle. Address input defines the column address. In addition to the column address. AP is used to invoke autprecharge operation at the end of the burst read or write cycle. If AP is high, autprecharge is selected and BA0, BA1,BA2 defines the bank to be precharged. If AP is low, autprecharge is disabled. During a precharge command cycle, AP is used in conjunction with BA0,BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0,BA1,BA2. If AP is low, BA0, BA1 are used to define which bank to precharge. |
| DQ0-DQ63 | I/O | Data input/Output pins. |
| DM0-DM8 | Input | DM is and input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. |
| VDD, Vss | Supply | Power and ground for DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules. |
| DQS0-DQS8 /DQS0-/DQS8 | I/O | Data strobe for input and output data. |
| SA0-SA2 | Input | These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EEPROM address range. |
| SDA | I/O- | This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board. |
| SCL | Input | This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board. |
| /EVENT | | This signal indicates that a thermal event has been detected in the thermal sensing device. The system Should guarantee the electrical level requirement is met for /EVENT pin on TS/SPD part |
| VDD SPD | Supply | Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V. |

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FUNCTIONAL BLOCK DIAGRAM



- BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D7
- A0 - A13 → A0-A13 : SDRAMs D0 - D7
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D7
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D7
- CKE0 → CKE : SDRAMs D0 - D7
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D7
- ODT0 → ODT : SDRAMs D0 - D7
- CK0 → CK : SDRAMs D0 - D7

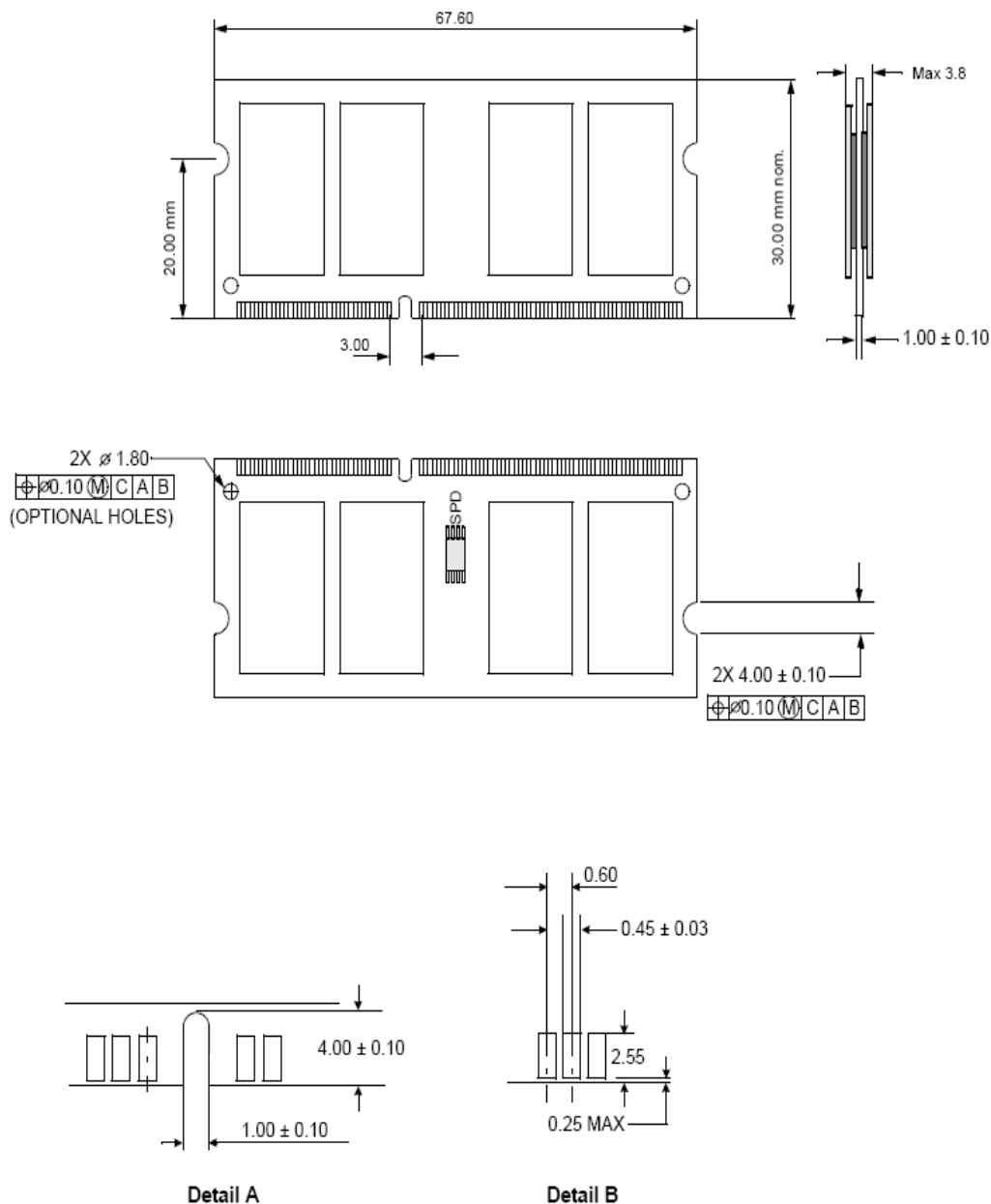


- Note :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DQS/ODT/DM/CKE/ $\overline{\text{S}}$ relationships must be maintained as shown.
 3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
 4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
 5. Refer to section 7.1 of this document for details on address mirroring.
 6. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
 7. One SPD exists per module.

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PACKAGE DIMENSIONS

Unit :mm



Tolerances : ± 0.15 mm unless otherwise specified

The used device is 128Mx8 PROMOS, DDR3,FBGA
DDR3 SDRAM Part No.: **V73CBG01808RBJ11 *8EA**

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Declaration of Compliance with the RoHS Directive

DATA SPECIALTIES CO.,LTD Hereby declares that the products compliant with the European Union Directive 2002/95/EC for Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment(RoHS Directive).

Below list of DSL(DATA SPECIALTIES CO.,LTD.) products are Compliance.

| No. | Substance | Max. Conc. |
|-----|--------------------------------------|------------|
| 1 | Cd (Cadmium) | <100ppm |
| 2 | Hg (Mercury) | <1000ppm |
| 3 | Pb (Lead) | <1000ppm |
| 4 | Cr+6 (Hexavalent Chromium) | <1000ppm |
| 5 | PBB (Polybrominated Biphenyl ethers) | <1000ppm |
| 6 | PBDE (Polybrominated Diphenyl) | <1000ppm |

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Declaration of Compliance with the PFOS Directive

DATA SPECIALTIES CO.,LTD Hereby declares that the products compliant with DIRECTIVE 2006/122/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL regarding exception of the use in photoresist or anti reflective coatings for photolithography (usually semiconductor).

Only some kind of DATA SPECIALTIES CO.,LTD. Use PFOS in photoresist process, but do not contain PFOS in the Product.

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