May 2004

RMBA09501

Cellular 2 Watt Linear GaAs MMIC Power Amplifier

General Description

The RMBA09501 is a highly linear Power Amplifier. The two stage circuit uses our pHEMT process. It is designed for use as a driver stage for Cellular base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for CDMA operation.

Features

- 2 Watt Linear output power at 36dBc ACPR1 for CDMA operation
- Small Signal Gain of > 30dB
- Small outline SMD package

Device

Absolute Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Drain Supply Voltage[1]		+10	V
V_{GS}	Gate Supply Voltage		-5	V
P_{RF}	RF Input Power (from 50Ω source)		+5	dBm
T_C	Case Operating Temperature	-30	+85	°C
T_S	Storage Temperature	-40	+100	°C

Note:
1. Only under quiescent conditions—no RF applied.

Electrical Characteristics[2]

Parameter	Min	Typ	Max	Units
Frequency Range	869		894	MHz
Gain (Small Signal)		35		dB
Gain Variation: Over Frequency Range Over Temperature Range		 ±1.5 ±2.5		 dB dB
Noise Figure		6		dB
Linear Output Power: for CDMA[3]	33			dBm
OIP3[5]		43		dBm
Idd @ 33dBm Pout – 7V		1.0		A
PAE @ 33dBm Pout		28.5		%
Input VSWR (50Ω)		2:1		
RF Input Power		+1		dBm
Drain Voltage (V_{DD})		7.0		V
Gate Voltages (VG_1, VG_2)[4]	-2		-0.25	V
Quiescent Currents (IDQ1, IDQ2)[4]		150, 400		mA
Thermal Resistance (Channel to Case) Rjc		11		°C/W

Notes:

2. V_{DD} = 7.0V, T_C = 25°C. Part mounted on evaluation board with input and output matching to 50Ω.
3. 9 Channel Forward Link QPSK Source; 1.23Mbps modulation rate. CDMA ACPR1 is measured using the ratio of the average power within the 1.23MHz channel at band center to the average power within a 30KHz bandwidth at an 885KHz offset. Minimum CDMA output power is met with ACPR1 > 36dBc.
4. VG1 and VG2 must be individually adjusted to achieve IDQ1 and IDQ2. A single VGG bias supply adjusted to achieve IDQTOTAL = 550mA can be used with nearly equivalent performance. Values for IDQ1 and IDQ2 shown have been optimized for CDMA operation. IDQ1 and IDQ2 (or IDQTOTAL) can be adjusted to optimize the linearity of the amplifier for other modulation systems.
5. OIP3 specifications are achieved for power output levels of 27 and 30 dBm per tone with tone spacing of 1.25MHz at bandcenter.

The device requires external input and output matching to 50Ω as shown in Figure 3 and the Parts List.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

The following describes a procedure for evaluating the RMBA09501, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for Cellular Base stations, or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. The RMBA09501 requires external passive components for DC bias and RF input and output matching circuits as shown in Figure 3 and the Part List. A recommended schematic circuit is shown in Figure 3. The gate biases for the two stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of Figure 3. The following designations should be noted:

(1) Pin designations are as shown in Figure 2.

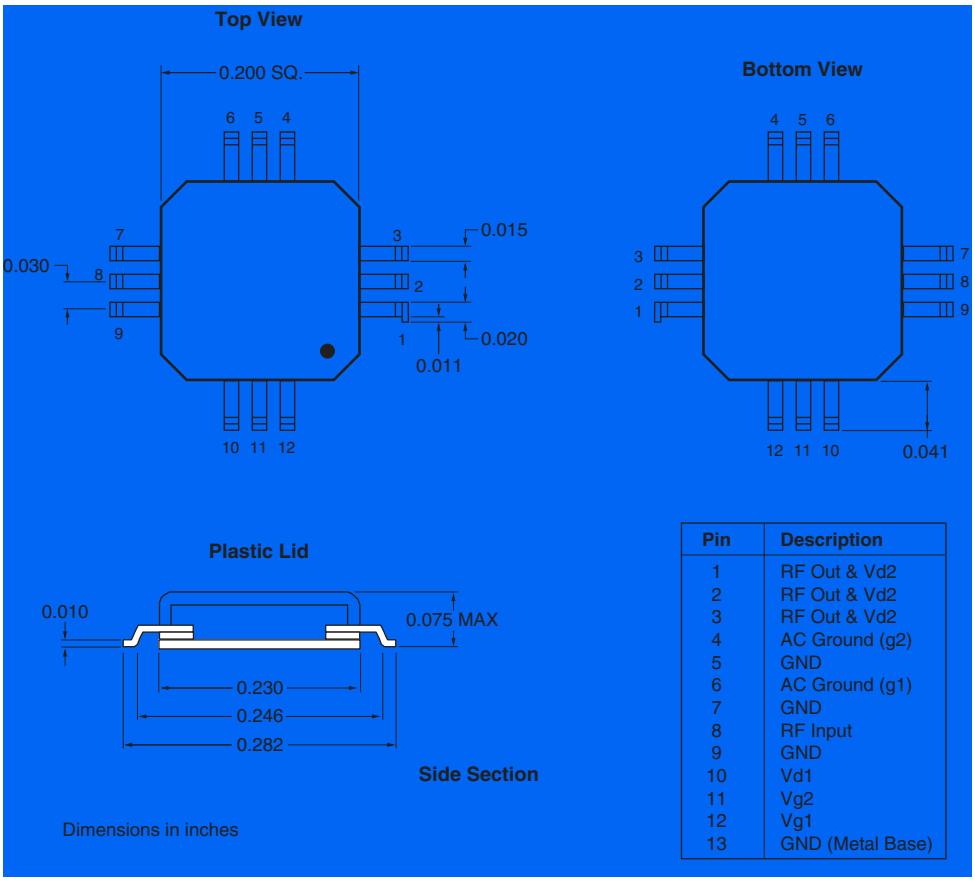
(2) Vg1 and Vg2 are the Gate Voltages (negative) applied at the pins of the package.

(3) Vgg1 and Vgg2 are the negative supply voltages at the evaluation board terminals.

(4) Vd1 and Vd2 are the Drain Voltages (positive) applied at the pins of the package.

(5) Vdd1 and Vdd2 are the positive supply voltages at the evaluation board terminals.

Note: The 2 terminals of Vdd1 and Vdd2 may be tied together. The base of the package must be soldered on to a heat sink for proper operation.



Pin	Description
1	RF Out & Vd2
2	RF Out & Vd2
3	RF Out & Vd2
4	AC Ground (g2)
5	GND
6	AC Ground (g1)
7	GND
8	RF Input
9	GND
10	Vd1
11	Vg2
12	Vg1
13	GND (Metal Base)

Figure 1. Package Outline and Pin Designations

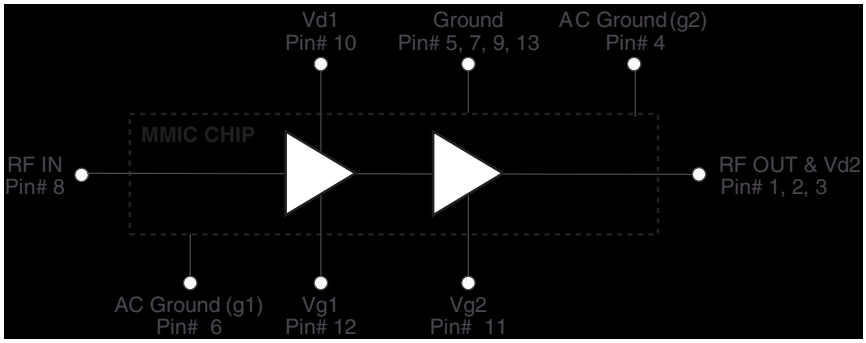


Figure 2. Functional Block Diagram of Packaged Product

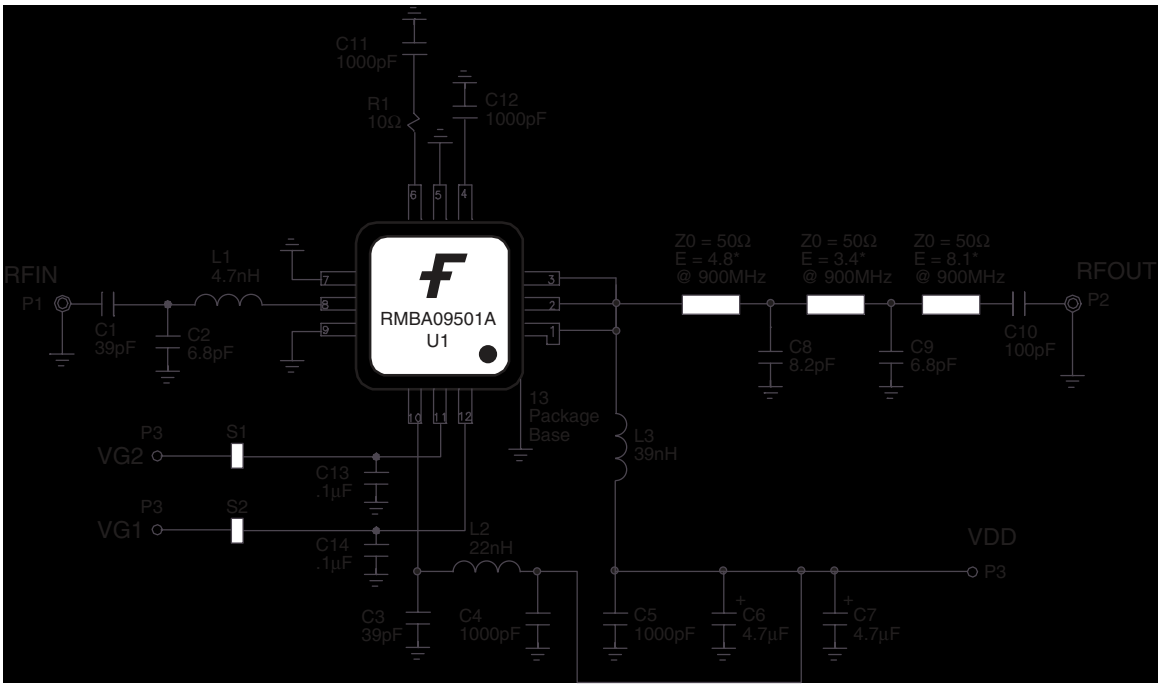


Figure 3. Schematic of Application Circuit Showing External Components

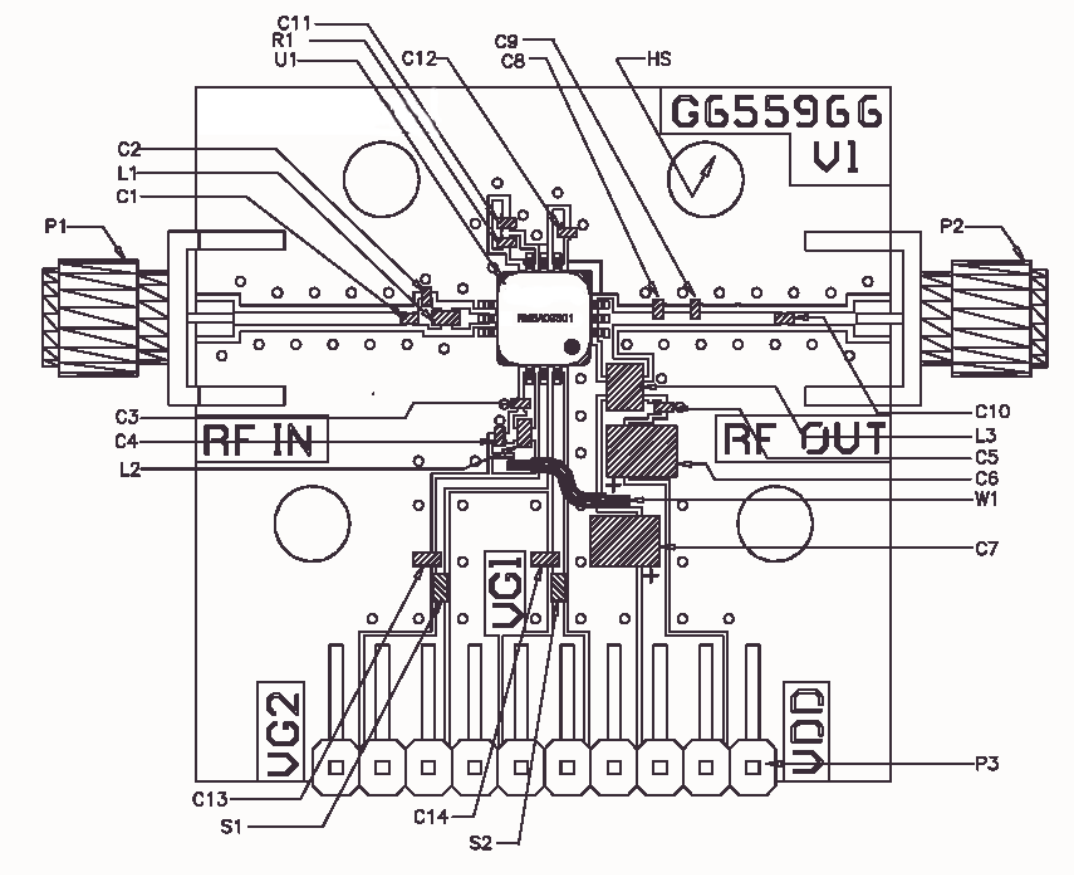


Figure 4. Layout of Test Evaluation Board (RMBA09501-TD, G657471)

Test Procedure for the Evaluation Board (RMBA09501-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA09501.) Note: Vdd1, 2 are tied together.

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Slowly apply gate supply voltages as specified on results sheet supplied with test board to the board terminals Vgg1 and Vgg2.

Step 3: Slowly apply drain supply voltages of +7.0V to the board terminals Vdd1, 2. Adjust Vgg to set the total quiescent current Idq1 and Idq2 (with no RF applied) Idq as per supplied result sheet. Gate supply voltages (Vgg i.e., Vgg1, Vgg2) may be adjusted, only if quiescent current (Idq1 and Idq2) values desired are different from those noted on the data summary supplied with product samples.

Step 4: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 5: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltages Vdd1, 2.

(iii) Turn down and off gate voltages Vgg1 and Vgg2.

Parts List for Test Evaluation Board (RMBA09501-TB, G654188/G654942)

Part	Value	Size (EIA)	Vendor(s)
C1, C3	39pF	0402	Murata, GRM36COG390J050
C2, C9	6.8pF	0402	Murata, GRM36COG6R8B050
C8	8.2pF	0402	Murata, GRM36COG8R2B50
C4, C5, C11, C12	1000pF	0402	Murata, GRM36X7R102K050
C6, C7	4.7µF	3528	TDK, C3216X7R102K050
L1	4.7nH	0603	Toko, LL1608-FH4N7S
L2	22nH	0603	Toko, LL1608-FH22NK
L3	39nH	1008	Coilcraft, 1008HQ-39NTKBC
R1	10Ω	0402	IMS, RCI-0402-10R0J
S1, S2			Bar or Ni Ribbon Short
W1	26AWG (0.015" dia) Wire		Alpha, 2853/1
U1	RMBA09501 PA		Fairchild Semiconductor
P3	Right angle Pin Header		3M 2340-5211TN
P1, P2	Brass SMA Connectors		Johnson Components 142-0701-841
Board	FR4		Raytheon Dwg# G654626, V1
C10	100pF	0603	Murata, GRM36COG101J50
C13, C14	1.0µF	0805	Murata, GRM39Y5V104Z50

Thermal Considerations for Heat Sinking the RMBA09501

The PWB must be prepared with either an embedded copper slug in the board where the package is to be mounted or a heat sink should be attached to the backside of the PWB where the package is to be mounted on the front side. The slug or the heat sink should be made of a highly electrically and thermally conductive material such as copper or aluminum. The slug should be at least the same thickness as the PWB. In the case of the heat sink, a small pedestal should protrude through a hole in the PWB where the package bottom is directly soldered. In either configuration, the top surface of the slug or the pedestal should be made coplanar with the package lead mounting plane i.e., the top surface of the PWB. Use Sn96 solder (96.5% Sn and 3.5% Ag) at 220°C for 20 seconds or less to attach the heat sink to the backside of the PWB. Then, using Sn63, the package bottom should be firmly soldered to the slug or the pedestal while the pins are soldered to the respective pads on the front side of the PWB without causing any stress on the pins. Remove flux completely if used for soldering.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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