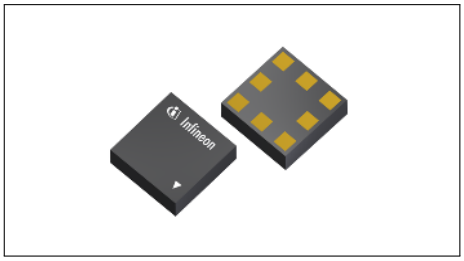
BGSA20VGL8

High RF Voltage Dual SPST Antenna Aperture Shunt Switch

Features

- Dual SPST designed for high-linearity antenna aperture switching and RF tuning applications
- Low R_{ON} resistance of 1.6 ohm at each port in ON state
- Low C_{OFF} capacitance of 240 fF at each port in OFF state
- > 67 V RF voltage OFF state handling
- Low harmonic generation
- GPIO control interface - including 4 control states
- Supply voltage range: 1.65 to 3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.1 mm (MSL1, 260°C per JEDEC J-STD-020)
- Suitable for EDGE/CDMA/WCDMA/C2K/LTE/5G Applications
- RoHS and WEEE compliant package



1.1 x 1.1 mm^2

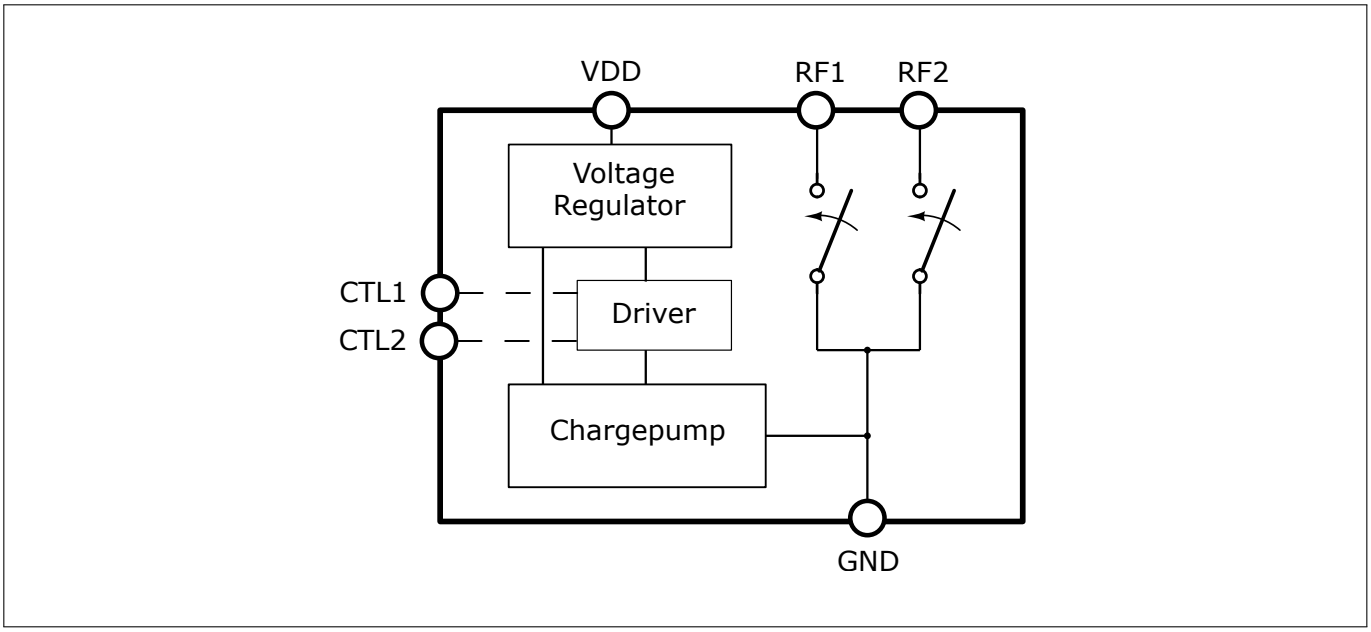
Application

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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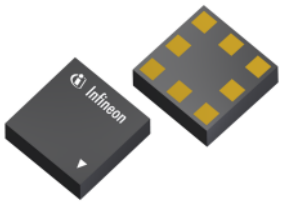
1 Features



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RoHS Halogen-Free Lead-Free Greer

Description

The BGSA20VGL8 is a versatile Dual Single Pole Single Throw (SPST) RF antenna shunt aperture switch optimized for low C_{off} as well as low R_{on} enabling applications up to 6.0 GHz. This single supply chip integrates 2 digital control pins. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Product Name	Marking	Package	Ordering Information
BGSA20VGL8	V	TSLP-8-1	BGSA 20VGL8 E6327

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	–	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	6	V	only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF voltage	V_{RF_max}	–	–	70	V	Short term peaks (1μs in 0.1% duty cycle), exceeding typical linearity, Ron and Coff parameters, in Isolation mode, test condition schematic in Fig. 1
ESD robustness, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD robustness, HBM [4]	$V_{ESD_{HBM}}$	-2	–	+2	kV	
Junction temperature	T_j	–	–	125	°C	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTL}	-0.7	–	3.3	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider potential ripple voltages on top of V_{DD}. Including RF ripple, V_{DD} must not exceed the maximum ratings: $V_{DD} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

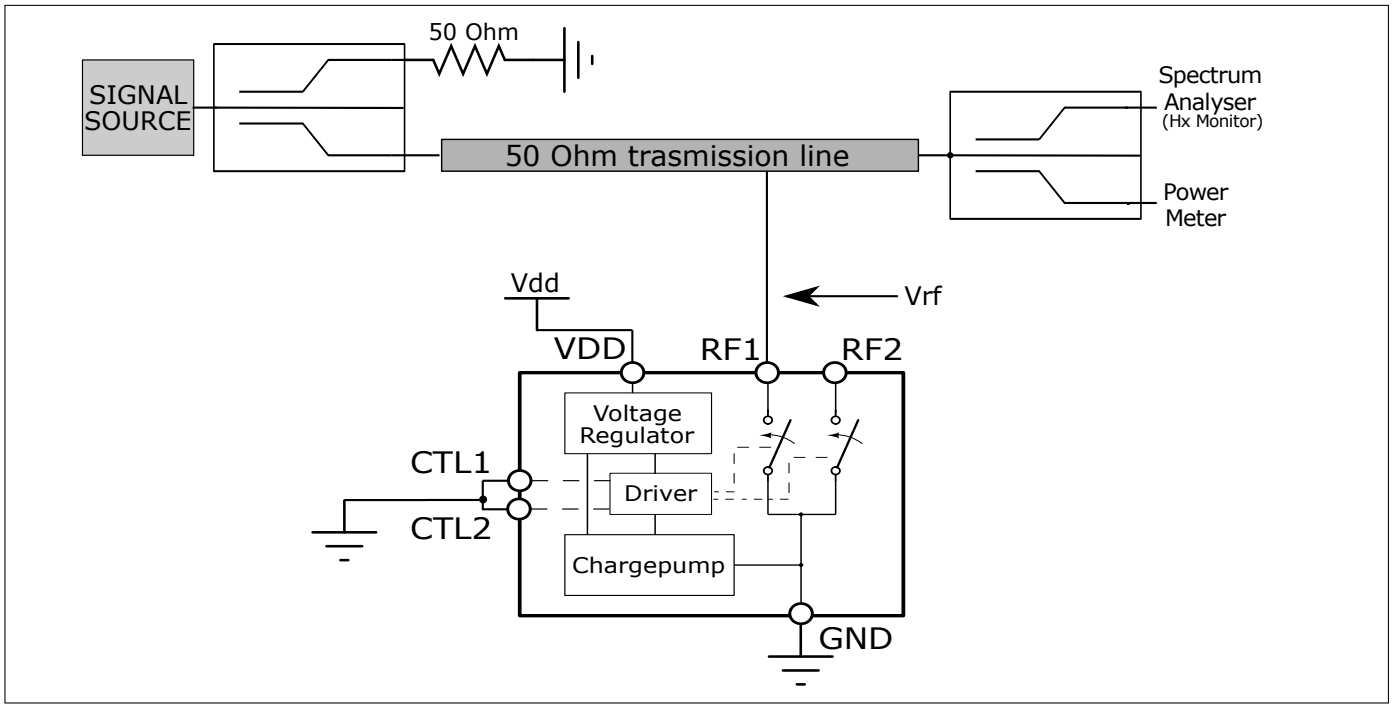

Figure 1: RF operating voltage measurement configuration - All OFF mode. RF1 stressed.

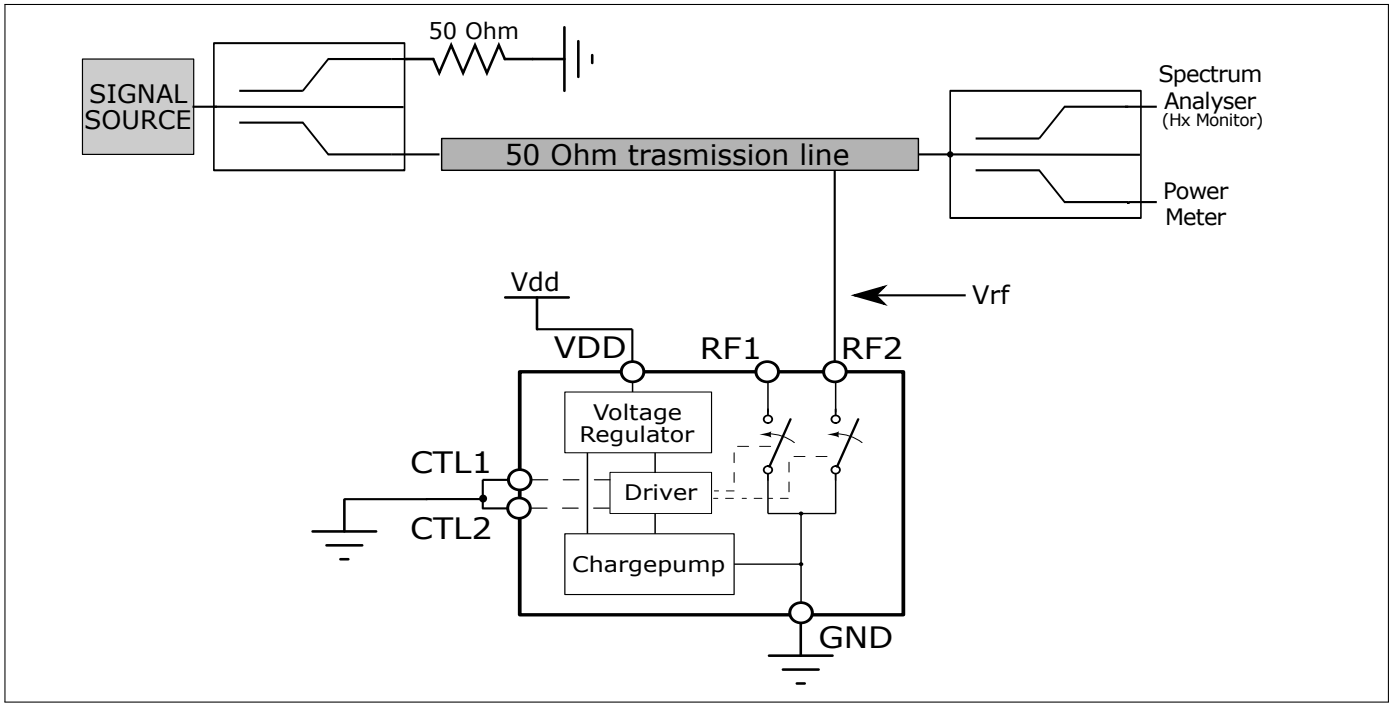

Figure 2: RF operating voltage measurement configuration - All OFF mode. RF2 stressed.

3 DC Characteristics

Table 2: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.6	V	–
Supply current	I_{DD}	40	70	–	µA	–
Control voltage low	$V_{Ctl,low}$	0	–	0.45	V	–
Control voltage high	$V_{Ctl,high}$	1.2	1.8	2.85	V	$V_{Ctl,high} \ll V_{DD}$
Control current low	$I_{Ctl,low}$	-1	0	1	µA	–
Control current high	$I_{Ctl,high}$	-1	0	4	µA	$V_{Ctl,high} \ll V_{DD}$ 1 MΩ Pull-Down resistor at Control Pins
Ambient temperature	T_A	-40	25	85	°C	–
RF switching time	t_{ST}		4.5	8	µs	P_{IN} = 0 dBm, Z_0 = 50 Ω, T_A = −40 °C... + 85 °C V_{DD} = 1.65 – 3.6 V Referring Fig. 3
Startup time	t_{Pup}		8	10	µs	

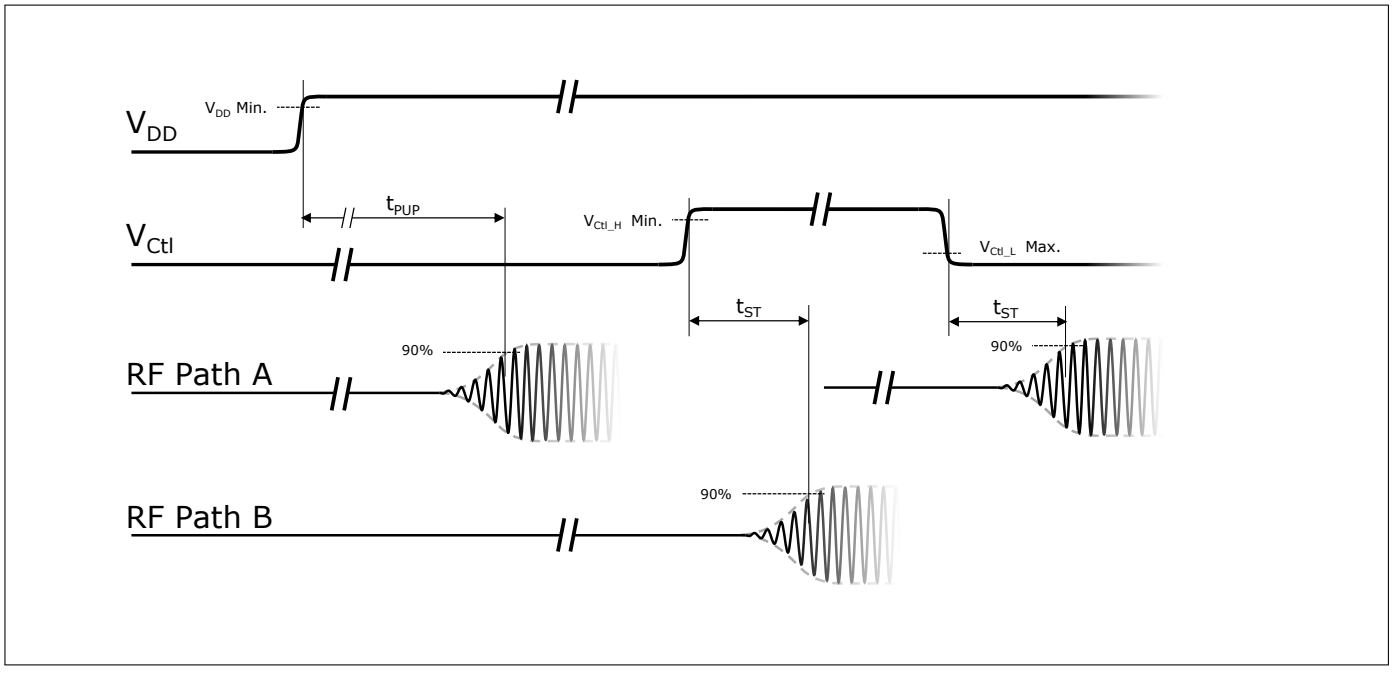

Figure 3: Switching Time Definition

4 RF Small Signal Characteristics

Table 3: Parametric specifications using SPST configuration

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
RF1 or RF2 to Ground ON DC resistance	R_{ON}		1.6	1.7	Ω	V_{DD} = 1.65 – 3.6 V, T_A = 25 °C
RF1 or RF2 to Gnd OFF DC resistance	R_{OFF}	250	270		kΩ	
RF1 or RF2 to Ground OFF capacitance	C_{OFF}		240	300	fF	V_{DD} = 1.65 – 3.6 V, T_A = 25 °C, extracted from Isolation (S21) measurement Z_0 = 50 Ω

Table 4: RF electrical parameters

Isolation: RF1 to RF2 or RF2 to RF1 [1,2,3]

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
698 - 910 MHz	ISO_{RF1RF2}	49	53		dB	V_{DD} = 1.65 – 3.6 V, Z_0 = 50 Ω, T_A = –40 °C... + 85 °C
1710 - 1910 MHz		43	45		dB	
1911 - 2169 MHz		42	44		dB	
2170 - 2690 MHz		40	43		dB	
3300 - 3800 MHz		38	40		dB	
3801 - 4800 MHz		35	39		dB	
4801 - 6000 MHz		32	37		dB	

[1] Valid for all RF power levels, no compression behavior
[2] SOLT-calibrated, P_{IN} = 0 dBm
[3] On application board without any matching components

5 RF large signal parameter

Table 5: RF large signal specifications at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Max. RF Operating Voltage	V_{RF_opr}	–	–	67	V	In Isolation mode 900MHz, test condition schematic in Fig. 1 or Fig. 2 for H2/H3 < -33 dBm @ 50Ω
Harmonic Generation up to 12.75 GHz						
All RF Ports - Second Order Harmonics	P_{H2}		-76	-73	dBm	25 dBm, 50Ω, f_0 = 663 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-86	-85	dBm	25 dBm, 50Ω, f_0 = 663 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Second Order Harmonics	P_{H2}		-58	-56	dBm	35 dBm, 50Ω, f_0 = 920 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-72	-70	dBm	35 dBm, 50Ω, f_0 = 920 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Second Order Harmonics	P_{H2}		-58	-55	dBm	33 dBm, 50Ω, f_0 = 1910 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-70	-68	dBm	33 dBm, 50Ω, f_0 = 1910 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Second Order Harmonics	P_{H2}		-66	-64	dBm	25 dBm, 50Ω, f_0 = 2690 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-79	-77	dBm	25 dBm, 50Ω, f_0 = 2690 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Second Order Harmonics	P_{H2}		-65	-63	dBm	25 dBm, 50Ω, f_0 = 3500 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-80	-78	dBm	25 dBm, 50Ω, f_0 = 3500 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Second Order Harmonics	P_{H2}		-66	-64	dBm	25 dBm, 50Ω, f_0 = 5000 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports - Third Order Harmonics	P_{H3}		-81	-80	dBm	25 dBm, 50Ω, f_0 = 5000 MHz, test condition in Fig. 1 and Fig. 2
All RF Ports	P_{Hx}	–	–	-80	dBm	25 dBm, 50Ω
Intermodulation Distortion IMD2						
IIP2, low	IIP2,l	123	125	131	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	127	130	135	dBm	
Intermodulation Distortion IMD3						
IIP3	IIP3	77	78	79	dBm	IIP3 conditions table 9

RF large signal parameter

Table 6: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 7: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

6 Logic Table

Table 8: Logic Table

CTL 1	CTL 2	Mode
0	0	RF1 and RF2 isolated from ground
0	1	RF2 connected to ground
1	0	RF1 connected to ground
1	1	RF1 and RF2 connected to ground

7 Application Information

Pin Configuration and Function

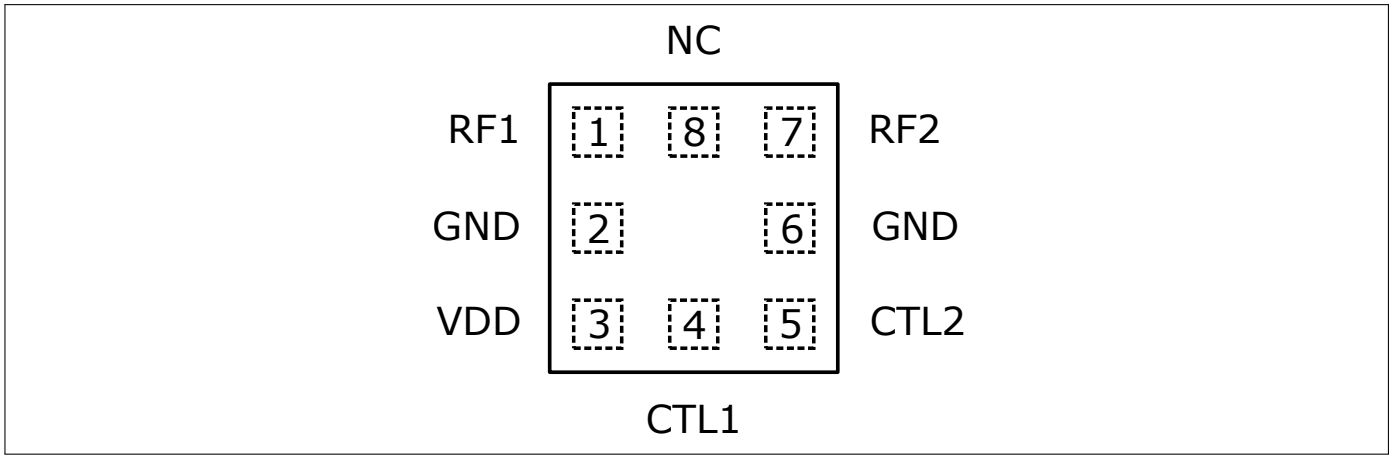

Figure 4: BGSA20VGL8 Pin Configuration (top view)

Table 9: Pin Definition and Function

Pin No.	Name	Function
1	RF1	RF port
2	GND	Ground
3	VDD	DC Supply Voltage
4	CTL1	Control Pin 1
5	CTL2	Control Pin 2
6	GND	Ground
7	RF2	RF port
8	NC	Not Connected

Table 10: ESD robustness, System Level Test (SLT)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD SLT [1]	$V_{ESD_{SLT}}$	-8	–	+8	kV	RF1, RF2 vs system GND, with 27 nH shunt inductor

[1] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

8 Package Information

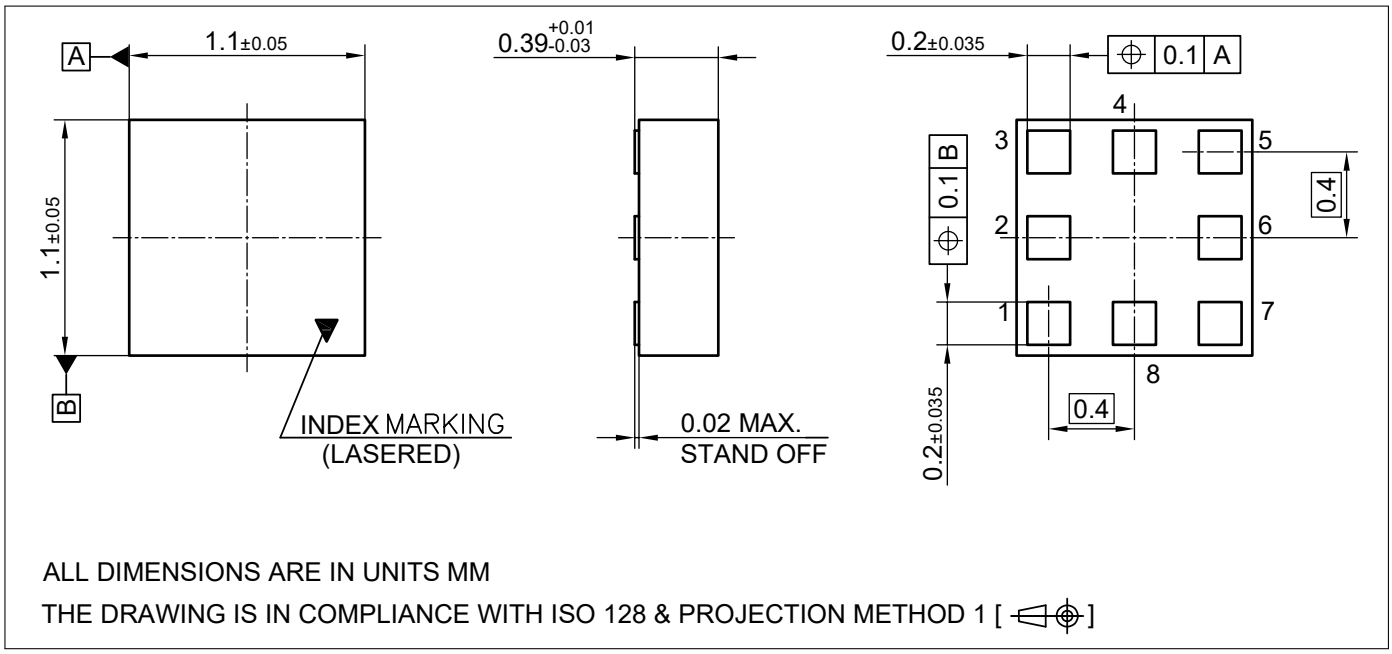

Figure 5: TSLP-8-1 Package Outline (top, side and bottom views)

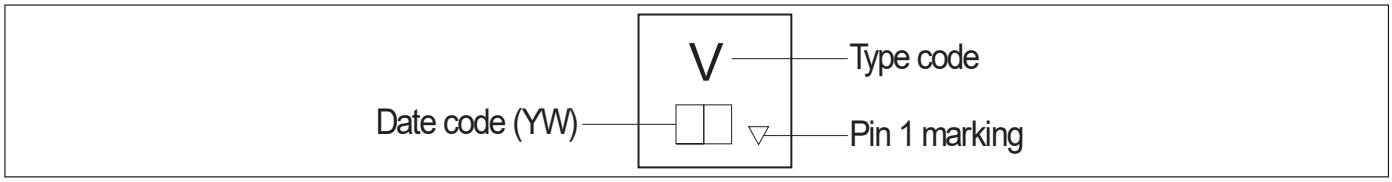

Figure 6: Marking Specification (top view): Date code digits Y and W defined in Table 11/12

Table 11: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 12: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

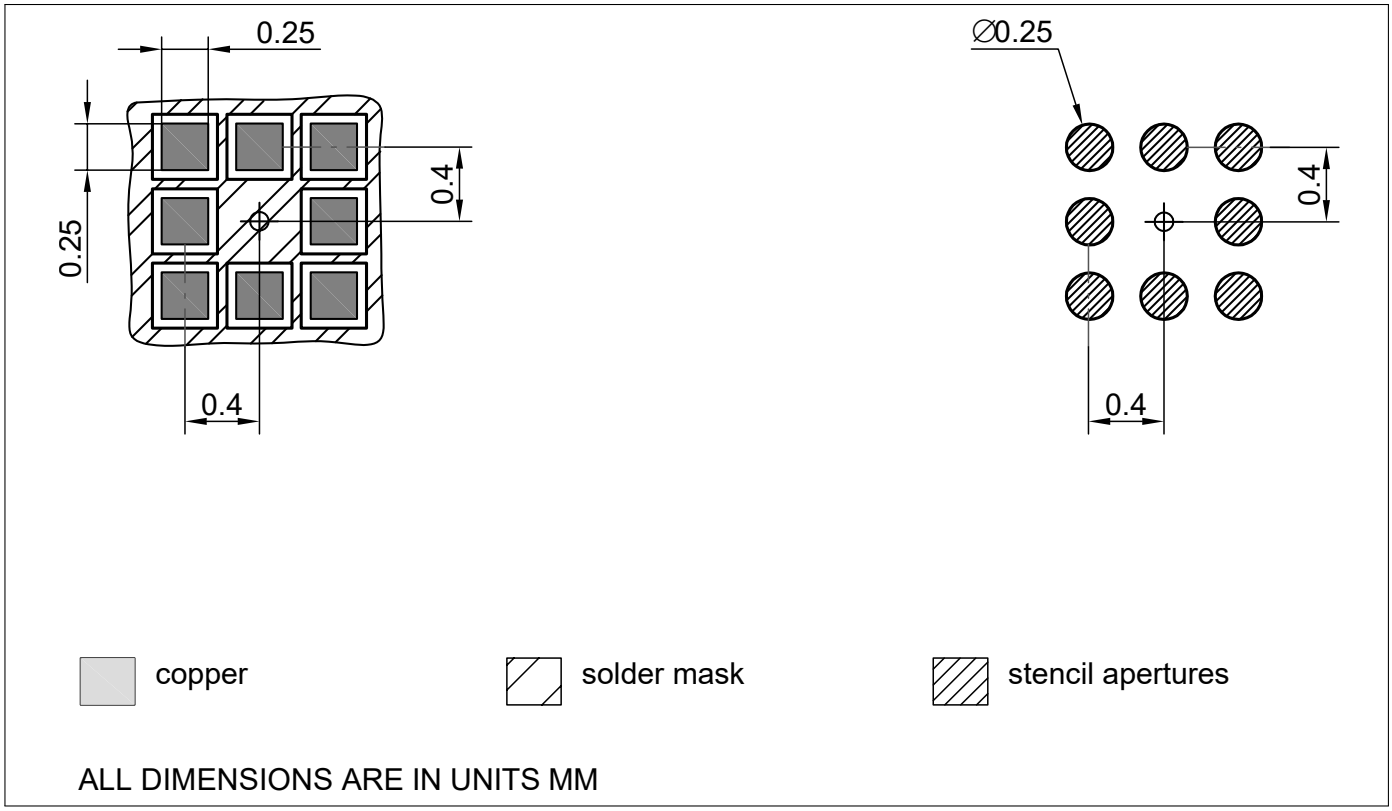

Figure 7: Footprint Recommendation

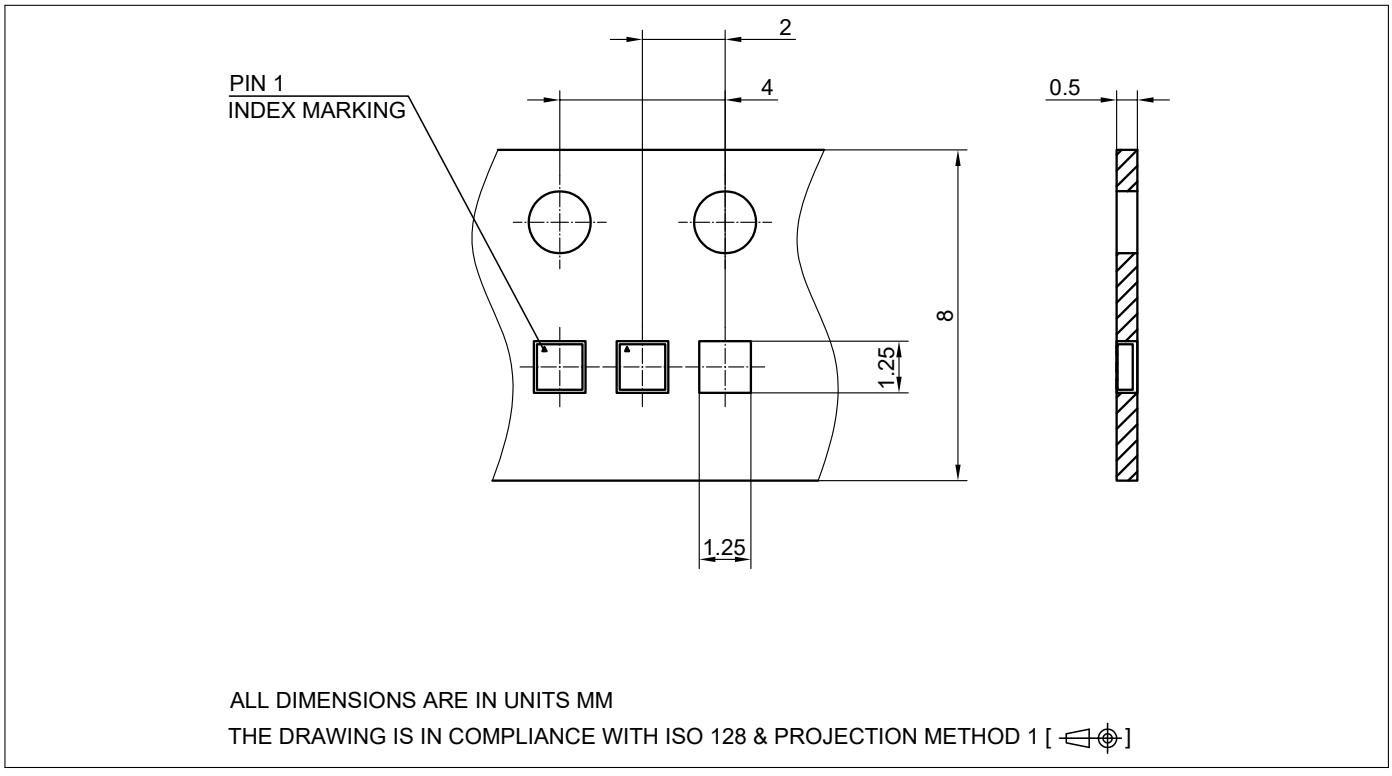

Figure 8: TSLP-8-1 Carrier Tape

Revision History	
Creation of document Revision 2.1, 2021-06-23	
Page or Item	**Subjects (major changes since previous revision)**
-	Release of the final datasheet

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Edition 2021-06-23
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
Doc_Number

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