ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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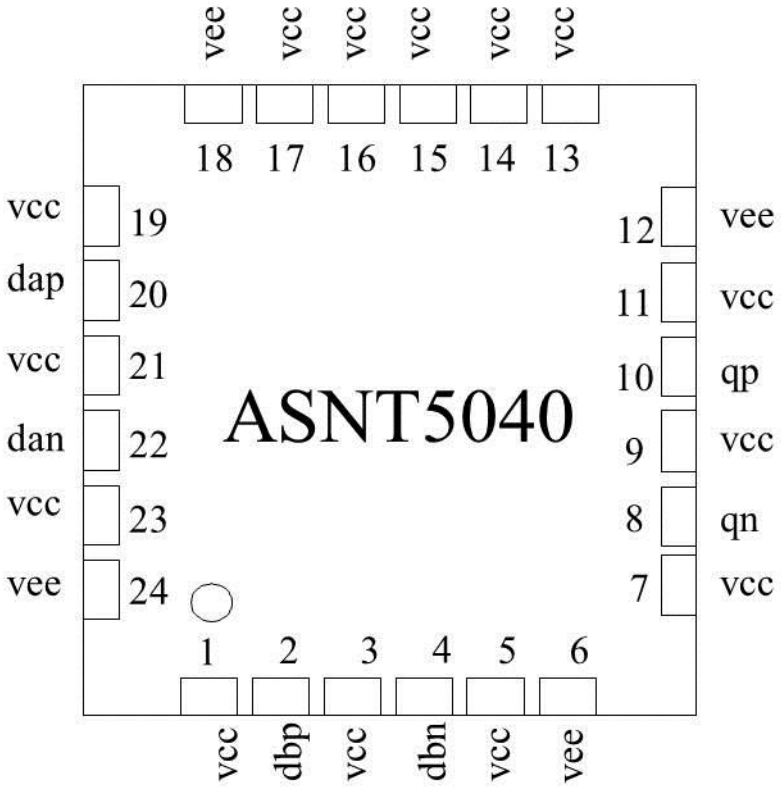
ASNT5040-PQC
DC-17*GHz* XOR Logic Gate

- High speed broadband Exclusive-OR (XOR) Boolean logic gate
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 415*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



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DESCRIPTION

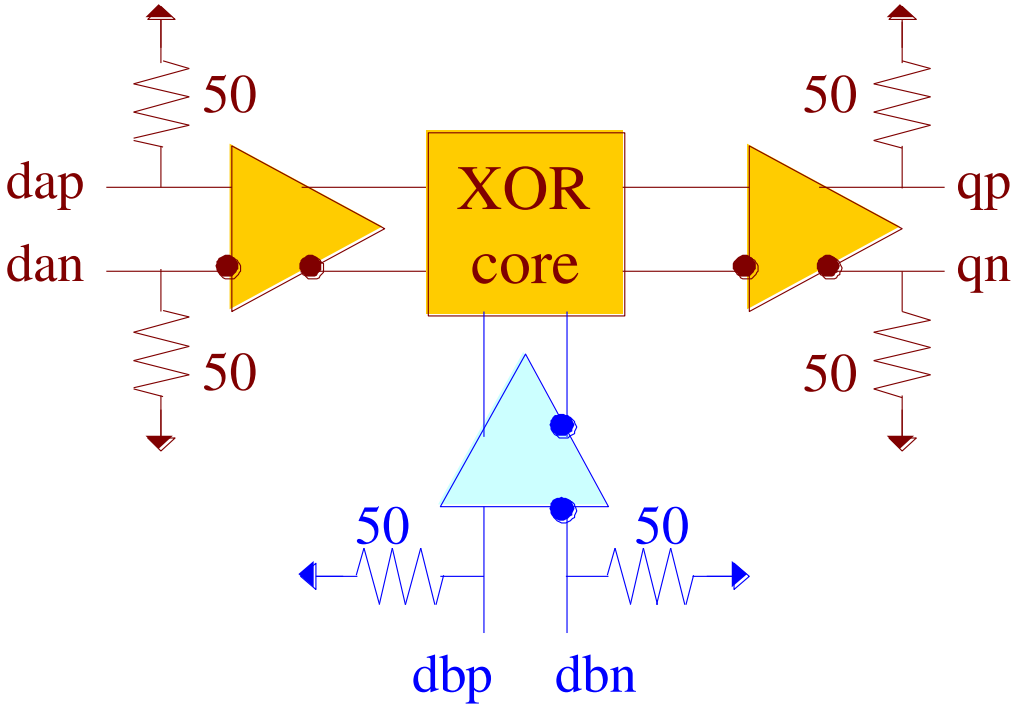

Fig. 1. Functional Block Diagram

The temperature stable ASNT5040-PQC SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can XOR a high-speed clock input signal dap/dan with another high-speed clock input signal dbp/dbn, and deliver a high-speed double frequency clock output signal qp/qn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.46	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dap	20	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc.
dan	22		
dbp	2	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc.
dbn	4		
qp	10	CML output	Differential data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc.
qn	8		
Supply and Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)		1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21, 23
vee	Negative power supply. (0*V* or -3.3*V*)		6, 12, 18, 24

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ELECTRICAL CHARACTERISTICS

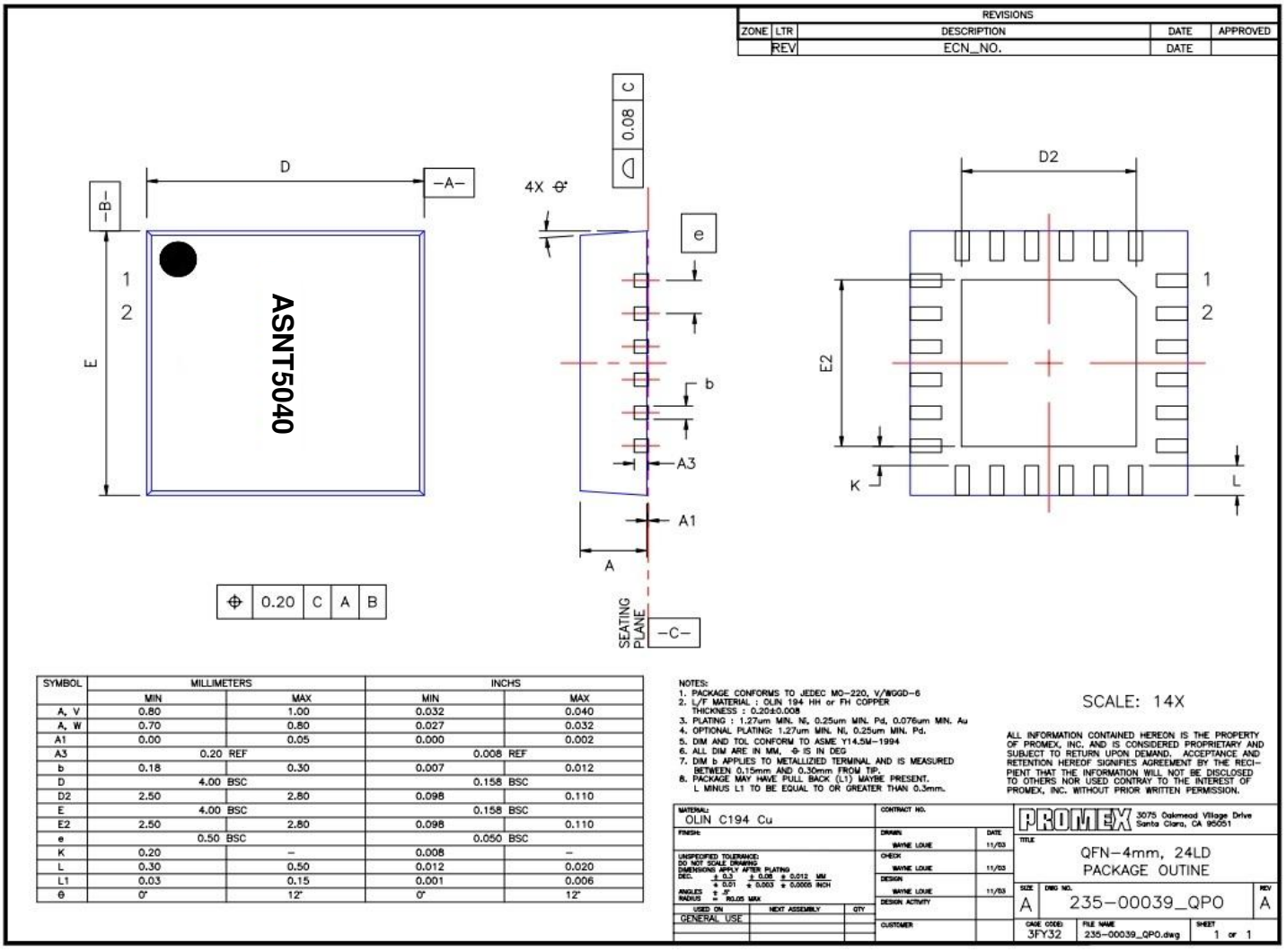
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		125		*mA*	
Power consumption		415		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (dap/dan, dbp/dbn)					
Frequency	DC		8.5	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Clock (qp/qn)					
Frequency	DC		17	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	15	17	19	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5040-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

NOTES:
1. PACKAGE CONFORMS TO JEDEC MO-220, V/WGGD-6
2. L/F MATERIAL : OLIN 194 HH or FH COPPER THICKNESS : 0.20±0.008
3. PLATING : 1.27um MIN. Ni, 0.25um MIN. Pd, 0.076um MIN. Au
4. OPTIONAL PLATING: 1.27um MIN. Ni, 0.25um MIN. Pd.
5. DIM AND TOL CONFORM TO ASME Y14.5M-1994
6. ALL DIM ARE IN MM, ⊕ IS IN DEG
7. DIM b APPLIES TO METALLIZIED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TIP.
8. PACKAGE MAY HAVE PULL BACK (L1) MAYBE PRESENT. L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.3mm.

Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
5.1.2	04-2020	Updated Package Information
5.0.2	07-2019	Updated Letterhead
5.0.1	03-2013	Corrected title Revised package pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Format correction
4.0	10-2008	Revised electrical characteristics section Revised packaging information section
3.0	06-2007	Revised electrical characteristics section
2.0	04-2007	Revised terminal functions section
1.0	01-2007	First release