MSP430F2619S-HT Mixed-Signal Microcontroller

1 Device Overview

1.1 Features

- Low-Supply Voltage Range 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 365 µA at 1 MHz, 2.2 V
  - Standby Mode (VLO): 0.5 µA
  - Off Mode (RAM Retention): 0.1 µA
- Wake-Up From Standby Mode in Less than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Four Universal Serial Communication Interfaces (USCIs)
  - USCI_A0 and USCI_A1
    - Enhanced UART Supporting Auto-Baud-Rate Detection (LIN)
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1
    - I^2C
    - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- MSP430F2619S 120KB + 256B Flash Memory, 4KB RAM
- Available in 64-Pin QFP Package or 64-Pin and 80-Pin KGD Options
- For Complete Module Descriptions, Refer to *MSP430x2xx Family User's Guide* (SLAU144).

1.2 Applications

- Supports Extreme Temperature Applications:
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability
- This device is qualified for 1000 hours of continuous operation at maximum rated temperature.
- TI high-temperature products use highly-optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

1.3 Description

The MSP430F2619S ultra-low-power microcontroller features different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430F2619S is a microcontroller configuration with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, dual 12-bit D/A converters, four universal serial communication interface (USCI) modules, DMA, and up to 64 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone RF sensor front end is another area of application.

Device Information(1)

PART NUMBER	PACKAGE	T_A
MSP430F2619SPM	QFP (PM)	–55°C to 150°C
MSP430F2619S64KGD1	KGD 64-Pin Functionality(2)	
MSP430F2619SKGD1	KGD 80-Pin Functionality(2)	

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*.
(2) KGD = Known good die.

1.4 Functional Block Diagram

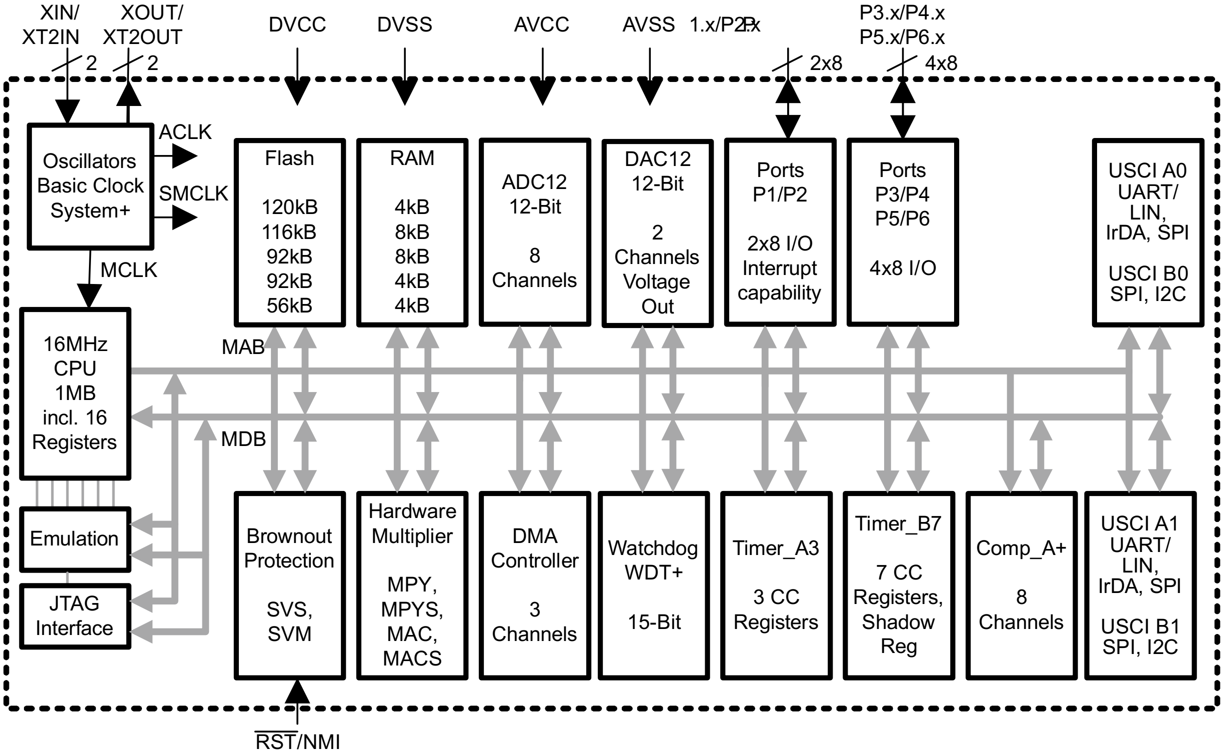


Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2013) to Revision E	Page
• Added *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	2
• Changed ORDERING INFORMATION table to *Device Information* table	2
• Added 64-pin KGD device	2
• Added new bond pad coordinates table for 80-pin KGD device	13

Changes from Revision C (April 2013) to Revision D	Page
• Added bullet under *Supports Extreme Temperature Applications*	1
• Deleted Ordering Information table note (2) referencing package information	2
• Changed *Bare Die Information* section	10

3 Terminal Configurations and Functions

3.1 Pin Diagram

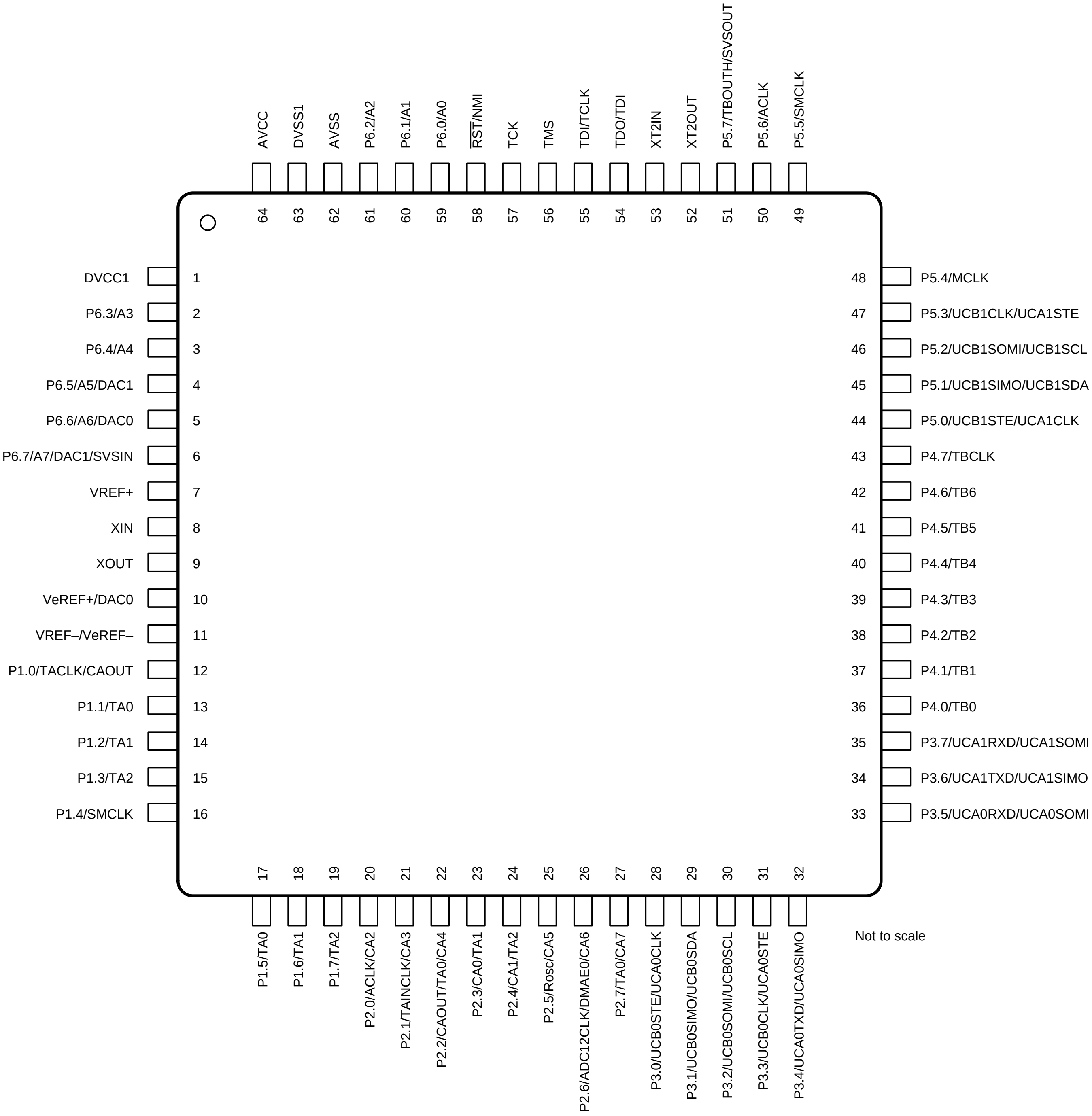


Figure 3-1. 64-Pin PM Package (Top View)

3.2 Pin Attributes

Table 3-1. Pin Attributes (64-PM Package)

PIN		I/O	DESCRIPTION
NAME	PM		
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC1}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input/Comparator_A output
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	I/O	General-purpose digital I/O pin/ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc/CA5	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input
P2.6/ADC12CLK/DMAE0/CA6	26	I/O	General-purpose digital I/O pin/conversion clock – 12-bit ADC/DMA channel 0 external trigger/Comparator_A input
P2.7/TA0/CA7	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/Comparator_A input
P3.0/UCB0STE/UCA0CLK	28	I/O	General-purpose digital I/O pin/USCI B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/UCB0SDA	29	I/O	General-purpose digital I/O pin/USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/UCB0SCL	30	I/O	General-purpose digital I/O pin/USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	31	I/O	General-purpose digital I/O/USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	32	I/O	General-purpose digital I/O pin/USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/UCA0SOMI	33	I/O	General-purpose digital I/O pin/USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/UCA1SIMO	34	I/O	General-purpose digital I/O pin/USCI A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/UCA1SOMI	35	I/O	General-purpose digital I/O pin/USCIA1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output

Table 3-1. Pin Attributes (64-PM Package) (continued)

PIN		I/O	DESCRIPTION
NAME	PM		
P4.1/TB1	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0/UCB1STE/UCA1CLK	44	I/O	General-purpose digital I/O pin/USCI B1 slave transmit enable/USCI A1 clock input/output
P5.1/UCB1SIMO/UCB1SDA	45	I/O	General-purpose digital I/O pin/USCI B1slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/UCB1SCL	46	I/O	General-purpose digital I/O pin/USCI B1slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/UCA1STE	47	I/O	General-purpose digital I/O/USCI B1 clock input/output, USCI A1 slave transmit enable
P5.4/MCLK	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance -- Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O pin/analog input A0 – 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O pin/analog input A1 – 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O pin/analog input A2 – 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O pin/analog input A3 – 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O pin/analog input A4 – 12-bit ADC
P6.5/A5/DAC1	4	I/O	General-purpose digital I/O pin/analog input A5 – 12-bit ADC/DAC12.1 output
P6.6/A6/DAC0	5	I/O	General-purpose digital I/O pin/analog input A6 – 12-bit ADC/DAC12.0 output
P6.7/A7/DAC1/SVSIN	6	I/O	General-purpose digital I/O pin/analog input a7 – 12-bit ADC/DAC12.1 output/SVS input
P7.0	NC	I/O	General-purpose digital I/O pin
P7.1	NC	I/O	General-purpose digital I/O pin
P7.2	NC	I/O	General-purpose digital I/O pin
P7.3	NC	I/O	General-purpose digital I/O pin
P7.4	NC	I/O	General-purpose digital I/O pin
P7.5	NC	I/O	General-purpose digital I/O pin
P7.6	NC	I/O	General-purpose digital I/O pin
P7.7	NC	I/O	General-purpose digital I/O pin
P8.0	NC	I/O	General-purpose digital I/O pin
P8.1	NC	I/O	General-purpose digital I/O pin
P8.2	NC	I/O	General-purpose digital I/O pin
P8.3	NC	I/O	General-purpose digital I/O pin
P8.4	NC	I/O	General-purpose digital I/O pin
P8.5	NC	I/O	General-purpose digital I/O pin

Table 3-1. Pin Attributes (64-PM Package) (continued)

PIN		I/O	DESCRIPTION
NAME	PM		
P8.6/XT2OUT	NC	O	General-purpose digital I/O pin/Output terminal of crystal oscillator XT2
P8.7/XT2IN	NC	I	General-purpose digital I/O pin/Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
XT2IN	53	I	Input port for crystal oscillator XT2
$\overline{\text{RST}}$/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices)
TCK	57	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
Ve_{REF+}/DAC0	10	I	Input for an external reference voltage/DAC12.0 output
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.

3.3 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils	Silicon with backgrind	Floating	TiN/AlCu.5%	800 nm

Table 3-2. Bond Pad Coordinates in Microns (64-Pin MSP430F2619S64KGD1)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
AVCC	1	90.65	4729.1	165.65	4804.1
DVCC1	2	90.65	4586.85	165.65	4661.85
P6.3/A3	3	87.4	4440.3	162.4	4515.3
P6.4/A4	4	87.4	4282.65	162.4	4357.65
P6.5/A5/DAC1	5	87.4	4125.05	162.4	4200.05
P6.6/A6/DAC0	6	87.4	3943.9	162.4	4018.9
P6.7/A7/DAC1/SVSIN	7	87.4	3762.75	162.4	3837.75
VREF+	8	92.95	3524.75	167.95	3599.75
XIN	9	87.4	3346.6	162.4	3421.6
XOUT	10	87.4	2472.4	162.4	2547.4
VeREF+/DAC0	11	92.95	2251	167.95	2326
VREF-/VeREF-	12	92.95	2082.5	167.95	2157.5
P1.0/TACLK/CAOUT	13	87.4	1866.2	162.4	1941.2
N/C	14	87.4	1730.6	162.4	1805.6
N/C	15	87.4	1595	162.4	1670
N/C	16	87.4	1459.4	162.4	1534.4
N/C	17	87.4	1323.8	162.4	1398.8
P1.1/TA0	18	87.4	1188.2	162.4	1263.2
P1.2/TA1	19	87.4	1052.6	162.4	1127.6
P1.3/TA2	20	87.4	807.7	162.4	882.7
P1.4/SMCLK	21	87.4	672.1	162.4	747.1
P1.5/TA0	22	559.1	87.4	634.1	162.4
P1.6/TA1	23	694.7	87.4	769.7	162.4
P1.7/TA2	24	830.3	87.4	905.3	162.4
P2.0/ACLK/CA2	25	1234.9	87.4	1309.9	162.4
P2.1/TAINCLK/CA3	26	1370.5	87.4	1445.5	162.4
P2.2/CAOUT/TA0/CA4	27	1506.1	87.4	1581.1	162.4
N/C	28	1641.7	87.4	1716.7	162.4
N/C	29	1777.3	87.4	1852.3	162.4
N/C	30	1912.9	87.4	1987.9	162.4
N/C	31	2053	87.4	2128	162.4
P2.3/CA0/TA1	32	2193.1	87.4	2268.1	162.4
P2.4/CA1/TA2	33	2328.7	87.4	2403.7	162.4
P2.5/ROSC/CA5	34	2464.3	87.4	2539.3	162.4
P2.6/ADC12CLK/DMAE0/CA6	35	2671.1	87.4	2746.1	162.4
P2.7/TA0/CA7	36	2807.15	87.4	2882.15	162.4
P3.0/UCB0STE/UCA0CLK	37	3585.9	87.4	3660.9	162.4
P3.1/UCB0SIMO/UCB0SDA	38	3721.5	87.4	3796.5	162.4
P3.2/UCB0SOMI/UCB0SCL	39	3861.6	87.4	3936.6	162.4
P3.3/UCB0CLK/UCA0STE	40	4001.7	87.4	4076.7	162.4
P3.4/UCA0TXD/UCA0SIMO	41	4137.3	87.4	4212.3	162.4
P3.5/UCA0RXD/UCA0SOMI	42	4887.6	669.65	4962.6	744.65
P3.6/UCA1TXD/UCA1SIMO	43	4887.6	805.25	4962.6	880.25
P3.7/UCA1RXD/UCA1SOMI	44	4887.6	940.85	4962.6	1015.85
N/C	45	4887.6	1076.45	4962.6	1151.45
N/C	46	4887.6	1212.05	4962.6	1287.05
P4.0/TB0	47	4887.6	1352.15	4962.6	1427.15

Table 3-2. Bond Pad Coordinates in Microns (64-Pin MSP430F2619S64KGD1) (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
P4.1/TB1	48	4887.6	1492.25	4962.6	1567.25
P4.2/TB2	49	4887.6	1627.85	4962.6	1702.85
P4.3/TB3	50	4887.6	2533.55	4962.6	2608.55
P4.4/TB4	51	4887.6	2669.15	4962.6	2744.15
P4.5/TB5	52	4887.6	2804.75	4962.6	2879.75
N/C	53	4884.35	2953.25	4959.35	3028.25
N/C	54	4887.6	3060.45	4962.6	3135.45
P4.6/TB6	55	4887.6	3153.45	4962.6	3228.45
P4.7/TBCLK	56	4887.6	3289.05	4962.6	3364.05
P5.0/UCB1STE/UCA1CLK	57	4887.6	3424.65	4962.6	3499.65
P5.1/UCB1SIMO/UCB1SDA	58	4887.6	3560.25	4962.6	3635.25
P5.2/UCB1SOMI/UCB1SCL	59	4887.6	3700.35	4962.6	3775.35
P5.3/UCB1CLK/UCA1STE	60	4887.6	3840.45	4962.6	3915.45
P5.4/MCLK	61	4887.6	3997.05	4962.6	4072.05
P5.5/SMCLK	62	4237.65	4887.6	4312.65	4962.6
P5.6/ACLK	63	4102.05	4887.6	4177.05	4962.6
P5.7/TBOUTH/SVSOUT	64	3966.45	4887.6	4041.45	4962.6
N/C	65	3830.85	4887.6	3905.85	4962.6
N/C	66	3547.7	4887.6	3622.7	4962.6
N/C	67	3412.1	4887.6	3487.1	4962.6
N/C	68	3276.5	4887.6	3351.5	4962.6
XT2OUT	69	3140.9	4887.6	3215.9	4962.6
XT2IN	70	2992.85	4887.6	3067.85	4962.6
TDO/TDI	71	2844.6	4887.6	2919.6	4962.6
TDI/TCLK	72	2448	4887.6	2523	4962.6
TMS	73	2152.25	4887.6	2227.25	4962.6
TCK	74	1568.55	4887.6	1643.55	4962.6
RST/NMI	75	1431.85	4887.6	1506.85	4962.6
P6.0/A0	76	1230.75	4887.6	1305.75	4962.6
P6.1/A1	77	1077.9	4887.6	1152.9	4962.6
P6.2/A2	78	923.95	4887.6	998.95	4962.6
AVSS	79	821.05	4887.95	896.05	4962.95
AVSS	80	674.95	4887.6	749.95	4962.6
DVSS1	81	499.2	4887.6	574.2	4962.6
AVCC	82	337.85	4884.35	412.85	4959.35

Table 3-3. Bond Pad Coordinates in Microns (80-Pin MSP430F2619SKGD1)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
AVCC	1	90.65	4729.1	165.65	4804.1
DVCC1	2	90.65	4586.85	165.65	4661.85
P6.3/A3	3	87.4	4440.3	162.4	4515.3
P6.4/A4	4	87.4	4282.65	162.4	4357.65
P6.5/A5/DAC1	5	87.4	4125.05	162.4	4200.05
P6.6/A6/DAC0	6	87.4	3943.9	162.4	4018.9
P6.7/A7/DAC1/SVSIN	7	87.4	3762.75	162.4	3837.75
VREF+	8	92.95	3524.75	167.95	3599.75
XIN	9	87.4	3346.6	162.4	3421.6
XOUT	10	87.4	2472.4	162.4	2547.4
VeREF+/DAC0	11	92.95	2251	167.95	2326
VREF-/VeREF-	12	92.95	2082.5	167.95	2157.5
P1.0/TACLK/CAOUT	13	87.4	1866.2	162.4	1941.2
P1.1/TA0	14	87.4	1730.6	162.4	1805.6
P1.2/TA1	15	87.4	1595	162.4	1670
P1.3/TA2	16	87.4	1459.4	162.4	1534.4
P1.4/SMCLK	17	87.4	1323.8	162.4	1398.8
P1.5/TA0	18	87.4	1188.2	162.4	1263.2
P1.6/TA1	19	87.4	1052.6	162.4	1127.6
P1.7/TA2	20	87.4	807.7	162.4	882.7
P2.0/ACLK/CA2	21	87.4	672.1	162.4	747.1
P2.1/TAINCLK/CA3	22	559.1	87.4	634.1	162.4
P2.2/CAOUT/TA0/CA4	23	694.7	87.4	769.7	162.4
P2.3/CA0/TA1	24	830.3	87.4	905.3	162.4
P2.4/CA1/TA2	25	1234.9	87.4	1309.9	162.4
P2.5/Rosc/CA5	26	1370.5	87.4	1445.5	162.4
P2.6/ADC12CLK/DMAE0/CA6	27	1506.1	87.4	1581.1	162.4
P2.7/TA0/CA7	28	1641.7	87.4	1716.7	162.4
P3.0/UCB0STE/UCA0CLK	29	1777.3	87.4	1852.3	162.4
P3.1/UCB0SIMO/UCB0SDA	30	1912.9	87.4	1987.9	162.4
P3.2/UCBOSOMI/UCB0SCL	31	2053	87.4	2128	162.4
P3.3/UCB0CLK/UCA0STE	32	2193.1	87.4	2268.1	162.4
P3.4/UCA0TXD/UCA0SIMO	33	2328.7	87.4	2403.7	162.4
P3.5/UCA0RXD/UCA0SOMI	34	2464.3	87.4	2539.3	162.4
P3.6/UCA1TXD/UCA1SIMO	35	2671.1	87.4	2746.1	162.4
P3.7/UCA1RXD/UCA1SOMI	36	2807.15	87.4	2882.15	162.4
P4.0/TB0	37	3585.9	87.4	3660.9	162.4
P4.1/TB1	38	3721.5	87.4	3796.5	162.4
P4.2/TB2	39	3861.6	87.4	3936.6	162.4
P4.3/TB3	40	4001.7	87.4	4076.7	162.4
P4.4/TB4	41	4137.3	87.4	4212.3	162.4
P4.5/TB5	42	4887.6	669.65	4962.6	744.65
P4.6/TB6	43	4887.6	805.25	4962.6	880.25
P4.7/TBCLK	44	4887.6	940.85	4962.6	1015.85
P5.0/UCB1STE/UCA1CLK	45	4887.6	1076.45	4962.6	1151.45
P5.1/UCB1SIMO/UCB1SDA	46	4887.6	1212.05	4962.6	1287.05
P5.2/UCB1SOMI/UCB1SCL	47	4887.6	1352.15	4962.6	1427.15

Table 3-3. Bond Pad Coordinates in Microns (80-Pin MSP430F2619SKGD1) (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
P5.3/UCB1CLK/UCA1STE	48	4887.6	1492.25	4962.6	1567.25
P5.4/MCLK	49	4887.6	1627.85	4962.6	1702.85
P5.5/SMCLK	50	4887.6	2533.55	4962.6	2608.55
P5.6/ACLK	51	4887.6	2669.15	4962.6	2744.15
P5.7/TBOUTH/SVSOUT	52	4887.6	2804.75	4962.6	2879.75
DVCC2	53	4884.35	2953.25	4959.35	3028.25
DVSS2	54	4887.6	3060.45	4962.6	3135.45
P7.0	55	4887.6	3153.45	4962.6	3228.45
P7.1	56	4887.6	3289.05	4962.6	3364.05
P7.2	57	4887.6	3424.65	4962.6	3499.65
P7.3	58	4887.6	3560.25	4962.6	3635.25
P7.4	59	4887.6	3700.35	4962.6	3775.35
P7.5	60	4887.6	3840.45	4962.6	3915.45
P7.6	61	4887.6	3997.05	4962.6	4072.05
P7.7	62	4237.65	4887.6	4312.65	4962.6
P8.0	63	4102.05	4887.6	4177.05	4962.6
P8.1	64	3966.45	4887.6	4041.45	4962.6
P8.2	65	3830.85	4887.6	3905.85	4962.6
P8.3	66	3547.7	4887.6	3622.7	4962.6
P8.4	67	3412.1	4887.6	3487.1	4962.6
P8.5	68	3276.5	4887.6	3351.5	4962.6
P8.6/XT2OUT	69	3140.9	4887.6	3215.9	4962.6
P8.7/XT2IN	70	2992.85	4887.6	3067.85	4962.6
TDO/TDI	71	2844.6	4887.6	2919.6	4962.6
TDI/TCLK	72	2448	4887.6	2523	4962.6
TMS	73	2152.25	4887.6	2227.25	4962.6
TCK	74	1568.55	4887.6	1643.55	4962.6
RST/NMI	75	1431.85	4887.6	1506.85	4962.6
P6.0/A0	76	1230.75	4887.6	1305.75	4962.6
P6.1/A1	77	1077.9	4887.6	1152.9	4962.6
P6.2/A2	78	923.95	4887.6	998.95	4962.6
AVSS	79	821.05	4887.95	896.05	4962.95
AVSS	80	674.95	4887.6	749.95	4962.6
DVSS1	81	499.2	4887.6	574.2	4962.6
AVCC	82	337.85	4884.35	412.85	4959.35

4 Specifications

4.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
	Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
	Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3	V
	Diode current at any device terminal	–2	2	mA
T_{stg}	Storage temperature (unprogrammed device(3))	–55	150	°C
	Storage temperature (programmed device(3))	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to VSS. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

4.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	±4000	V
		Charged-device model (CDM), per JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

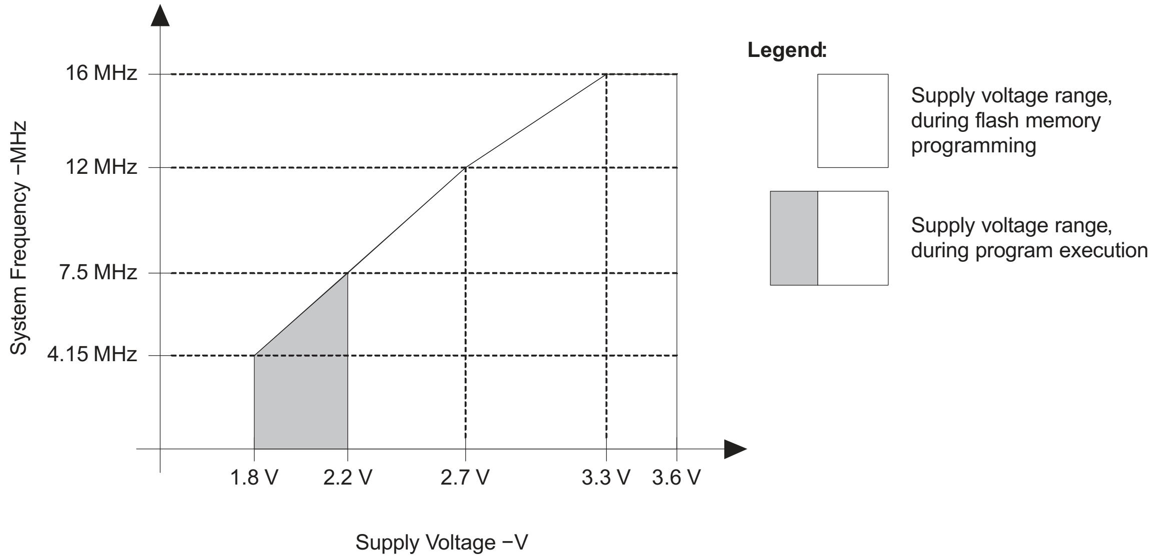
4.3 Recommended Operating Conditions(1)(2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution	$AV_{CC} = DV_{CC} = V_{CC}$(3)	1.8		3.6	V
	Supply voltage during flash memory programming		2.2		3.6	
V_{SS}	Supply voltage	$AV_{SS} = DV_{SS} = V_{SS}$		0		V
T_A	Operating free-air temperature range		–55		150	°C
	Processor frequency f_{SYSTEM} (Maximum MCLK frequency)(1)(2) (see Figure 4-1)	V_{CC} = 2.2 V, duty cycle = 50% ±10%	DC		10	MHz
		V_{CC} = 2.7 V, duty cycle = 50% ±10%	DC		12	
		$V_{CC} \geq$ 3.3 V, duty cycle = 50% ±10%	DC		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.

(2) Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.

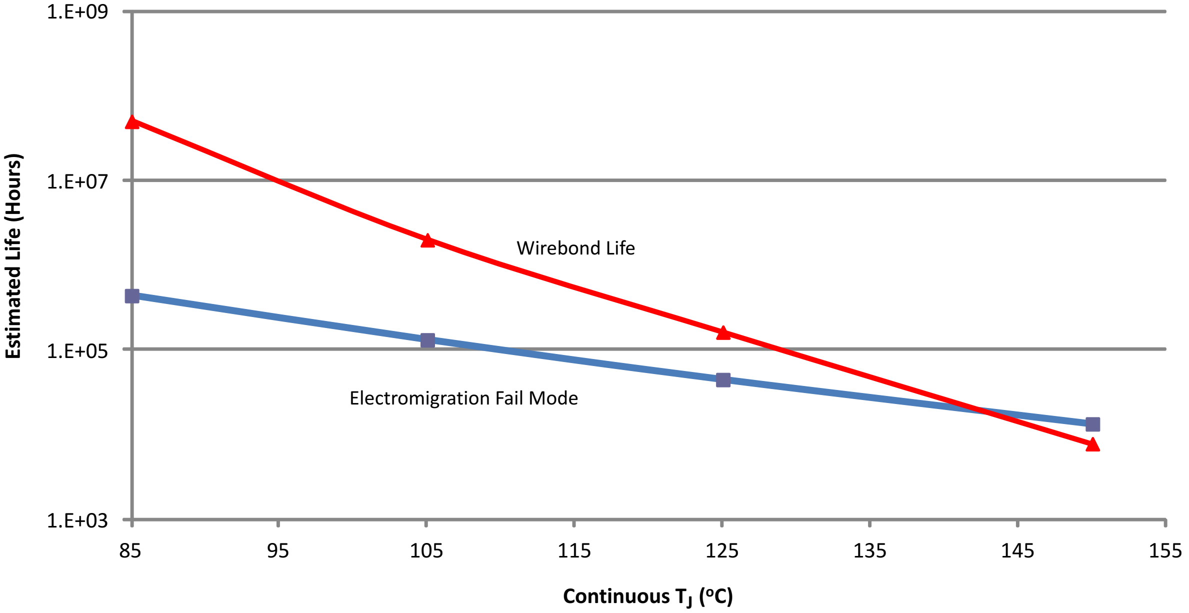
(3) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 4-1. Operating Area



(1) Wirebond Life = Time at temperature with or without bias.
(2) Electromigration Fail Mode = Time at temperature with bias.
(3) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
(4) The predicted operating lifetime vs. junction temperature is based on reliability modeling and available qualification data.

Figure 4-2. Device Life Curve

4.4 Thermal Information

THERMAL METRIC[1]		**MSP430F2619S-HT**	**UNIT**
		PM (QFP)	
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Active-Mode Supply Current Into AV_{CC} Excluding External Current – Electrical Characteristics(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNIT**
$I_{AM,\ 1MHz}$	Active-mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	T_A = –55°C to 85°C, V_{CC} = 2.2 V		365	395	µA
			T_A = 105°C, V_{CC} = 2.2 V		375	420	
			T_A = 150°C, V_{CC} = 2.2 V		640		
			T_A = –55°C to 85°C, V_{CC} = 3 V		515	560	
			T_A = 105°C, V_{CC} = 3 V		525	595	
			T_A = 150°C, V_{CC} = 3 V		700		
$I_{AM,\ 1MHz}$	Active-mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	T_A = –55°C to 85°C, V_{CC} = 2.2 V		330	370	µA
			T_A = 105°C, V_{CC} = 2.2 V		340	390	
			T_A = 150°C, V_{CC} = 2.2 V		660		
			T_A = –55°C to 85°C, V_{CC} = 3 V		460	495	
			T_A = 105°C, V_{CC} = 3 V		470	520	
			T_A = 150°C, V_{CC} = 3 V		710		
$I_{AM,\ 4kHz}$	Active-mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32,768 Hz/8 = 4,096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	T_A = –55°C to 85°C, V_{CC} = 2.2 V		2.1	9	µA
			T_A = 105°C, V_{CC} = 2.2 V		15	31	
			T_A = –55°C to 85°C, V_{CC} = 3 V		3	11	
			T_A = 105°C, V_{CC} = 3 V		19	32	
$I_{AM,\ 100kHz}$	Active-mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0,\ 0)} \cong$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	T_A = –55°C to 85°C, V_{CC} = 2.2 V		67	86	µA
			T_A = 105°C, V_{CC} = 2.2 V		80	99	
			T_A = 150°C, V_{CC} = 2.2 V		190		
			T_A = –55°C to 85°C, V_{CC} = 3 V		84	107	
			T_A = 105°C, V_{CC} = 3 V		99	128	
			T_A = 150°C, V_{CC} = 3 V		240		

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

4.6 Typical Characteristics – Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

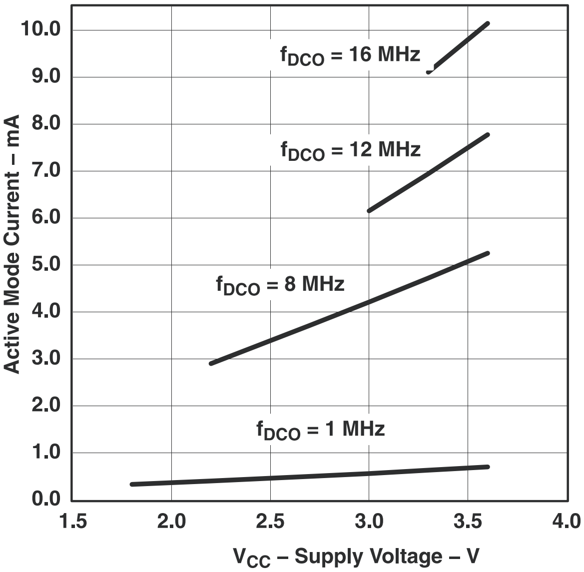


Figure 4-3. Active-Mode Current vs V_{CC}, T_A = 25°C

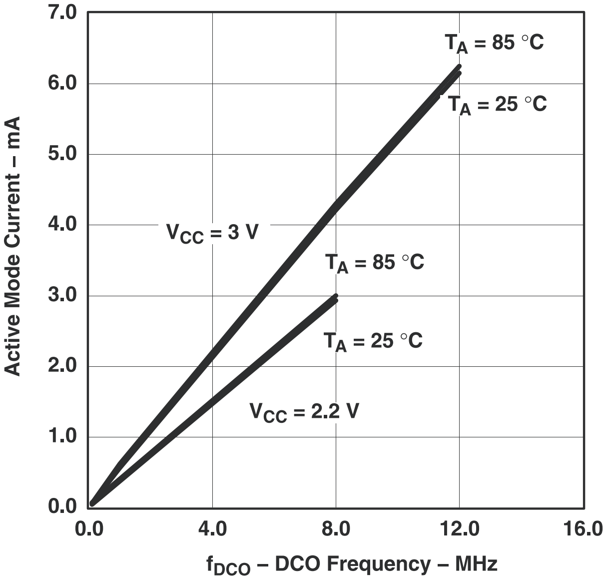


Figure 4-4. Active-Mode Current vs DCO Frequency

4.7 Active-Mode Current vs DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Active-mode current supply	$f_{SMCLK} = f_{DCO}$ = 1 MHz	T_A = –55°C, V_{CC} = 2.2 V			0.35	mA
		T_A = –40°C, V_{CC} = 2.2 V			0.30	
		T_A = 25°C, V_{CC} = 2.2 V			0.36	
		T_A = 125°C, V_{CC} = 2.2 V			0.38	
		T_A = 150°C, V_{CC} = 2.2 V			0.42	
		T_A = –55°C, V_{CC} = 3 V			0.50	
		T_A = –40°C, V_{CC} = 3 V			0.49	
		T_A = 25°C, V_{CC} = 3 V			0.51	
		T_A = 125°C, V_{CC} = 3 V			0.55	
		T_A = 150°C, V_{CC} = 3 V			0.60	
Active-mode current supply	$f_{SMCLK} = f_{DCO}$ = 12 MHz	T_A = –55°C, V_{CC} = 2.2 V			3.71	mA
		T_A = –40°C, V_{CC} = 2.2 V			3.73	
		T_A = 25°C, V_{CC} = 2.2 V			3.79	
		T_A = 125°C, V_{CC} = 2.2 V			4.45	
		T_A = 150°C, V_{CC} = 2.2 V			4.60	
		T_A = –55°C, V_{CC} = 3 V			5.47	
		T_A = –40°C, V_{CC} = 3 V			5.49	
		T_A = 25°C, V_{CC} = 3 V			5.54	
		T_A = 125°C, V_{CC} = 3 V			5.68	
		T_A = 150°C, V_{CC} = 3 V			5.77	
Active-mode current supply	$f_{SMCLK} = f_{DCO}$ = 16 MHz	T_A = –55°C, V_{CC} = 2.2 V			5.46	mA
		T_A = –40°C, V_{CC} = 2.2 V			5.58	
		T_A = 25°C, V_{CC} = 2.2 V			5.89	
		T_A = 125°C, V_{CC} = 2.2 V			6.03	
		T_A = 150°C, V_{CC} = 2.2 V			6.20	
		T_A = –55°C, V_{CC} = 3 V			7.14	
		T_A = –40°C, V_{CC} = 3 V			7.14	
		T_A = 25°C, V_{CC} = 3 V			7.21	
		T_A = 125°C, V_{CC} = 3 V			7.429	
		T_A = 150°C, V_{CC} = 3 V			7.54	

4.8 Low-Power-Mode Supply Currents Into AV_{CC} Excluding External Current – Electrical Characteristics(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{LPM0,\ 1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	T_A = –55°C to 85°C, V_{CC} = 2.2 V		68	83	µA
			T_A = 105°C, V_{CC} = 2.2 V		83	98	
			T_A = 150°C, V_{CC} = 2.2 V		210		
			T_A = –55°C to 85°C, V_{CC} = 3 V		87	105	
			T_A = 105°C, V_{CC} = 3 V		100	125	
			T_A = 150°C, V_{CC} = 3 V		240		
$I_{LPM0,\ 100kHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0,\ 0)}$ $\not\approx$ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	T_A = –55°C to 85°C, V_{CC} = 2.2 V		37	49	µA
			T_A = 105°C, V_{CC} = 2.2 V		50	62	
			T_A = 150°C, V_{CC} = 2.2 V		160		
			T_A = –55°C to 85°C, V_{CC} = 3 V		40	55	
			T_A = 105°C, V_{CC} = 3 V		57	73	
			T_A = 150°C, V_{CC} = 3 V		185		
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	T_A = –55°C to 85°C, V_{CC} = 2.2 V		23	33	µA
			T_A = 105°C, V_{CC} = 2.2 V		35	46	
			T_A = 150°C, V_{CC} = 2.2 V		148		
			T_A = –55°C to 85°C, V_{CC} = 3 V		25	36	
			T_A = 105°C, V_{CC} = 3 V		40	55	
			T_A = 150°C, V_{CC} = 3 V		168		
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	T_A = –55°C, V_{CC} = 2.2 V		0.8	1.2	µA
			T_A = 25°C, V_{CC} = 2.2 V		1	1.3	
			T_A = 85°C, V_{CC} = 2.2 V		4.6	7	
			T_A = 105°C, V_{CC} = 2.2 V		14	24	
			T_A = –55°C, V_{CC} = 3 V		0.9	1.3	
			T_A = 25°C, V_{CC} = 3 V		1.1	1.5	
			T_A = 85°C, V_{CC} = 3 V		5.5	8	
			T_A = 105°C, V_{CC} = 3 V		17	30	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	T_A = –55°C, V_{CC} = 2.2 V		0.4	1	µA
			T_A = 25°C, V_{CC} = 2.2 V		0.5	1	
			T_A = 85°C, V_{CC} = 2.2 V		4.3	6.5	
			T_A = 105°C, V_{CC} = 2.2 V		14	24	
			1T_A = 50°C, V_{CC} = 2.2 V		125		
			T_A = –55°C, V_{CC} = 3 V		0.6	1.2	
			T_A = 25°C, V_{CC} = 3 V		0.6	1.2	
			T_A = 85°C, V_{CC} = 3 V		5	7.5	
			T_A = 105°C, V_{CC} = 3 V		16.5	29.5	
			T_A = 150°C, V_{CC} = 3 V		130		

---

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.

Low-Power-Mode Supply Currents Into AV_{CC} Excluding External Current – Electrical Characteristics(1)(2) *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	$T_A = –55°C, V_{CC} = 2.2$ V		0.1	0.5	μA
			$T_A = 25°C, V_{CC} = 2.2$ V		0.1	0.5	
			$T_A = 85°C, V_{CC} = 2.2$ V		4	6	
			$T_A = 105°C, V_{CC} = 2.2$ V		13	23	
			$T_A = 150°C, V_{CC} = 2.2$ V		125		
			$T_A = –55°C, V_{CC} = 3$ V		0.2	0.5	
			$T_A = 25°C, V_{CC} = 3$ V		0.2	0.5	
			$T_A = 85°C, V_{CC} = 3$ V		4.7	7	
			$T_A = 105°C, V_{CC} = 3$ V		14	24	
			$T_A = 150°C, V_{CC} = 3$ V		146		

(5) Current for brownout included.

4.9 Typical Characteristics – LPM4 Current

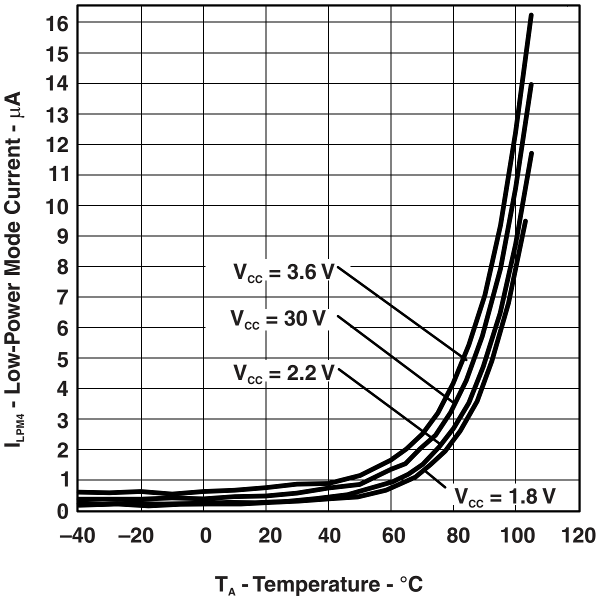


Figure 4-5. I_{LPM4} -- LPM4 Current vs Temperature

4.10 Schmitt-Trigger Inputs (Ports P1 Through P6, and $\overline{\text{RST}}$/NMI, JTAG, XIN, and XT2IN)[1] – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		0.45 x V_{CC}		0.75 x V_{CC}	V
		V_{CC} = 2.2 V	1.00		1.65	
		V_{CC} = 3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		0.25 x V_{CC}		0.55 x V_{CC}	V
		V_{CC} = 2.2 V	0.55		1.20	
		V_{CC} = 3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})	V_{CC} = 2.2 V	0.2		1	V
		V_{CC} = 3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS} For pulldown: V_{IN} = V_{CC}	20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}		5		pF

(1) XIN and XT2IN in bypass mode only.

4.11 Inputs (Ports P1 and P2) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag[1], V_{CC} = 2.2 V or 3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

4.12 Leakage Current (Ports P1 Through P6) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	See [1] and [2], V_{CC} = 2.2 V or 3 V		±250		nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

4.13 Standard Inputs - $\overline{\text{RST}}$/NMI – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V or 3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.2 V or 3 V	0.8 x V_{CC}	V_{CC}	V

4.14 Outputs (Ports P1 Through P6) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)} = –1.5$ mA(1), $V_{CC} = 2.2$ V	$V_{CC} – 0.25$	V_{CC}	V
		$I_{OH(max)} = –6$ mA(2), $V_{CC} = 2.2$ V	$V_{CC} – 0.6$	V_{CC}	
		$I_{OH(max)} = –1.5$ mA(1), $V_{CC} = 3$ V	$V_{CC} – 0.25$	V_{CC}	
		$I_{OH(max)} = –6$ mA(2), $V_{CC} = 3$ V	$V_{CC} – 0.6$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)} = 1.5$ mA(1), $V_{CC} = 2.2$ V	V_{SS}	V_{SS}+0.25	V
		$I_{OL(max)} = 6$ mA(2), $V_{CC} = 2.2$ V	V_{SS}	V_{SS}+0.6	
		$I_{OL(max)} = 1.5$ mA(1), $V_{CC} = 3$ V	V_{SS}	V_{SS}+0.25	
		$I_{OL(max)} = 6$ mA(2), $V_{CC} = 3$ V	V_{SS}	V_{SS}+0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

4.15 Output Frequency (Ports P1 Through P6) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, $C_L = 20$ pF, $R_L = 1$ kΩ(1)(2)	$V_{CC} = 2.2$ V	DC		10	MHz
			$V_{CC} = 3$ V	DC		12	
f_{Port_CLK}	Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, $C_L = 20$ pF(2)	$V_{CC} = 2.2$ V	DC		12	MHz
			$V_{CC} = 3$ V	DC		16	
$t_{(Xdc)}$	Duty cycle of output frequency	P5.6/ACLK, $C_L = 20$ pF, LF mode		30%	50%	70%	
		P5.6/ACLK, $C_L = 20$ pF, XT1 mode		40%	50%	60%	
		P5.4/MCLK, $C_L = 20$ pF, XT1 mode		40%		60%	
		P5.4/MCLK, $C_L = 20$ pF, DCO		50% – 15 ns	50%	50% + 15 ns	
		P1.4/SMCLK, $C_L = 20$ pF, XT2 mode		40%		60%	
		P1.4/SMCLK, $C_L = 20$ pF, DCO		50% – 15 ns		50% + 15 ns	

(1) A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

4.16 Typical Characteristics – Outputs

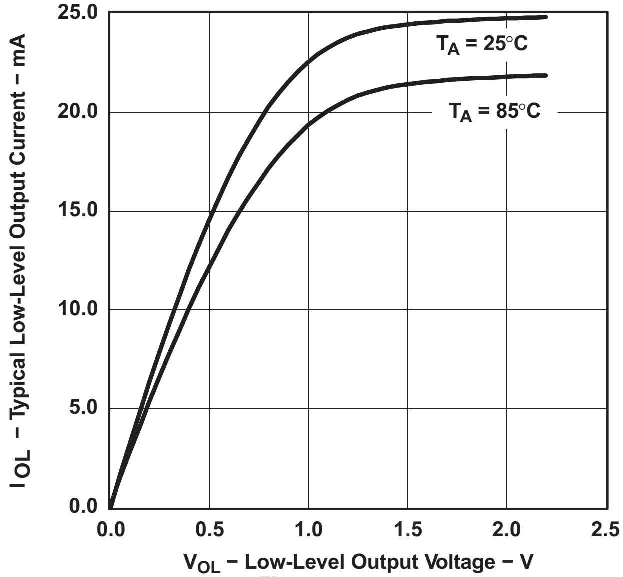


Figure 4-6.

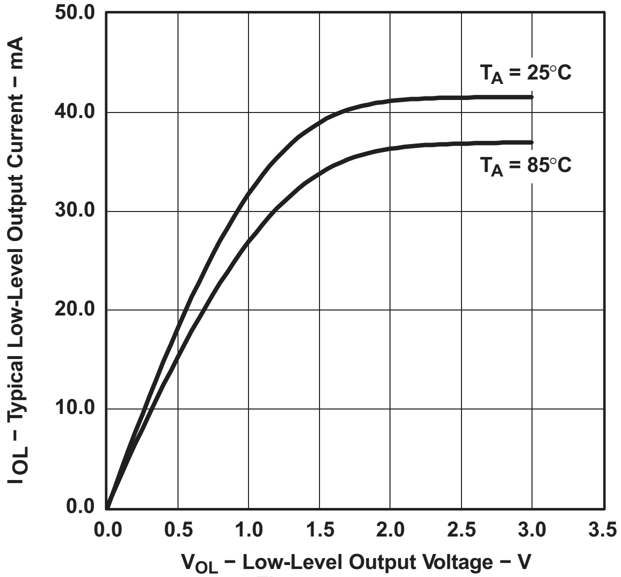


Figure 4-7.

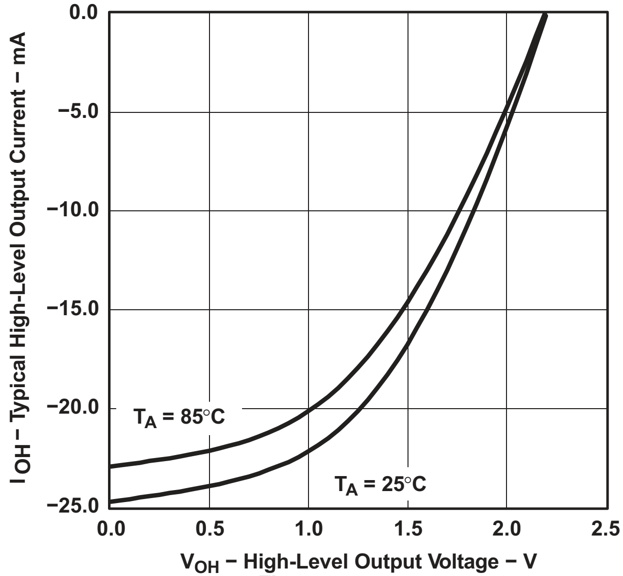


Figure 4-8.

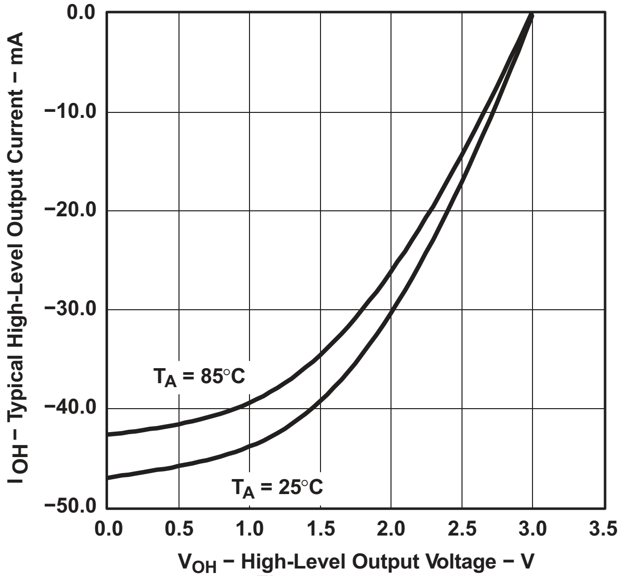


Figure 4-9.

4.17 POR/Brownout Reset (BOR) – Electrical Characteristics(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 4-10	$dV_{CC}/dt \leq 3$ V/s		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 4-10 through Figure 4-12	$dV_{CC}/dt \leq 3$ V/s			1.71	V
$V_{hys(B\_IT-)}$	See Figure 4-10	$dV_{CC}/dt \leq 3$ V/s	70	130	210	mV
$t_{d(BOR)}$	See Figure 4-10				2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally	V_{CC} = 2.2 V or 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

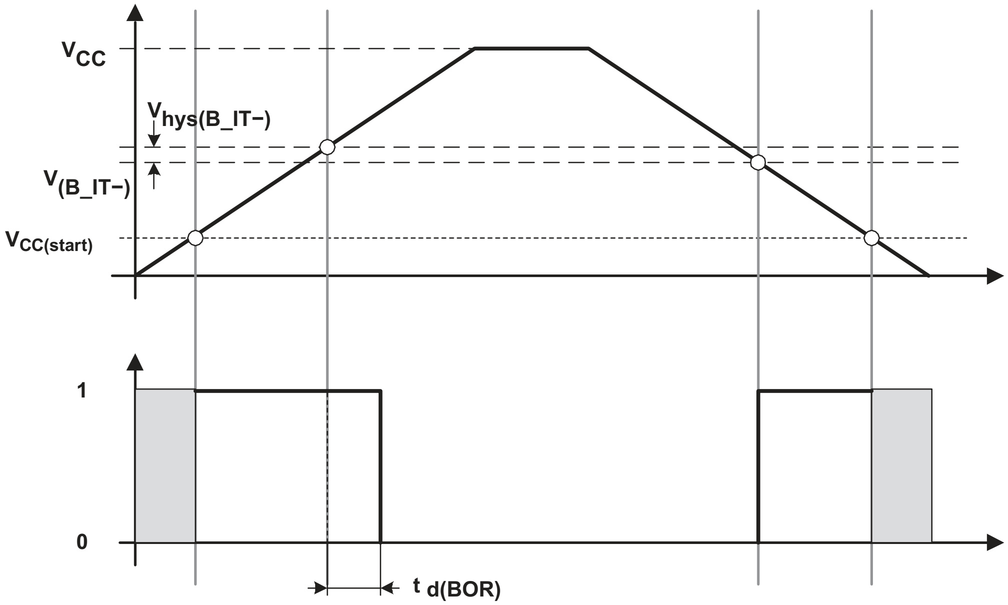


Figure 4-10. POR/Brownout Reset (BOR) vs Supply Voltage

4.18 Typical Characteristics - POR/Brownout Reset (BOR)

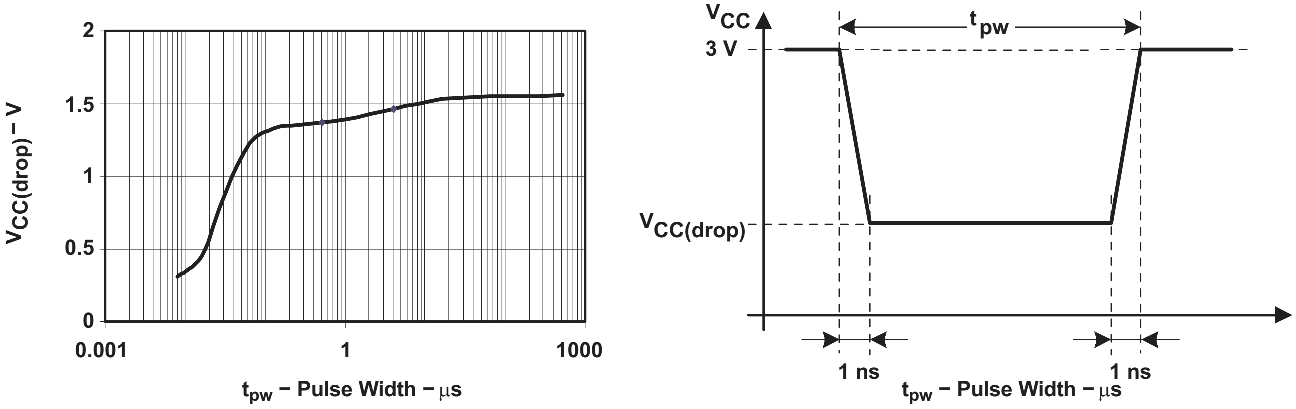


Figure 4-11. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

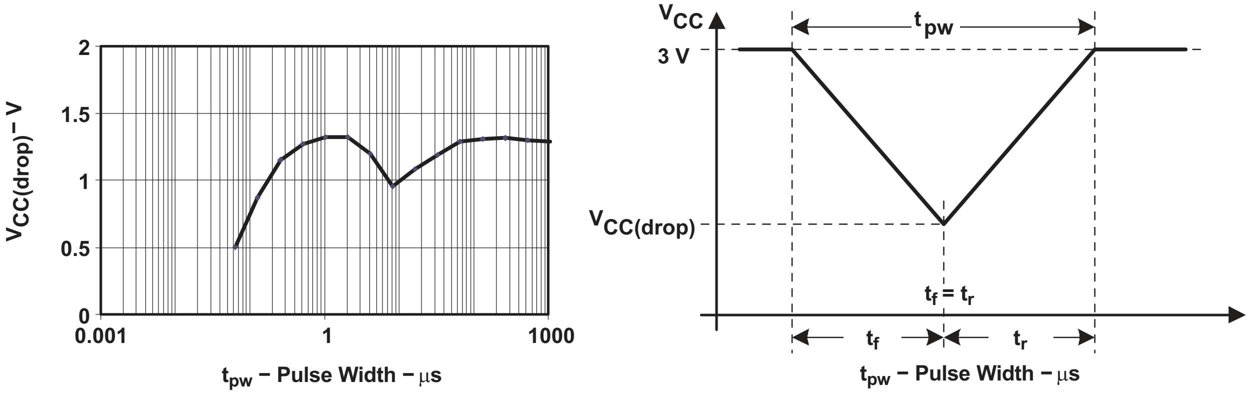


Figure 4-12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

4.19 SVS (Supply Voltage Supervisor/Monitor) - Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 4-13)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	
$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, $V_{CC} = 3$ V		20	150		µs
t_{settle}	VLD ≠ 0 (see (1))				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 4-13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 4-13)	VLD = 1	70	120	210	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)} \times 0.004$		$V_{(SVS\_IT-)} \times 0.016$	V
	$V_{CC}/dt \le 3$ V/s (see Figure 4-13), External voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 4-13 and Figure 4-14)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (2)	
		VLD = 13	3.24	3.5	3.76 (2)	
		VLD = 14	3.43	3.7 (2)	3.99 (2)	
	$V_{CC}/dt \le 3$ V/s (see Figure 4-13 and Figure 4-14), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, $V_{CC} = 2.2$ V/3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value between 2 and 15. The overdrive is assumed to be > 50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

4.20 Typical Characteristics - SVS

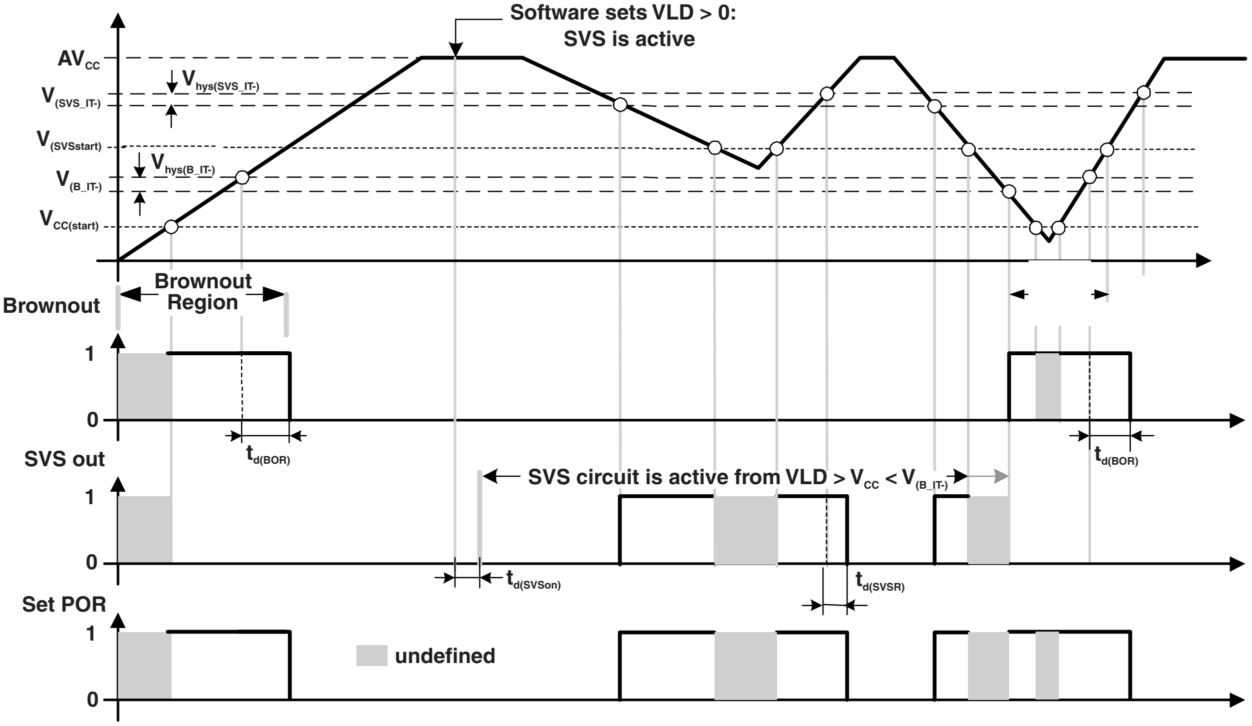


Figure 4-13. SVS Reset (SVSR) vs Supply Voltage

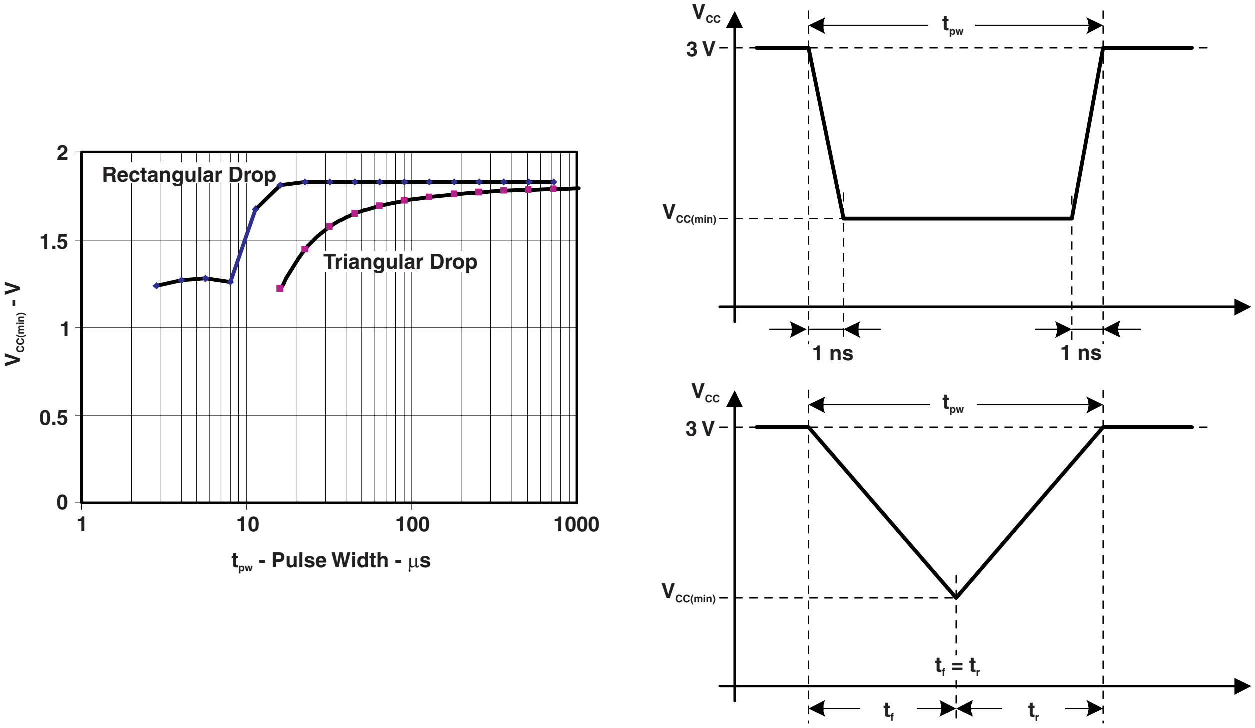


Figure 4-14. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

4.21 Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO} + 1)}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO} + 1)} \tag{1}$$

4.22 DCO Frequency – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14	1.8		3.6	V
		RSELx = 14	2.2		3.6	
		RSELx = 15	3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0, V_{CC} = 2.2 V or 3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	4.30		7.30	M Hz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0, V_{CC} = 2.2 V or 3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$, V_{CC} = 2.2 V or 3 V			1.55	ratio

DCO Frequency – Electrical Characteristics *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$, V_{CC} = 2.2 V or 3 V	1.05	1.08	1.12	ratio
Duty cycle		Measured at P1.4/SMCLK, V_{CC} = 2.2 V or 3 V	40%	50%	60%	

4.23 Calibrated DCO Frequencies (Tolerance at Calibration) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration		T_A = 25°C, V_{CC} = 3 V	–1%	±0.2%	1%	
$f_{CAL(1\ MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms T_A = 25°C, V_{CC} = 3 V	0.990	1	1.010	MHz
$f_{CAL(8\ MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms T_A = 25°C, V_{CC} = 3 V	7.920	8	8.080	MHz
$f_{CAL(12\ MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms T_A = 25°C, V_{CC} = 3 V	11.88	12	12.12	MHz
$f_{CAL(16\ MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms T_A = 25°C, V_{CC} = 3 V	15.84	16	16.16	MHz

4.24 Calibrated DCO Frequencies (Tolerance Over Temperature) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature		T_A = 0°C to 85°C, V_{CC} = 3 V		–2.5%	±0.5%	2.5%	
8-MHz tolerance over temperature		T_A = 0°C to 85°C, V_{CC} = 3 V		–2.5%	±1.0%	2.5%	
12-MHz tolerance over temperature		T_A = 0°C to 85°C, V_{CC} = 3 V		–2.5%	±1.0%	2.5%	
16-MHz tolerance over temperature		T_A = 0°C to 85°C, V_{CC} = 3 V		–3.0%	±2.0%	3.0%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms T_A = 0°C to 85°C	V_{CC} = 2.2 V	0.970	1	1.030	MHz
			V_{CC} = 3 V	0.975	1	1.025	
			V_{CC} = 3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms T_A = 0°C to 85°C	V_{CC} = 2.2 V	7.760	8	8.400	MHz
			V_{CC} = 3 V	7.800	8	8.200	
			V_{CC} = 3.6 V	7.600	8	8.240	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms T_A = 0°C to 85°C	V_{CC} = 2.2 V	11.70	12	12.30	MHz
			V_{CC} = 3 V	11.70	12	12.30	
			V_{CC} = 3.6 V	11.70	12	12.30	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms T_A = 0°C to 85°C	V_{CC} = 3 V	15.52	16	16.48	MHz
			V_{CC} = 3.6 V	15.00	16	16.48	

4.25 Calibrated DCO Frequencies (Tolerance Over Supply Voltage V_{CC}) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}		T_A = 25°C, V_{CC} = 1.8 V to 3.6 V	–3%	±2%	3%	
8-MHz tolerance overV_{CC}		T_A = 25°C, V_{CC} = 1.8 V to 3.6 V	–3%	±2%	3%	
12-MHz tolerance over V_{CC}		T_A = 25°C, V_{CC} = 2.2 V to 3.6 V	–3%	±2%	3%	
16-MHz tolerance over V_{CC}		T_A = 25°C, V_{CC} = 3 V to 3.6 V	–6%	±2%	3%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms, T_A = 25°C, V_{CC} = 1.8 V to 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms, T_A = 25°C, V_{CC} = 1.8 V to 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms, T_A = 25°C, V_{CC} = 2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms, T_A = 25°C, V_{CC} = 3 V to 3.6 V	15.00	16	16.48	MHz

4.26 Calibrated DCO Frequencies (Overall Tolerance) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature		T_A = –55°C to 150°C, V_{CC} = 1.8 V to 3.6 V	–5%	±2%	5%	
8-MHz tolerance over temperature		T_A = –55°C to 150°C, V_{CC} = 1.8 V to 3.6 V	–5%	±2%	5%	
12-MHz tolerance over temperature		T_A = –55°C to 150°C, V_{CC} = 2.2 V to 3.6 V	–5%	±2%	5%	
16-MHz tolerance over temperature		T_A = –55°C to 150°C, V_{CC} = 3 V to 3.6 V	–6%	±3%	6%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms, T_A = –55°C to 150°C, V_{CC} = 1.8 V to 3.6 V	.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms, T_A = –55°C to 150°C, V_{CC} = 1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms, T_A = –55°C to 150°C, V_{CC} = 2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms, T_A = –55°C to 150°C, V_{CC} = 3 V to 3.6 V	15.00	16	17.00	MHz

4.27 Typical Characteristics – Calibrated DCO Frequency

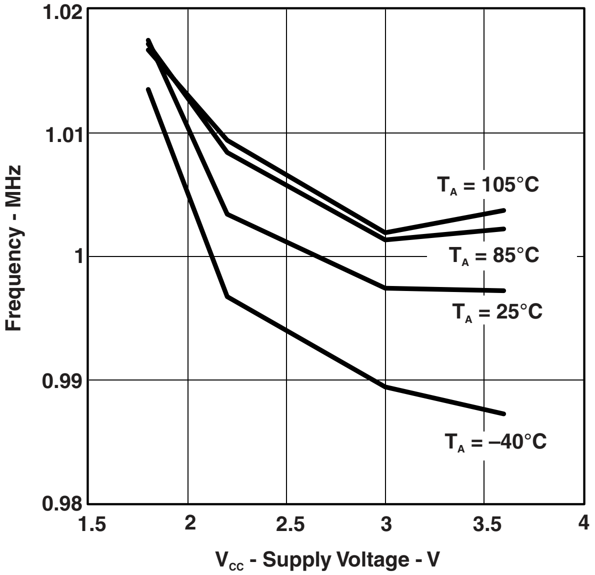


Figure 4-15. Calibrated 1-MHz DCO Frequency vs V_{CC}

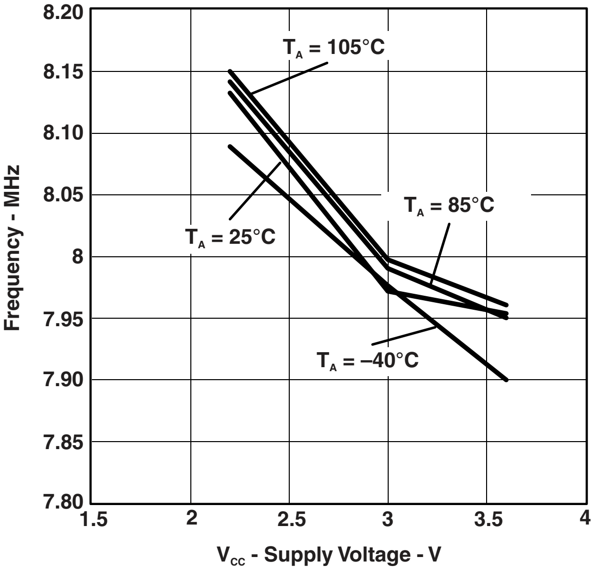


Figure 4-16. Calibrated 8-MHz DCO Frequency vs V_{CC}

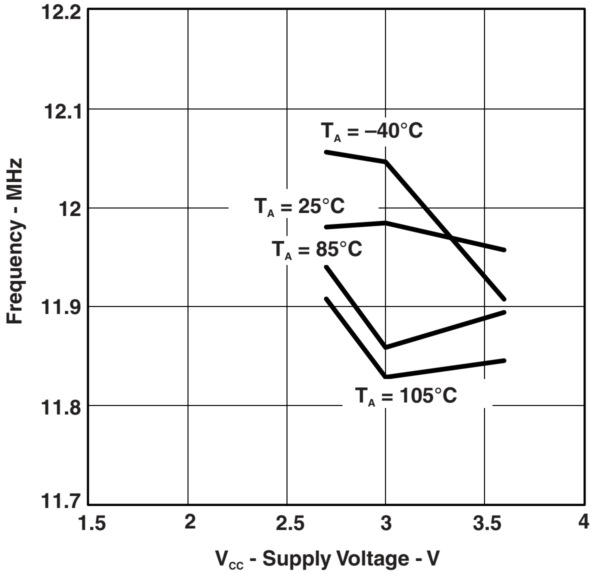


Figure 4-17. Calibrated 12-MHz DCO Frequency vs V_{CC}

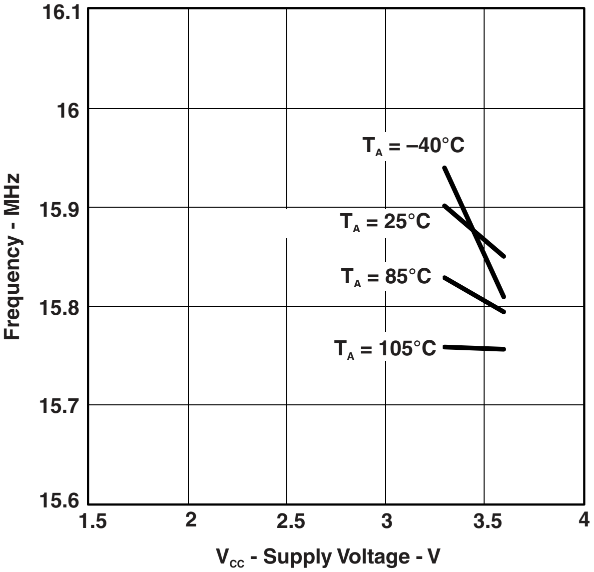


Figure 4-18. Calibrated 16-MHz DCO Frequency vs V_{CC}

4.28 Wake-Up From Low-Power Modes (LPM3/4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 [1]	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, V_{CC} = 2.2 V or 3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, V_{CC} = 2.2 V or 3 V			1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, V_{CC} = 3 V			1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, V_{CC} = 3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 [2]				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$	

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

4.29 Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

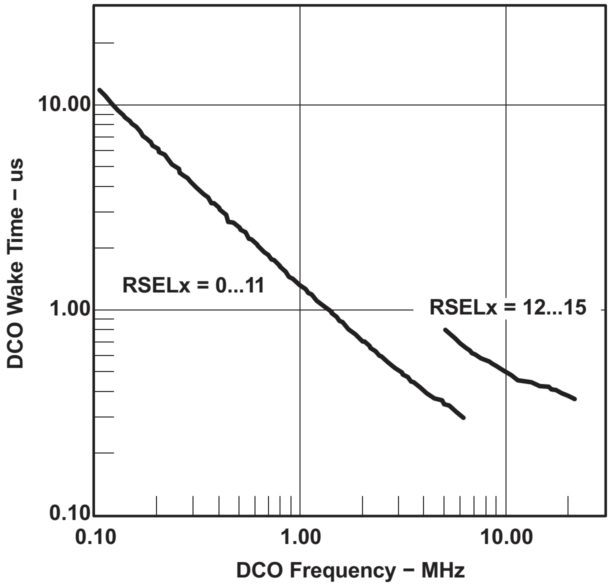


Figure 4-19. Clock Wake-Up Time From LPM3 vs DCO Frequency

4.30 DCO With External Resistor R_{OSC} – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	V_{CC} = 2.2 V	1.8	MHz
			V_{CC} = 3 V	1.95	
D_t	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V		±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, V_{CC} = 2.2 V or 3 V		10	%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50 ppm/°C

4.31 Typical Characteristics - DCO With External Resistor R_{OSC}

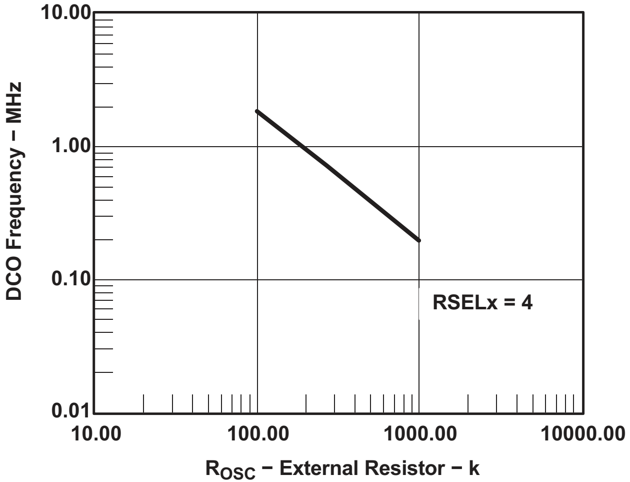


Figure 4-20. DCO Frequency vs R_{OSC}, V_{CC} = 2.2 V, T_A = 25°C

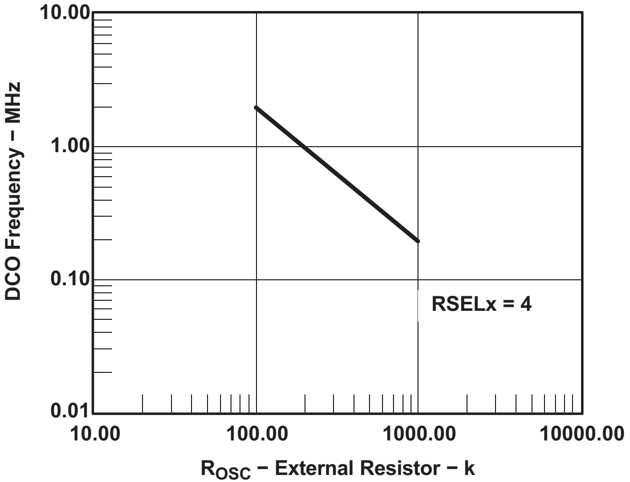


Figure 4-21. DCO Frequency vs R_{OSC}, V_{CC} = 3.0 V, T_A = 25°C

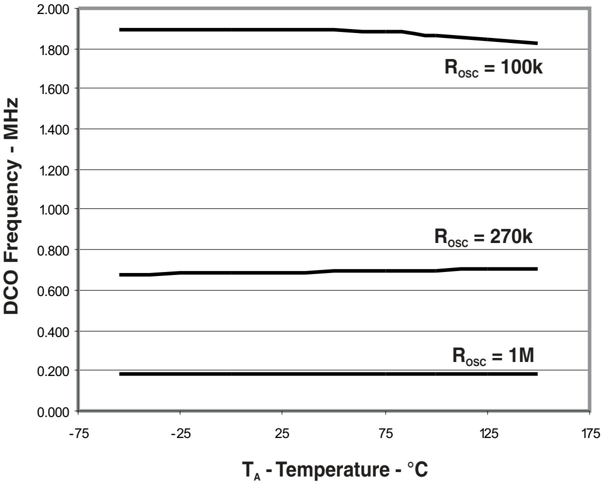


Figure 4-22. DCO Frequency vs Temperature, V_{CC} = 3.0 V

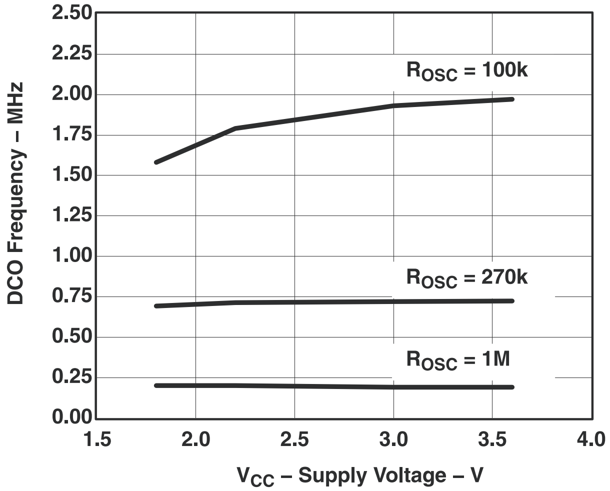


Figure 4-23. DCO Frequency vs V_{CC}, T_A = 25°C

4.32 Crystal Oscillator (LFXT1) Low-Frequency Modes – Electrical Characteristics(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1, V_{CC} = 1.8 V to 3.6 V			32,768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, V_{CC} = 1.8 V to 3.6 V		10,000	32,768	50,000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0;$f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(3)	XTS = 0	XCAPx = 0		1		pF
			XCAPx = 1		5.5		
			XCAPx = 2		8.5		
			XCAPx = 3		11		
Duty cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz, V_{CC} = 2.2 V or 3 V		30%	50%	70%	
$f_{Fault,LF}$	Oscillator fault frequency threshold, LF mode (4)	XTS = 0, LFXT1Sx = 3(5), V_{CC} = 2.2 V or 3 V		10		10,000	Hz

(1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
- Keep as short of a trace as possible between the device and the crystal.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) LFXT1 in 32-KHz mode is specified to function only between –55°C to 105°C. This module is know to fail above 110°C. For further info contact TI support.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

4.33 Internal Very-Low-Power, Low-Frequency Oscillator (VLO) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	T_A = –55°C to 85°C, V_{CC} = 2.2 V or 3 V	4	12	20	kHz
		T_A = 150°C, V_{CC} = 2.2 V or 3 V			22	
df_{VLO}/dT	VLO frequency temperature drift	See (1), V_{CC} = 2.2 V or 3 V		0.5	0.8	%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	See (2), T_A = 25°C, V_{CC} = 1.8 V to 3.6V		4		%/V

(1) Calculated using the box method:
S Version: (MAX(–55 to 150°C) – MIN(–55 to 150°C))/MIN(–55 to 150°C)/(150°C – (–55°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8V to 3.6 V))/MIN(1.8 V to 3.6 V)/(3.6 V – 1.8 V)

4.34 Crystal Oscillator (LFXT1) High Frequency Modes – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, V_{CC} = 1.8 V to 3.6 V		0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator lcrystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, V_{CC} = 1.8 V to 3.6 V		1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	V_{CC} = 1.8 V to 3.6 V	2		10	MHz
			V_{CC} = 2.2 V to 3.6 V	2		12	
			V_{CC} = 3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	V_{CC} = 1.8 V to 3.6 V	0.4		10	MHz
			V_{CC} = 2.2 V to 3.6 V	0.4		12	
			V_{CC} = 3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 4-24 and Figure 4-25)	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XTS = 1(3)			1		pF
Duty cycle	HF mode	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz, V_{CC} = 3 V		40%	50%	60%	
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz, V_{CC} = 3 V		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode(4)	XTS = 1, LFXT1Sx = 3(5), V_{CC} = 2.2 V or 3 V		30		300	kHz

(1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
- Keep as short of a trace as possible between the device and the crystal.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals

4.35 Typical Characteristics – LFXT1 Oscillator in HF Mode (XTS = 1)

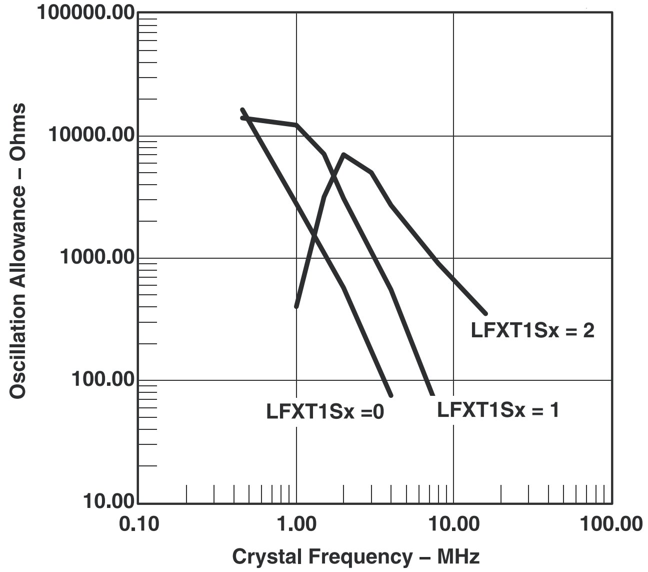


Figure 4-24. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

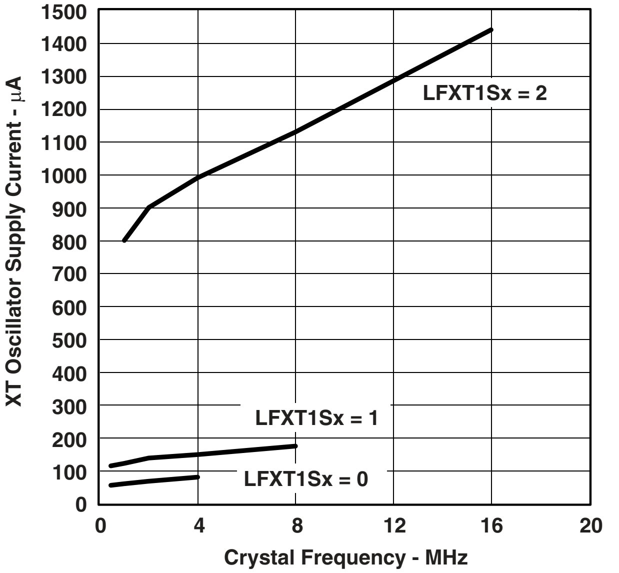


Figure 4-25. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

4.36 Crystal Oscillator (XT2) – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0, V_{CC} = 1.8 V to 3.6 V		0.4		0.9	MHz
f_{XT2}	XT2 oscillator lcrystal frequency, mode 1	XT2Sx = 1, V_{CC} = 1.8 V to 3.6 V		1		4	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	V_{CC} = 1.8 V to 3.6 V	2		10	MHz
			V_{CC} = 2.2 V to 3.6 V	2		12	
			V_{CC} = 3 V to 3.6 V	2		16	
f_{XT2}	XT2 oscillator logic-level square-wave input frequency,	XT2Sx = 3	V_{CC} = 1.8 V to 3.6 V	0.4		10	MHz
			V_{CC} = 2.2 V to 3.6 V	0.4		12	
			V_{CC} = 3 V to 3.6 V	0.4		16	
OA	Oscillation allowance (see Figure 4-26 and Figure 4-27)	XT2Sx = 0, f_{XT2} = 1 MHz; $C_{L,eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, f_{XT2} = 4MHz; $C_{L,eff}$ = 15 pF			800		
		XT2Sx = 2, $f_{XT1, HF}$ = 16 MHz; $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	See (3)			1		pF
Duty cycle	HF mode	Measured at P1.4/SMCLK, f_{XT2} = 10 MHz, V_{CC} = 2.2 V or 3 V		40%	50%	60%	
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz, V_{CC} = 2.2 V or 3 V		40%	50%	60%	
f_{Fault}	Oscillator fault frequency, HF mode(4)	XT2Sx = 3(5), V_{CC} = 2.2 V or 3 V		30		300	kHz

(1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
- Keep as short of a trace as possible between the device and the crystal.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

4.37 Typical Characteristics – XT2 Oscillator

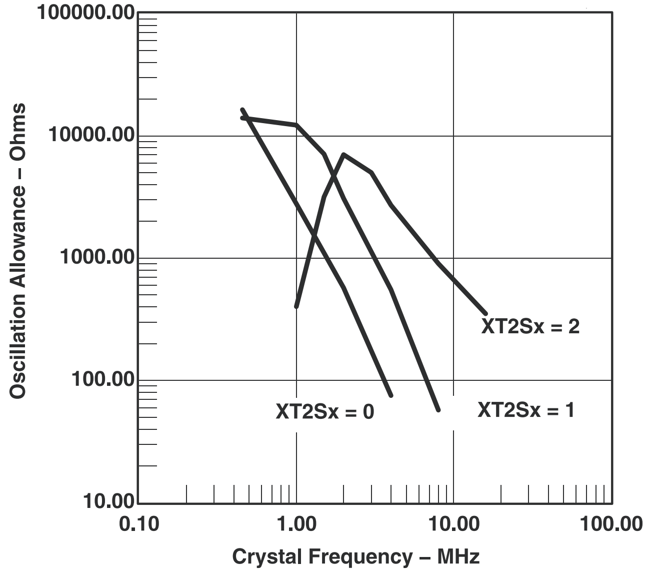


Figure 4-26. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

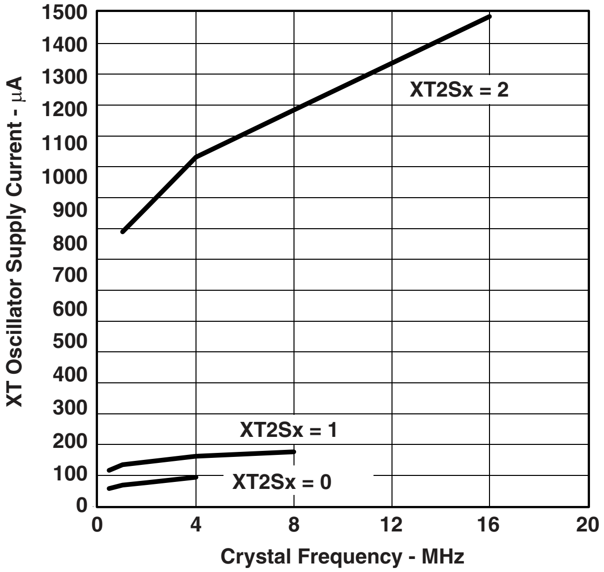


Figure 4-27. XT2 Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

4.38 Timer_A – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	V_{CC} = 2.2 V		10	MHz
			V_{CC} = 3 V		16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2, V_{CC} = 2.2 V or 3 V		20		ns

4.39 Timer_B – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	V_{CC} = 2.2 V		10	MHz
			V_{CC} = 3 V		16	
$t_{TB,cap}$	Timer_B, capture timing	TB0, TB1, TB2, V_{CC} = 2.2 V or 3 V		20		ns

4.40 USCI (UART Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK; Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)	V_{CC} = 2.2 V or 3 V			1	MHz
t_τ	UART receive deglitch time(1)	V_{CC} = 2.2 V	50	150	600	ns
		V_{CC} = 3 V	50	150	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

4.41 USCI (SPI Master Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see Figure 4-28 and Figure 4-29)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	V_{CC}= 2.2 V		110		ns
		V_{CC} = 3 V		75		
$t_{HD,MI}$	SOMI input data hold time	V_{CC} = 2.2 V		0		ns
		V_{CC} = 3 V		0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	V_{CC} = 2.2 V		30	ns
			V_{CC} = 3 V		20	

---

[1] $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

4.42 USCI (SPI Slave Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 4-30 and Figure 4-31)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	V_{CC} = 2.2 V or 3 V			50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high	V_{CC} = 2.2 V or 3 V		10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	V_{CC} = 2.2 V or 3 V			50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	V_{CC} = 2.2 V or 3 V			50		ns
$t_{SU,SI}$	SIMO input data setup time	V_{CC} = 2.2 V		20			ns
		V_{CC} = 3 V		15			
$t_{HD,SI}$	SIMO input data hold time	V_{CC} = 2.2 V		10			ns
		V_{CC} = 3 V		10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	V_{CC} = 2.2 V		75	110	ns
			V_{CC} = 3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

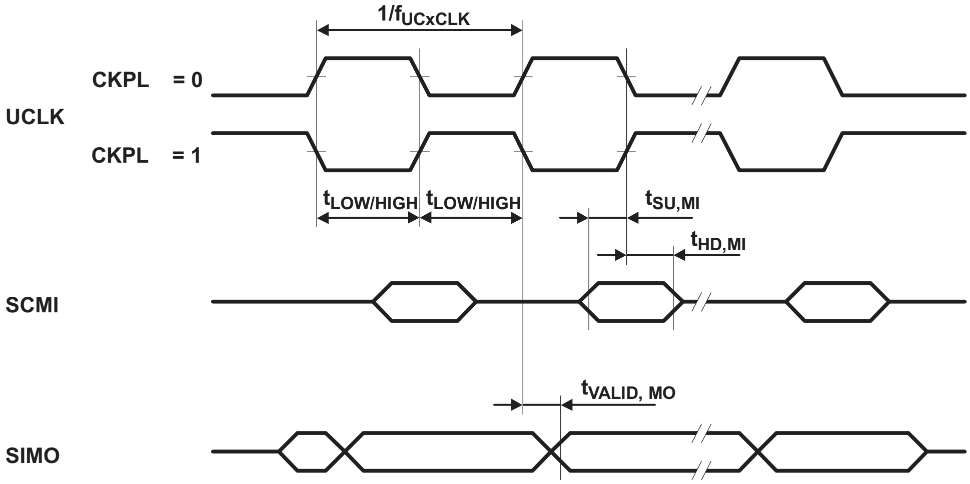


Figure 4-28. SPI Master Mode, CKPH = 0

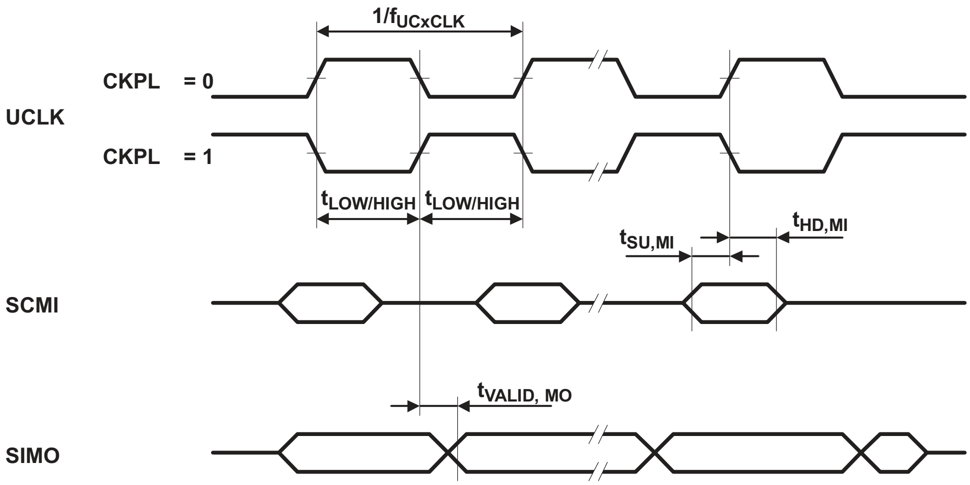


Figure 4-29. SPI Master Mode, CKPH = 1

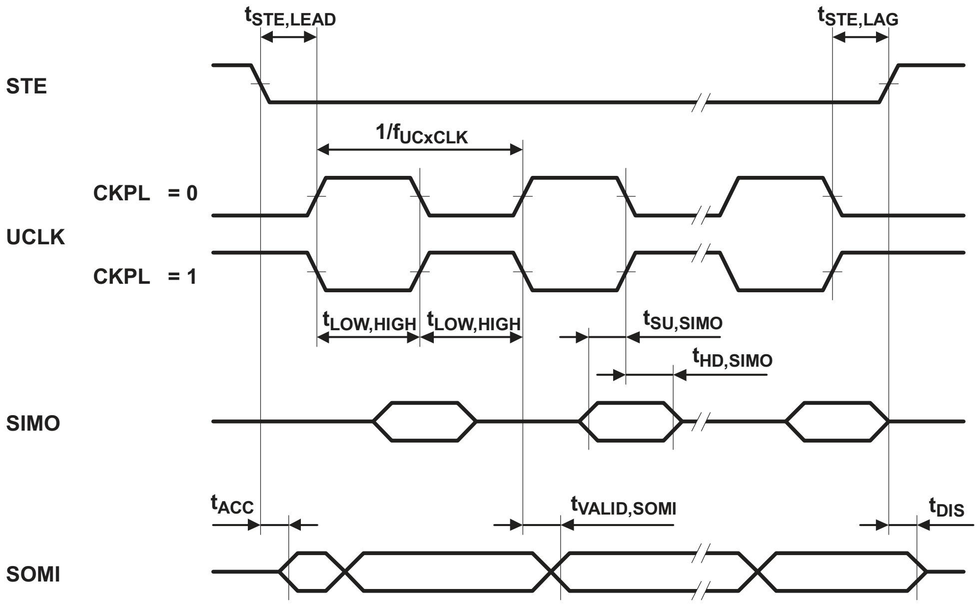


Figure 4-30. SPI Slave Mode, CKPH = 0

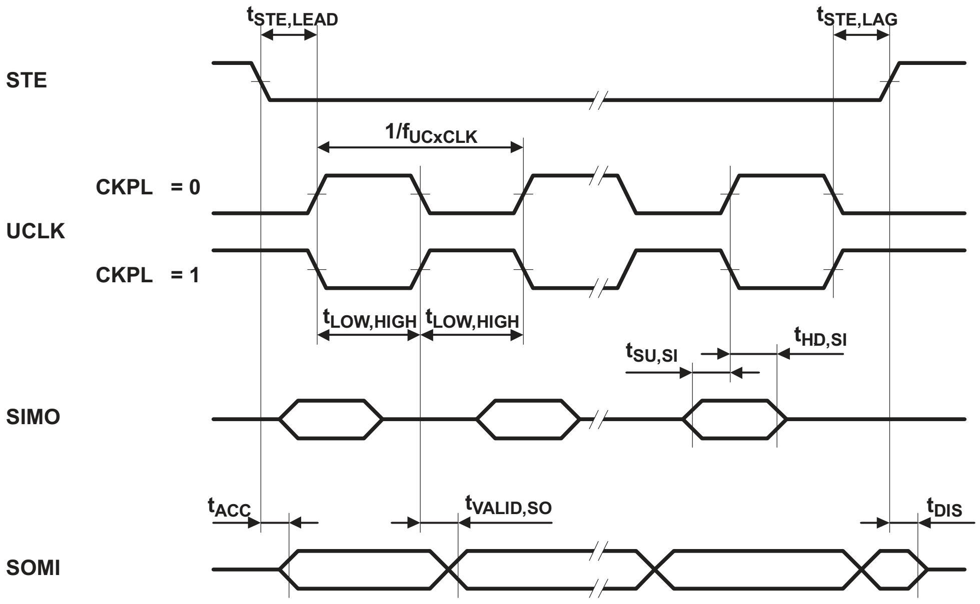


Figure 4-31. SPI Slave Mode, CKPH = 1

4.43 USCI (I2C Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4-32)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%		f_{SYSTEM}		MHz
f_{SCL}	SCL clock frequency	V_{CC} = 2.2 V or 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le$ 100 kHz, V_{CC} = 2.2 V or 3 V	4.0			µs
		$f_{SCL} >$ 100 kHz, V_{CC} = 2.2 V or 3 V	0.6			
$t_{SU,STA}$	Set-up time for a repeated START	$f_{SCL} \le$ 100 kHz, V_{CC} = 2.2 V or 3 V	4.7			µs
		$f_{SCL} >$ 100 kHz, V_{CC} = 2.2 V or 3 V	0.6			
$t_{HD,DAT}$	Data hold time	V_{CC} = 2.2 V or 3 V	0			ns
$t_{SU,DAT}$	Data set-up time	V_{CC} = 2.2 V or 3 V	250			ns
$t_{SU,STO}$	Set-up time for STOP	V_{CC} = 2.2 V or 3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter	V_{CC} = 2.2 V	50	150	600	ns
		V_{CC} = 3 V	50	100	600	

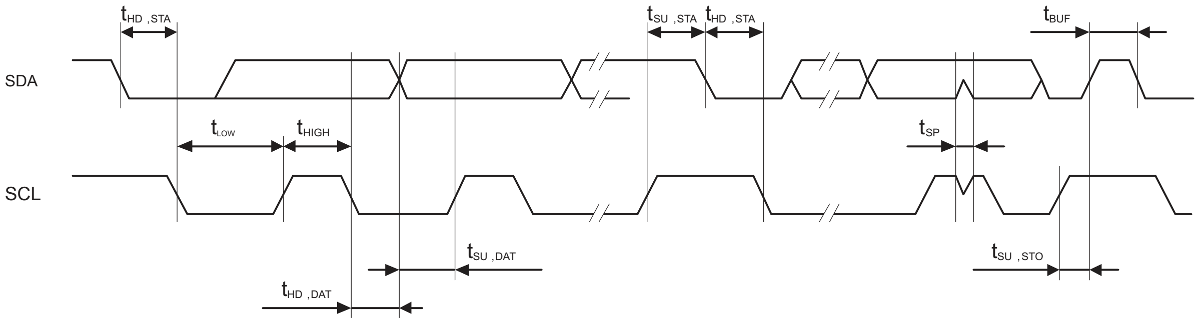


Figure 4-32. I2C Mode Timing

4.44 Comparator_A+ – Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1 CARSEL = 0 CAREF = 0	V_{CC} = 2.2 V		25	80	µA
			V_{CC} = 3 V		45	96	
$I_{(Refladder/Refdiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3 no load at P2 3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V or 3 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1, V_{CC} = 2.2 V or 3 V		0		V_{CC} - 1	V
$V_{(Ref025)}$	Voltage at 0.25 V_{CC} node/V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, V_{CC} = 2.2 V or 3 V		0.23	0.24	0.25	V
$V_{(Ref050)}$	Voltage at 0.5 V_{CC} node/V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, V_{CC} = 2.2 V or 3 V		0.47	0.48	0.5	V
$V_{(RefVT)}$	See Figure 4-36 and Figure 4-37	PCA0 = 1, CARSEL = 1, CAREF = 3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See [2], V_{CC} = 2.2 V or 3 V		–30		30	mV
V_{hys}	Input hysteresis	CAON=1, V_{CC} = 2.2 V or 3 V		0	0.7	1.4	mV
$t_{(response)}$	Response time, low-to-high and high-to-low[3]	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	V_{CC} = 2.2 V	80	165	300	ns
			V_{CC} = 3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	2.8	µs
			V_{CC} = 3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.x)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(3) The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

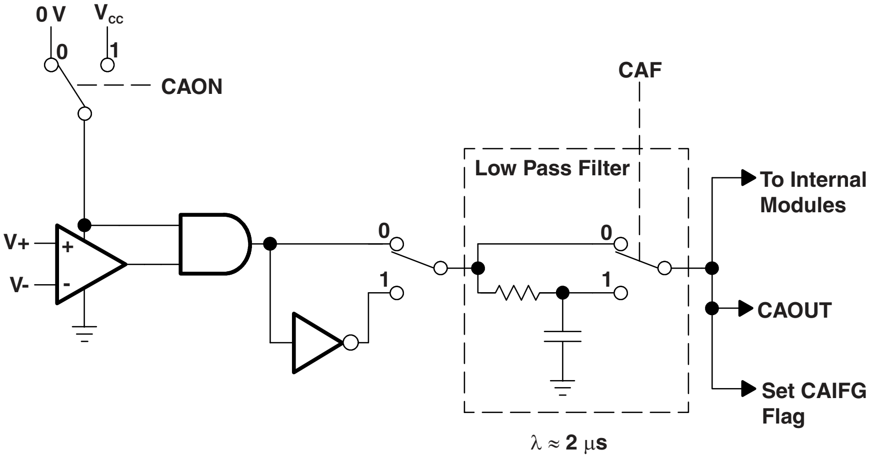


Figure 4-33. Block Diagram of Comparator_A Module

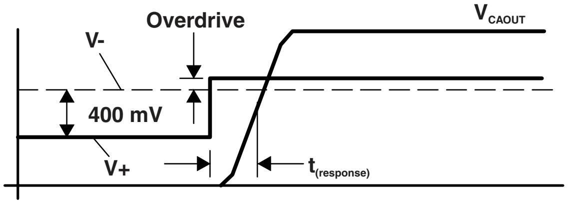


Figure 4-34. Overdrive Definition

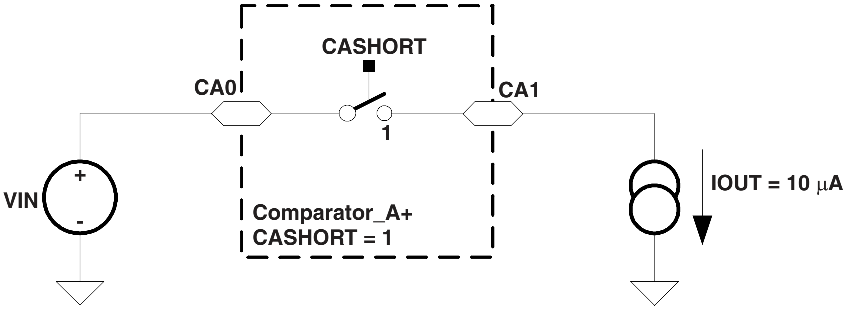


Figure 4-35. Comparator_A+ Short Resistance Test Condition

4.45 Typical Characteristics – Comparator A+

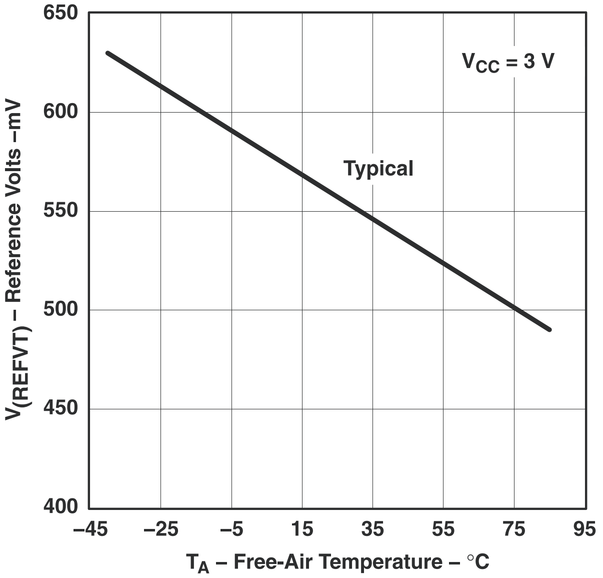


Figure 4-36. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

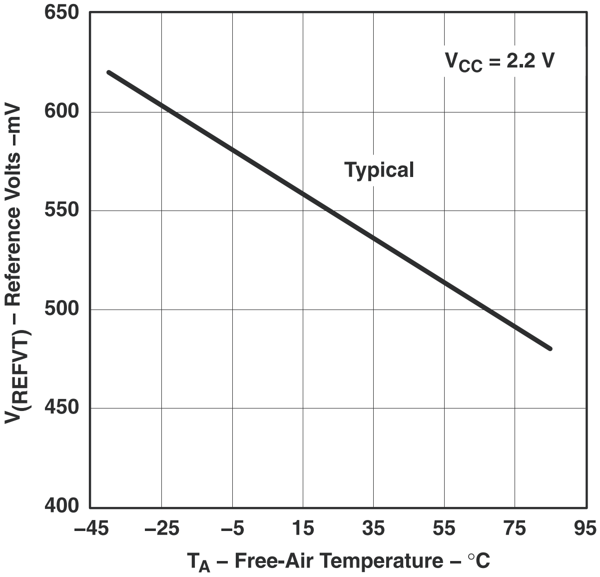


Figure 4-37. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

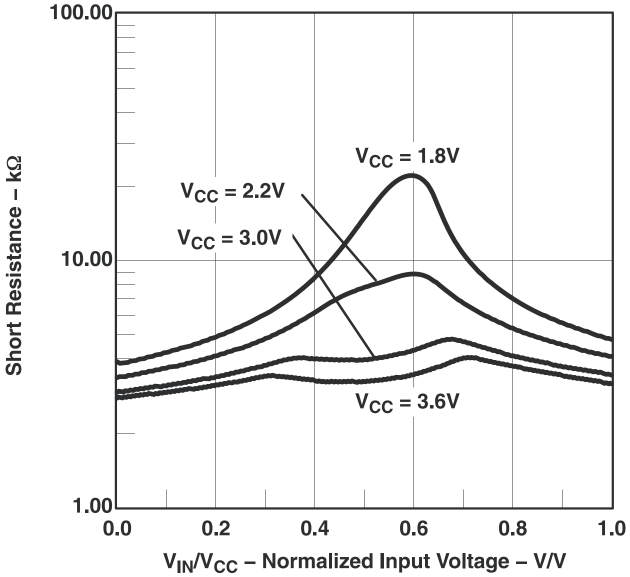


Figure 4-38. Short Resistance vs V_{IN}/V_{CC}

4.46 12-Bit ADC Power-Supply and Input Range Conditions – Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage range	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range [2]	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le VP6.x/Ax \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal[3]	$f_{ADC10CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	V_{CC} = 2.2 V		0.65	0.8	mA
			V_{CC} = 3 V		0.8	1	
I_{REF+}	Reference supply current, into AV_{CC} terminal[4]	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1, V_{CC} = 3 V			0.5	0.7	mA
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	V_{CC} = 2.2 V		0.5	0.7	
			V_{CC} = 3 V		0.5	0.7	
C_I[5]	Input capacitance	Only one terminal selected at a time, P6.x/Ax, V_{CC} = 2.2 V				40	pF
R_I[5]	Input MUX ON resistance	$0\text{ V} \le V_{Ax} \le V_{AVCC}$, V_{CC} = 3 V				2000	Ω

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.
(5) Limits verified by design.

4.47 12-Bit ADC External Reference – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-/VeREF-}$ (1)	1.4		V_{AVCC}	V
V_{REF-} /V_{eREF+}	Negative external reference voltage input	$V_{eREF+} > V_{REF-/VeREF-}$ (2)	0		1.2	V
(V_{eREF+} - V_{REF-} / V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-/VeREF-}$ (3)	1.4		V_{AVCC}	V
I_{VeREF+}	Static input current	0 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{CC} = 2.2 V or 3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	0 V ≤ V_{eREF-} ≤ V_{AVCC}, V_{CC} = 2.2 V or 3 V			±1	µA

(1) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(2) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be appliedwith reduced accuracy requirements.

(3) The accuracy limitsminimum external differential reference voltage. Lower differential reference voltage levels may be appliedwith reduced accuracy requirements.

4.48 12-Bit ADC Built-In Reference – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 (2.5 V) $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	T_A = -55°C to 85°C, V_{CC} = 3 V	2.4	2.5	2.6	V
			T_A = 150°C, V_{CC} = 3 V	2.37	2.5	2.64	
		REF2_5V = 1 (1.5 V) $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	T_A = -55°C to 85°C, V_{CC} = 2.2 V or 3 V	1.44	1.5	1.56	
			T_A = 150°C, V_{CC} = 2.2 V or 3 V	1.42	1.5	1.57	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$		2.2			V
		REF2_5V = 1, –0.5 mA ≤ $I_{VREF+} \le I_{VREF+}min$		2.8			
		REF2_5V = 1, –1 mA ≤ $I_{VREF+} \le I_{VREF+}min$		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal	V_{CC} = 3 V		0.01		–0.5	mA
		V_{CC} = 3 V		0.01		–1	
$I_{L(VREF)+}$ (1)	Load current regulation, V_{REF+} terminal	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \not\approx$ 0.75 V, REF2_5V = 0	V_{CC} = 3 V			±2	LSB
			V_{CC} = 3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \not\approx$ 1.25 V, REF2_5V = 1, V_{CC} = 3 V				±2	
$I_{DL(VREF)+}$ (2)	Load current regulation, V_{REF+} terminal	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, at $\not\approx$ 0.5 V_{REF+}, Error of conversion result ≤ 1 LSB, V_{CC} = 3 V				20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (3)	REFON = 1, 0 mA ≤ $I_{VREF+} \le I_{VREF+}max$, V_{CC} = 2.2 V or 3 V		5	10		µF
T_{REF+} (1)	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA, V_{CC} = 2.2 V or 3 V				±100	ppm/°C
t_{REFON} (1)	Settling time of internal reference voltage (4) (see Figure 4-39)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

(1) Limits characterized.
(2) Limits verified by design.
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests use two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

4.49 Typical Characteristics – ADC12

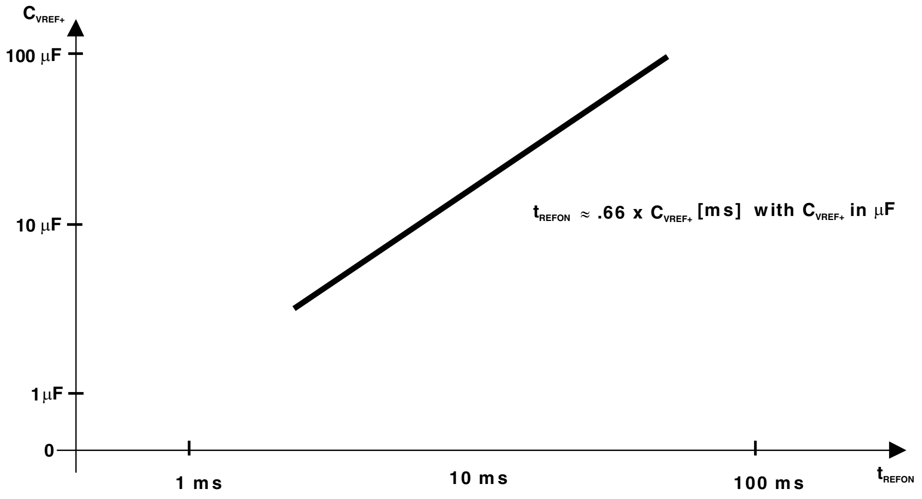


Figure 4-39. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

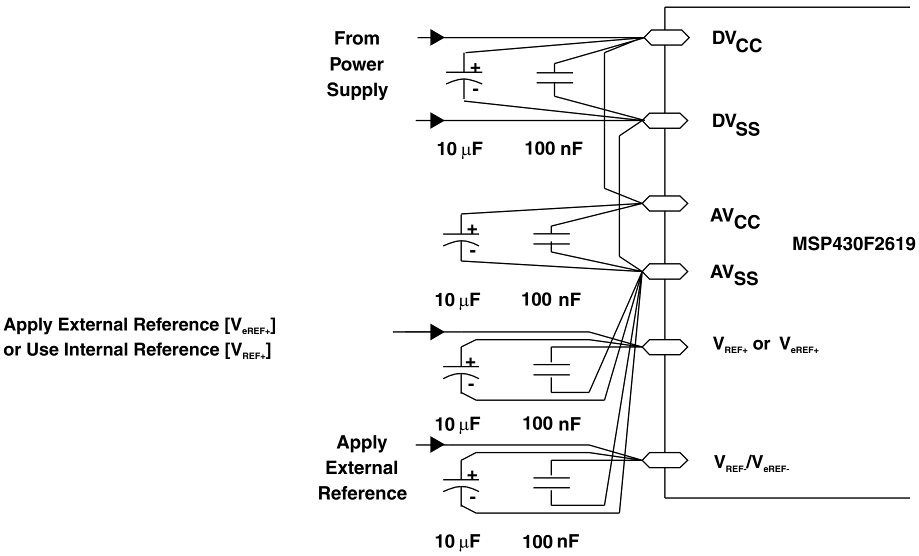


Figure 4-40. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

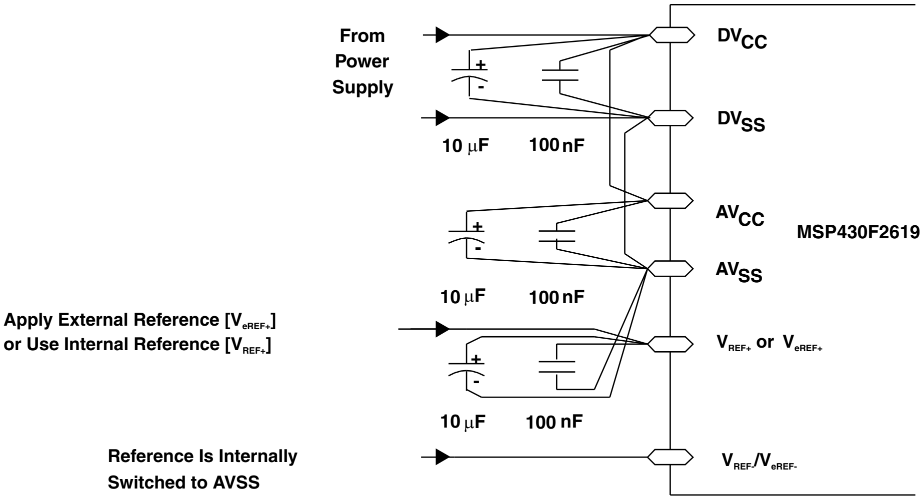


Figure 4-41. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{eREF-} = AV_{SS}$, Internally Connected

4.50 12-Bit ADC Timing Parameters – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC12 input clock frequency	For specified performance of ADC12 linearity parameters, V_{CC} = 2.2 V or 3 V		0.45	5	6.3	MHz
$f_{ADC12OSC}$	ADC12 built-in oscillator frequency	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$, V_{CC} = 2.2 V or 3 V		3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	ADC12 built-in oscillator, $C_{VREF+} \geq 5\ \mu F$, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz, V_{CC} = 2.2 V or 3 V		2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK: ADC12SSEL ≠ 0			13 x ADC12DIV x $1/f_{ADC12CLK}$		
$t_{ADC12ON}$ (1)	Turn-on settling time of the ADC	See (2)				100	ns
t_{Sample} (1)	Sampling time	RS = 400 Ω, RI = 1000 Ω, CI = 30 pF, $\tau = [R_S + R_I] \times C_I$ (3)	V_{CC} = 3 V	1220			ns
			V_{CC} = 2.2 V	1400			

(1) Limits verified by design.
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB: $t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I +$ 800 ns where n = ADC resolution = 12, R_S = external source resistance.

4.51 12-Bit ADC Linearity Parameters – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ 1.6 V, V_{CC} = 2.2 V or 3 V			±2	LSB
		1.6 V < (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ V_{AVCC}, V_{CC} = 2.2 V or 3 V			±1.7	
E_D	Differential linearity error	(V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic), V_{CC} = 2.2 V or 3 V			±1	LSB
E_O	Offset error	(V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic), V_{CC} = 2.2 V or 3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic), V_{CC} = 2.2 V or 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic), V_{CC} = 2.2 V or 3 V		±2	±5	LSB

4.52 12-Bit ADC Temperature Sensor and Built-In V_{MID} – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal[1]	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C, VCC = 2.2 V	V_{CC} = 2.2 V		40	120	µA
			V_{CC} = 3 V		60	160	
V_{Sensor}[2]	Sensor output voltage[3]	ADC12ON = 1, INCH = 0Ah, T_A = 0°C, V_{CC} = 2.2 V or 3 V			986		mV
TC_{SENSOR}[2]		ADC12ON = 1, INCH = 0Ah, V_{CC} = 2.2 V or 3 V			3.55		mV/°C
$t_{Sensor(sample)}$[2]	Sample time required if channel 10 is selected[4]	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB, V_{CC} = 2.2 V or 3 V		30			µs
I_{VMID}	Current into divider at channel 11[5]	ADC12ON = 1, INCH = 0Bh	V_{CC} = 2.2 V			NA	µA
			V_{CC} = 3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ≉ 0.5 × V_{AVCC}	V_{CC} = 2.2 V		1.1	1.1±0.04	V
			V_{CC} = 3 V		1.5	1.5 ±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected[6]	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	V_{CC} = 2.2 V	1400			ns
			V_{CC} = 3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1) or (ADC12ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) Limits characterized.
(3) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

4.53 12-Bit DAC Supply Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AV_{CC}	Supply voltage range	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ = 0 V		2.2		3.6	V
I_{DD}	Supply current, single DAC channel[1][2]	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0x0800, V_{CC} = 2.2 V or 3 V	T_A = -55°C to 85°C		50	110	µA
			T_A = 105°C		69	150	
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$, V_{CC} = 2.2 V or 3 V			50	130	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$, V_{CC} = 2.2 V or 3 V			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$, V_{CC} = 2.2 V or 3 V			700	1500	
PSSR	Power-supply rejection ratio[3][4]	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV, V_{CC} = 2.2 V or 3 V			70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV, V_{CC} = 2.2 V or 3 V			70		

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Section 4.57.
(3) PSRR = 20 × log{$\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}$}
(4) V_{REF} is applied externally. The internal reference is not used.

4.54 12-Bit DAC Linearity Parameters – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic	12			bits
INL	Integral nonlinearity(1)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±2	±8	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±2	±8	
DNL	Differential nonlinearity(1)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±0.4	±1	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±0.4	±1	
E_O	Offset voltage without calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±21		LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V		±21		
	Offset voltage with calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V			±3.5	
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1, V_{CC} = 2.2 V or 3 V			±3.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient(1)			30		µV/°C
E_G	Gain error(1)	V_{REF} = 1.5 V, V_{CC} = 2.2 V or 3 V			±3.5	LSB
		V_{REF} = 2.5 V, V_{CC} = 2.2 V or 3 V			±3.5	
$d_{E(G)}/d_T$	Gain temperature coefficient(1)			10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration(3)	DAC12AMPx = 2, V_{CC} = 2.2 V or 3 V			100	LSB
		DAC12AMPx = 3, 5, V_{CC} = 2.2 V or 3 V			32	
		DAC12AMPx = 4, 6, 7, V_{CC} = 2.2 V or 3 V			6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + b × x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx={0, 1}.The DAC12 module should be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

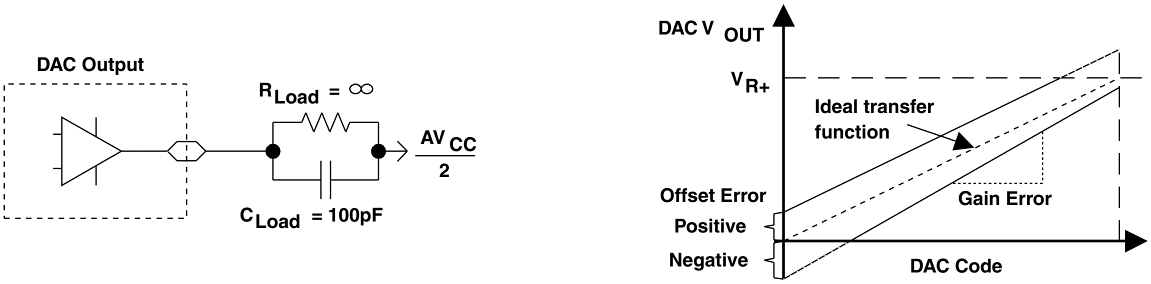


Figure 4-42. Linearity Test Load Conditions and Gain/Offset Definition

4.55 Typical Characteristics - 12-Bit DAC Linearity Specifications

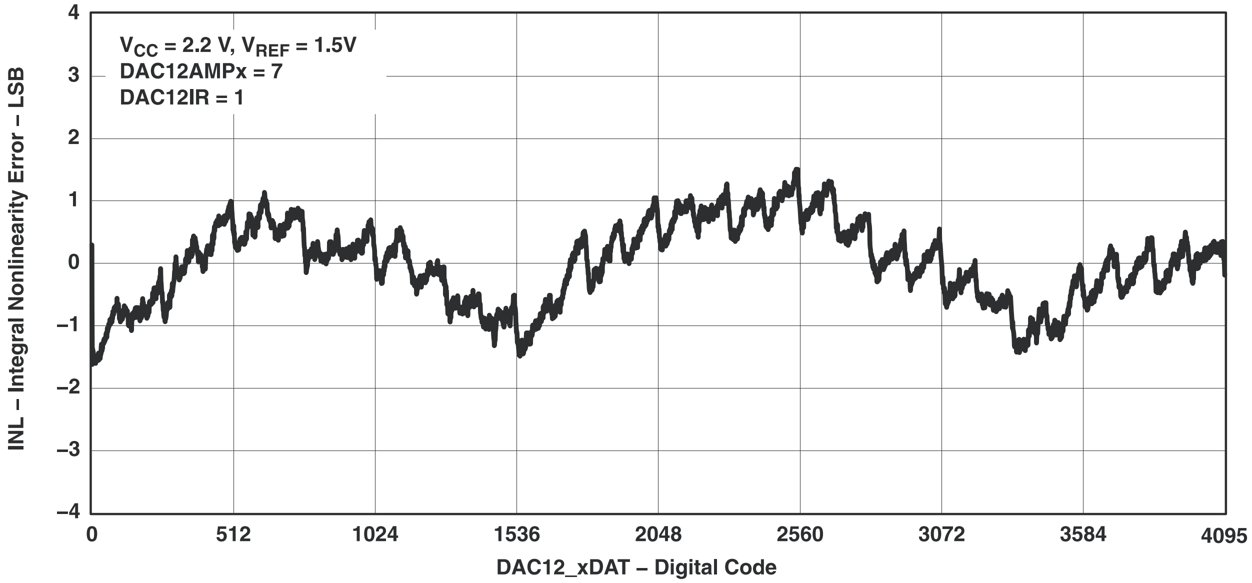


Figure 4-43. Typical INL Error vs Digital Input Data

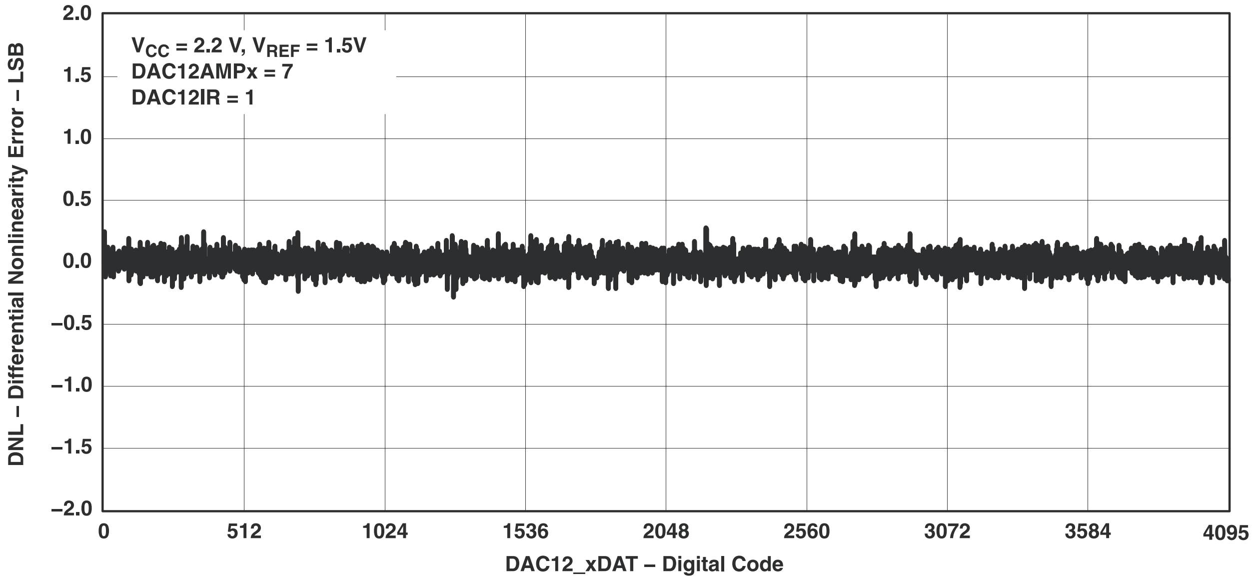


Figure 4-44. Typical DNL Error vs Digital Input Data

4.56 12-Bit DAC Output Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage range[1] (see Figure 4-45)	No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = $7V_{CC}$ = 2.2 V or 3 V	0		0.005	V
		No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = $7V_{CC}$ = 2.2 V or 3 V	AV_{CC} - 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7, V_{CC} = 2.2 V or 3 V	0		0.1	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7, V_{CC} = 2.2 V or 3 V	AV_{CC} - 0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance	V_{CC} = 2.2 V or 3 V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current	V_{CC} = 2.2 V	–0.5		0.5	mA
		V_{CC} = 3 V	–1		1	
$R_{O/P(DAC12)}$	Output resistance (see Figure 4-45)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h, V_{CC} = 2.2 V or 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0FFFh, V_{CC} = 2.2 V or 3 V		150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} - 0.3 V, DAC12AMPx = 7, V_{CC} = 2.2 V or 3 V		1	4	

---

(1) Data is valid after the offset calibration of the output amplifier.

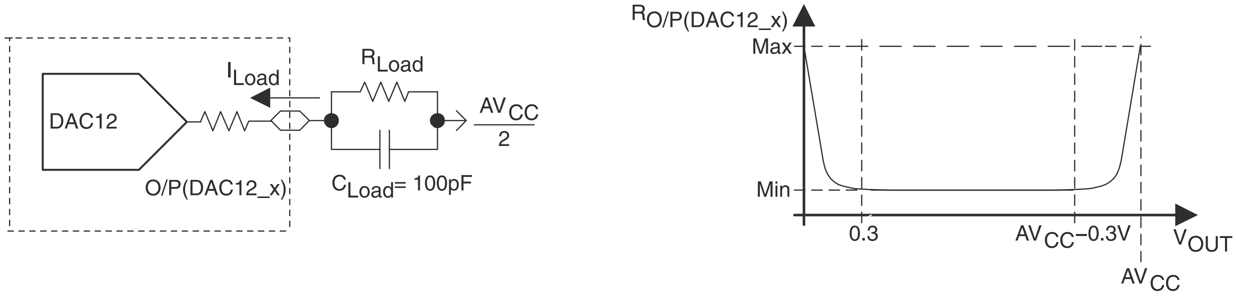


Figure 4-45. DAC12_x Output Resistance Tests

4.57 12-Bit DAC Reference Input Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{eREF+}	Reference input voltage range	DAC12IR = 0 [1][2], V_{CC} = 2.2 V or 3 V		$AV_{CC}/3$	AV_{CC} + 0.2	V
		DAC12IR = 1 [3][4], V_{CC} = 2.2 V or 3 V		AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0, V_{CC} = 2.2 V or 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0, V_{CC} = 2.2 V or 3 V	40	48	56	kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1, V_{CC} = 2.2 V or 3 V	20	24	28	
		DAC12_0 IR = 0, DAC12_1 IR = 1 DAC12_0 SREFx = DAC12_1 SREFx [5], V_{CC} = 2.2 V or 3 V				

---

[1] For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).

[2] The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} - V_{E(O)}] / [3 \times (1 + E_G)]$.

[3] For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).

[4] The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.

[5] When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

4.58 12-Bit DAC Dynamic Specifications, $V_{REF} = V_{CC}$, DAC12IR = 1 – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	SR	DAC12_xDAT = 800h, $Error_{V(O)} < \pm0.5$ LSB[1] (see Figure 4-46), V_{CC} = 2.2 V or 3 V	DAC12AMPx = 0 → {2, 3, 4}		60	120	µs
			DAC12AMPx = 0 → {5, 6}		15	30	
			DAC12AMPx = 0 → 7		6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h, V_{CC} = 2.2 V or 3 V	DAC12AMPx = 2		100	200	µs
			DAC12AMPx = 3, 5		40	80	
			DAC12AMPx = 4, 6, 7		15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h, V_{CC} = 2.2 V or 3 V	DAC12AMPx = 2		5		µs
			DAC12AMPx = 3, 5		2		
			DAC12AMPx = 4, 6, 7		1		
SR	Slew rate[2]	DAC12_xDAT = 80h → F7Fh → 80h, V_{CC} = 2.2 V or 3 V	DAC12AMPx = 2	0.05	0.12		V/µs
			DAC12AMPx = 3, 5	0.35	0.7		
			DAC12AMPx = 4, 6, 7	1.5	2.7		
	Glitch energy, full scale	DAC12_xDAT = 80h → F7Fh → 80h, V_{CC} = 2.2 V or 3 V	DAC12AMPx = 2		600		nV-s
			DAC12AMPx = 3, 5		150		
			DAC12AMPx = 4, 6, 7		30		
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 4-48)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, V_{CC} = 2.2 V or 3 V		40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, V_{CC} = 2.2 V or 3 V		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h, V_{CC} = 2.2 V or 3 V		550			
	Channel-to-channel crosstalk[3] (see Figure 4-49)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz, Duty cycle = 50%, V_{CC} = 2.2 V or 3 V			–80		dB
		DAC12_0DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f_{DAC12_0OUT} = 10 kHz, Duty cycle = 50%, V_{CC} = 2.2 V or 3 V			–80		

[1] R_{Load} and C_{Load} are connected to AV_{SS} (not $AV_{CC}/2$) in Figure 4-46.
[2] Slew rate applies to output voltage steps ≥ 200 mV.
[3] R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

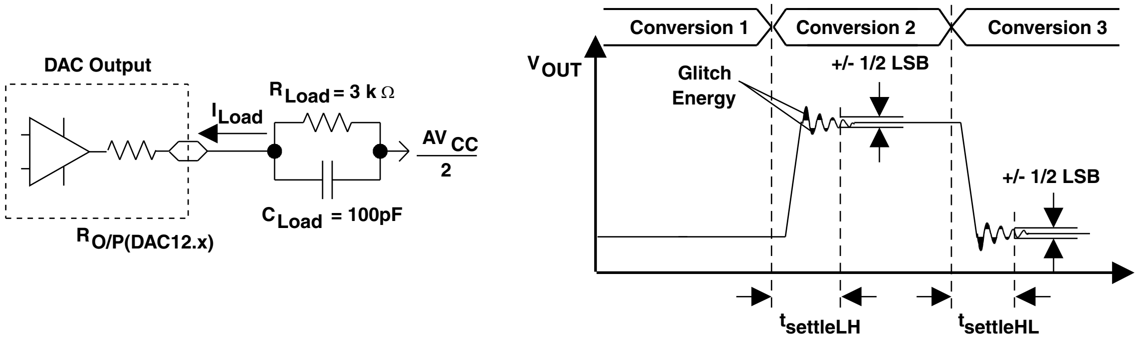


Figure 4-46. Settling Time and Glitch Energy Testing

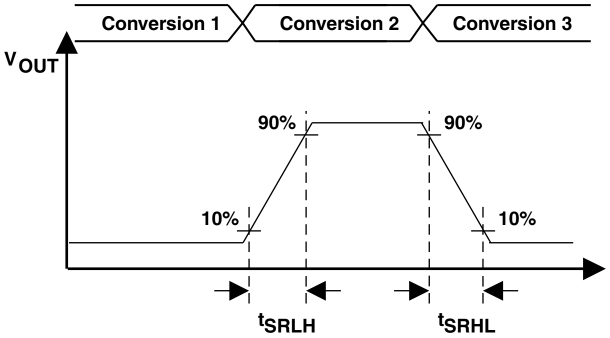


Figure 4-47. Slew Rate Testing

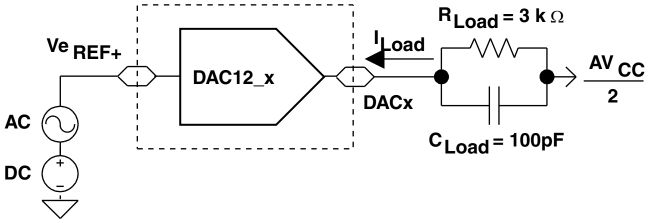


Figure 4-48. Test Conditions for 3-dB Bandwidth Specification

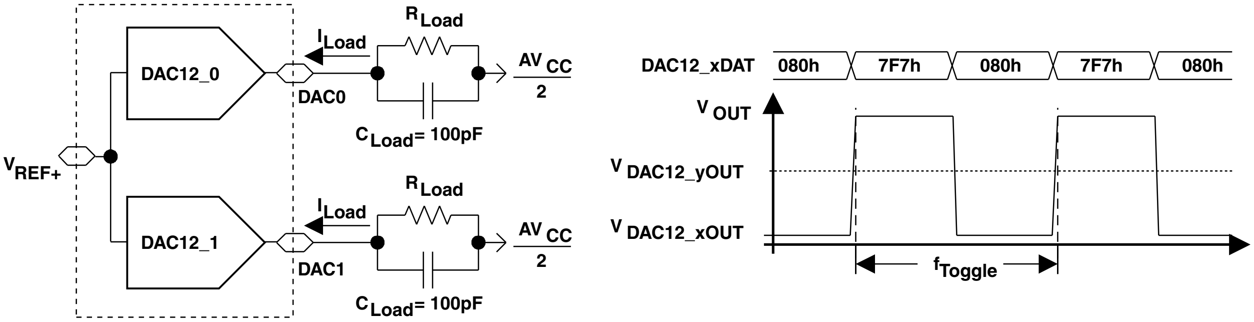


Figure 4-49. Crosstalk Test Conditions

4.59 Flash Memory – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage		2.2		3.6	V
f_{FTG}	Flash timing generator frequency		257		476	kHz
I_{PGM}	Supply current from V_{CC} during program	V_{CC} = 2.2 or 3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase	V_{CC} = 2.2 or 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	See (1), V_{CC} = 2.2 or 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time	V_{CC} = 2.2 or 3.6 V	20			ms
	Program/Erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
t_{Word}	Word or byte program time	See (2)		35		t_{FTG}
$t_{Block,\ 0}$	Block program time for 1st byte or word	See (2)		30		t_{FTG}
$t_{Block,\ 1\text{-}63}$	Block program time for each additional byte or word	See (2)		21		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

Flash Memory – Electrical Characteristics *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Block,\ End}$	Block program end-sequence wait time	See (2)		6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	See (2)		10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	See (2)		4819		t_{FTG}

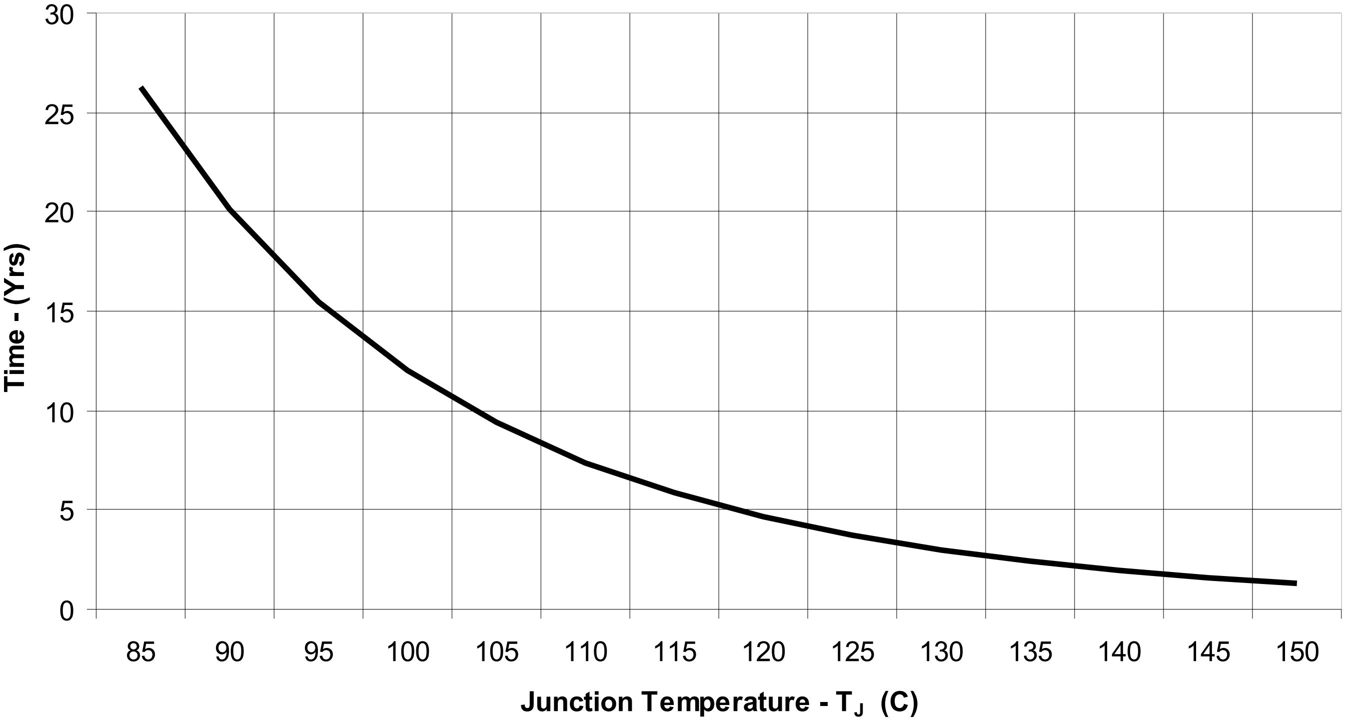


Figure 4-50. Flash Data Retention vs Junction Temperature

4.60 RAM – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

4.61 JTAG and Spy-Bi-Wire Interface – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See (1)	V_{CC} = 2.2 V	0		5	MHz
			V_{CC} = 3 V	0		10	
$R_{Internal}$	Internal pulldown resistance on TEST	See (2), V_{CC} = 2.2 V or 3 V		25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

4.62 JTAG Fuse(1) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

5 Detailed Description

5.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

5.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 5-1 shows examples of the three types of instruction formats; the address modes are listed in Table 5-2.

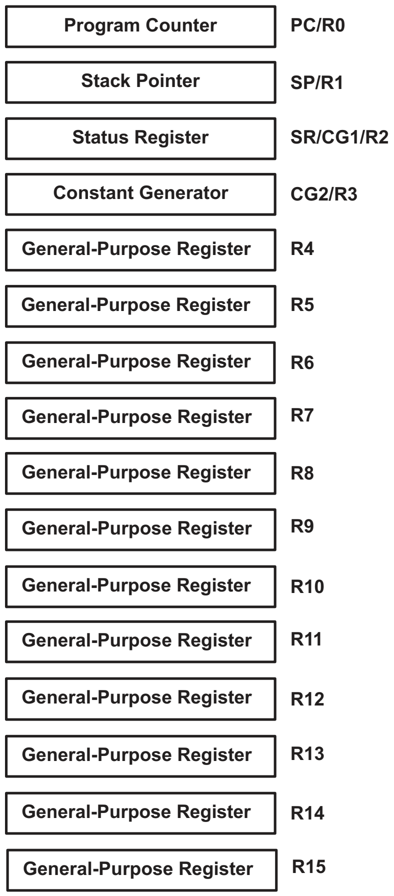


Table 5-1. Instruction Word Formats

Dual operands, source-destination	For example, ADD R4,R5	R4 + R5 → R5
Single operands, destination only	For example, CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	For example, JNE	Jump-on-equal bit = 0

Table 5-2. Address Mode Descriptions

ADDRESS MODE	S[1]	D[2]	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	•	•	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

5.3 Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
  - DCO’s DC generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc-generator remains enabled.
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc-generator is disabled.
  - Crystal oscillator is stopped.

5.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFF–0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV (2)	Reset	0x0FFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable, (non)-maskable, (non)-maskable	0x0FFFC	30
Timer_B7	TBCCR0 CCIFG(4)	maskable	0x0FFFA	29
Timer_B7	TBCCR1 and TBCCR2 CCIFGs, TBIFG(2)(4)	maskable	0x0FFF8	28
Comparator_A+	CAIFG	maskable	0x0FFF6	27
Watchdog timer+	WDTIFG	maskable	0x0FFF4	26
Timer_A3	TACCR0 CCIFG(4)	maskable	0x0FFF2	25
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG(2)(4)	maskable	0x0FFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0x0FFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0x0FFEC	22
ADC12	ADC12IFG(4)	maskable	0x0FFEA	21
			0x0FFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0x0FFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0x0FFE4	18
USCI_A0/USCI_B1 receive USCI_B1 I2C status	UCA1RXIFG, UCB1RXIFG(2)(5)	maskable	0x0FFE2	17
USCI_A1/USCI_B1 transmit USCI_B1 I2C receive/transmit	UCA1TXIFG, UCB1TXIFG(2)(6)	maskable	0x0FFE0	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG(2)(4)	maskable	0x0FFDE	15
DAC12	DAC12_0IFG, DAC12_1IFG(2)(4)	maskable	0x0FFDC	14
Reserved(7)(8)	Reserved		0x0FFDA to 0x0FFC0	13 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0x00000 – 0x001FF) or from within unused address range.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I^2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I^2C mode: UCB0RXIFG, UCB0TXIFG.
(7) The address 0x0FFBE is used as bootstrap loader security key (BSLSKEY). A 0x0AA55 at this location disables the BSL completely. A zero disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0x0FFDC to 0x0FFC0 are not used in this device and can be used for regular program code if necessary.

5.5 Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

5.5.1 Interrupt Enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE: Oscillator fault enable

NMIIE: (Non)maskable interrupt enable

ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

5.5.2 Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	▨	▨	▨	**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	**rw-(0)**	**rw-(1)**	**rw-1**	**rw-(0)**

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault7

RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode. Reset on V_{CC} power up.

PORIFG: Power-On Reset interrupt flag. Set on V_{CC} power up.

NMIIFG: Set via $\overline{\text{RST}}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	▨	▨	▨	▨	**UCB0 TXIFG**	**UCB0 RXIFG**	**UCA0 TXIFG**	**UCA0 RXIFG**
					rw-1	**rw-0**	**rw-1**	**rw-0**

UCA0RXIFG	USCI_A0 receive-interrupt flag
UCA0TXIFG	USCI_A0 transmit-interrupt flag
UCB0RXIFG	USCI_B0 receive-interrupt flag
UCB0TXIFG	USCI_B0 transmit-interrupt flag

Legend:

rw: Bit can be read and written.

rw-0, 1: Bit can be read and written. It is Reset or Set by PUC.

rw-(0), (1): Bit can be read and written. It is Reset or Set by POR.

▨ SFR bit is not present in device.

5.6 Memory Organization

		MSP430F2619
Memory Main: interrupt vector Main: code memory	Size Flash Flash	120 kB Flash 0x0FFFF – 0x0FFC0 0x0FFFF – 0x02100
RAM (total)	Size	4 kB 0x020FF -- 0x01100
Extended	Size	2 kB 0x020FF -- 0x01900
Mirrored	Size	2 kB 0x018FF -- 0x01100
Information memory	Size Flash	256 Byte 0x010FF – 0x01000
Boot memory	Size ROM	1 kB 0x0FFF – 0x0C00
RAM (mirrored at 18FFh to 01100h)	Size	2 kB 0x009FF – 0x0200
Peripherals	16-bit 8-bit 8-bit SFR	0x001FF – 0x00100 0x000FF – 0x00010 0x0000F – 0x00000

5.7 Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see *Features of the MSP430 Bootstrap Loader* (SLAA089).

BSL Function	PM Package Pins
Data Transmit	13 - P1.1
Data Receive	22 - P2.2

5.8 Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
- Flash content integrity check with marginal read modes.

5.9 Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to *MSP430x2xx Family User's Guide* (SLAU144).

5.10 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversionmemory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

5.11 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator for –55°C to 105°C operation. For > 105°C, use external clock source.
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Table 5-3. Tags Used by the TLV Structure

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at VCC = 3 V and T_A = 25°C at calibration
TAG_ADC12_1	0x10DA	0x08	ADC12_1 calibration tag
TAG_EMPTY	--	0xFE	Identifier for empty areas

Table 5-4. Labels Used by the ADC Calibration Structure

LABEL	CONDITION AT CALIBRATION/DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010; REF2_5 = 1, T_A = 125°C	word	0x000E
CAL_ADC_25T30	INCHx = 0x1010; REF2_5 = 1, T_A = 30°C	word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1,T_A = 30°C	word	0x000A
CAL_ADC_15T85	INCHx = 0x1010; REF2_5 = 0, T_A = 125°C	word	0x0008
CAL_ADC_15T30	INCHx = 0x1010; REF2_5 = 0, T_A = 30°C	word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0,T_A = 30°C	word	0x0004
CAL_ADC_OFFSET	External V_{REF} = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0002
CAL_ADC_GAIN_FACTOR	External V_{REF} = 1.5 , $f_{ADC12CLK}$ = 5 MHz	word	0x0000
CAL_BC1_1MHZ	--	byte	0x0007
CAL_DCO_1MHZ	--	byte	0x0006
CAL_BC1_8MHZ	--	byte	0x0005
CAL_DCO_8MHZ	--	byte	0x0004
CAL_BC1_12MHZ	--	byte	0x0003
CAL_DCO_12MHZ	--	byte	0x0002
CAL_BC1_16MHZ	--	byte	0x0001
CAL_DCO_16MHZ	--	byte	0x0000

5.12 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until VCC reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

5.13 Digital I/O

There are six 8-bit I/O ports implemented – ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

5.14 WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

5.15 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16 × 16, 16 × 8, 8 × 16, and 8 × 8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

5.16 USCI

The universal serial communication interface (USCI) module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I^2C and asynchronous communication protocols like UART, enhanced UART with automatic baud-rate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I^2C.

5.17 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 5-5. TIMER_A3 Signal Connections

INPUT PIN NO.	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE U SIGNAL	OUTPUT PIN NO.
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	V_{CC}			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DV_{SS}	GND			23 - P2.3
	DV_{CC}	V_{CC}			ADC12 (internal)
					DAC12_0 (internal)
					DAC12_1 (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DV_{SS}	GND			24 - P2.4
	DV_{CC}	V_{CC}			

5.18 Timer_B7

Timer_B7 is a 16-bit timer/counter with three capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B7 Signal Connections

INPUT PIN NO.	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NO.
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	$\overline{\text{TBCLK}}$	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			DAC_0 (internal)
	DV_{SS}	GND			DAC_1 (internal)
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

5.19 Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

5.20 ADC12

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

5.21 DAC12

The DAC12 module is a 12-bit, R-ladder, voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

5.22 Peripheral File Map

DMA	DMA channel 2 transfer size	DMA2SZ	0x01F2
	DMA channel 2 destination address	DMA2DA	0x01EE
	DMA channel 2 source address	DMA2SA	0x01EA
	DMA channel 2 control	DMA2CTL	0x01E8
	DMA channel 1 transfer size	DMA1SZ	0x01E6
	DMA channel 1 destination address	DMA1DA	0x01E2
	DMA channel 1 source address	DMA1SA	0x01DE
	DMA channel 1 control	DMA1CTL	0x01DC
	DMA channel 0 transfer size	DMA0SZ	0x01DA
	DMA channel 0 destination address	DMA0DA	0x01D6
	DMA channel 0 source address	DMA0SA	0x01D2
	DMA channel 0 control	DMA0CTL	0x01D0
	DMA module interrupt vector word	DMAIV	0x0126
	DMA module control 1	DMACTL1	0x0124
	DMA module control 0	DMACTL0	0x0122
DAC12	DAC12_1 data	DAC12_1DAT	0x01CA
	DAC12_1 control	DAC12_1CTL	0x01C2
	DAC12_0 data	DAC12_0DAT	0x01C8
	DAC12_0 control	DAC12_0CTL	0x01C0
ADC12	Interrupt-vector-word register	ADC12IV	0x01A8
	Interrupt-enable register	ADC12IE	0x01A6
	Interrupt-flag register	ADC12IFG	0x01A4
	Control register 1	ADC12CTL1	0x01A2
	Control register 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C

ADC12	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion 0	ADC12MEM0	0x0140
	ADC memory-control register15	ADC12MCTL15	0x008F
	ADC memory-control register14	ADC12MCTL14	0x008E
	ADC memory-control register13	ADC12MCTL13	0x008D
	ADC memory-control register12	ADC12MCTL12	0x008C
	ADC memory-control register11	ADC12MCTL11	0x008B
	ADC memory-control register10	ADC12MCTL10	0x008A
	ADC memory-control register9	ADC12MCTL9	0x0089
	ADC memory-control register8	ADC12MCTL8	0x0088
	ADC memory-control register7	ADC12MCTL7	0x0087
	ADC memory-control register6	ADC12MCTL6	0x0086
	ADC memory-control register5	ADC12MCTL5	0x0085
	ADC memory-control register4	ADC12MCTL4	0x0084
	ADC memory-control register3	ADC12MCTL3	0x0083
	ADC memory-control register2	ADC12MCTL2	0x0082
	ADC memory-control register1	ADC12MCTL1	0x0081
	ADC memory-control register0	ADC12MCTL0	0x0080
Timer_B7	Capture/compare register _ 6	TBCCR6	0x019E
	Capture/compare register 5	TBCCR5	0x019C
	Capture/compare register 4	TBCCR4	0x019A
	Capture/compare register 3	TBCCR3	0x0198
	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E

Timer_A3	Capture/compare register 2	TACCR2	0x0176
	Capture/compare register 1	TACCR1	0x0174
	Capture/compare register 0	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed +accumulate/operand1	MACS	0x0136
	Multiply+accumulate/operand1	MAC	0x0134
	Multiply signed/operand1	MPYS	0x0132
	Multiply unsigned/operand1	MPY	0x0130
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog/timer control	WDTCTL	0x0120
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I^{2}C interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I^{2}C slave address	UCB0SA	0x011A
	USCI B0 I^{2}C own address	UCB0OA	0x0118

USCI A1/B1	USCI A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI A1 receive buffer	UCA1RXBUF	0x00D6
	USCI A1 status	UCA1STAT	0x00D5
	USCI A1 modulation control	UCA1MCTL	0x00D4
	USCI A1 baud rate control 1	UCA1BR1	0x00D3
	USCI A1 baud rate control 0	UCA1BR0	0x00D2
	USCI A1 control 1	UCA1CTL1	0x00D1
	USCI A1 control 0	UCA1CTL0	0x00D0
	USCI A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI A1 IrDA transmit control	UCA1IRTCLT	0x00CE
	USCI B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI B1 receive buffer	UCB1RXBUF	0x00DE
	USCI B1 status	UCB1STAT	0x00DD
	USCI B1 I2C Interrupt enable	UCB1CIE	0x00DC
	USCI B1 baud rate control 1	UCB1BR1	0x00DB
	USCI B1 baud rate control 0	UCB1BR0	0x00DA
	USCI B1 control 1	UCB1CTL1	0x00D9
	USCI B1 control 0	UCB1CTL0	0x00D8
	USCI B1 I2C slave address	UCB1SA	0x017E
	USCI B1 I2C own address	UCB1OA	0x017C
	USCI A1/B1 interrupt enable	UC1IE	0x0006
	USCI A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059
Basic Clock	Basic clock system control3	BCSCTL3	0x0053
	Basic clock system control2	BCSCTL2	0x0058
	Basic clock system control1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030
Port P4	Port P4 selection	P4SEL	0x001F
	Port P4 resistor enable	P4REN	0x0011
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C

Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag2	IFG2	0x0003
	SFR interrupt flag1	IFG1	0x0002
	SFR interrupt enable2	IE2	0x0001
	SFR interrupt enable1	IE1	0x0000

6 Applications, Implementation, and Layout

6.1 P1.0 to P1.7, Input/Output With Schmitt Trigger

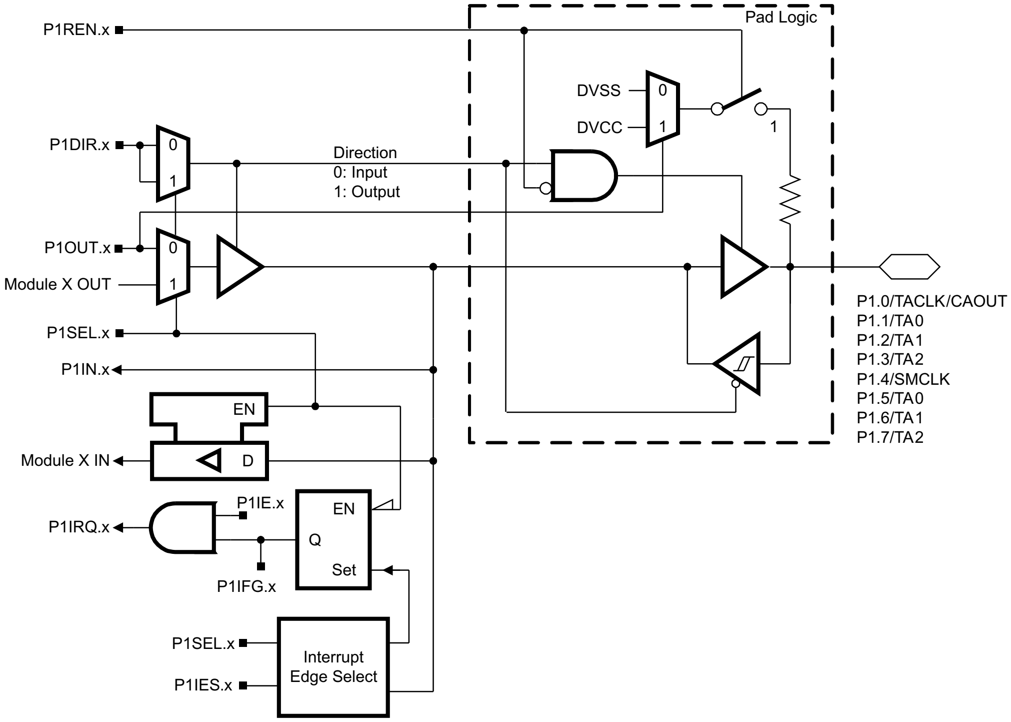


Figure 6-1. Port P1 (P1.0 to P1.7) Pin Schematic

Table 6-1. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3 I/O	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer_A3.TA2	1	1

6.2 P2.0 to P2.4, P2.6, and P2.7, Input/Output With Schmitt Trigger

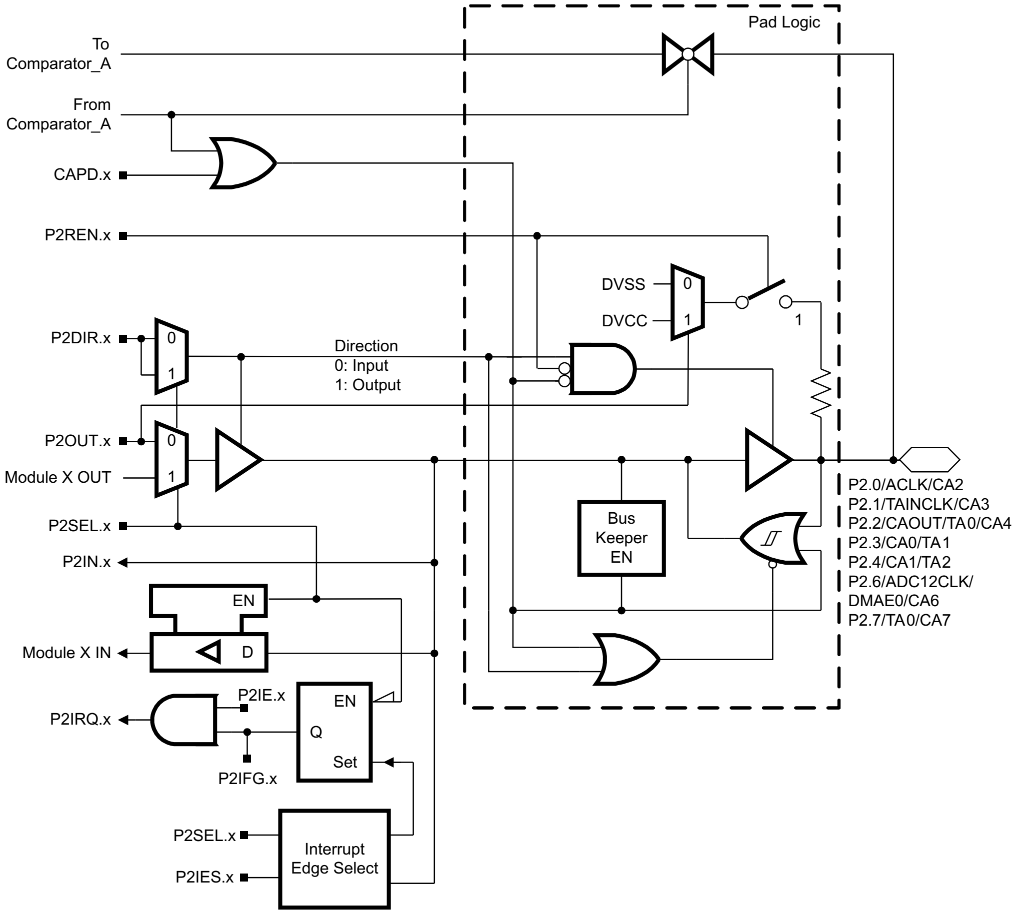


Figure 6-2. Port P2.0, P2.3, P2.4, P2.6 and P2.7 Pin Schematic

Table 6-2. Port P2.0, P2.3, P2.4, P2.6 and P2.7 Pin Functions

Pin Name (P2.X)	X	FUNCTION	CONTROL BITS/SIGNALS[1]		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0; O: 1	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TAINCLK/CA3	1	P2.2 (I/O)	0	I: 0; O: 1	0
		Timer_A3.INCLK	0	0	1
		DV_{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/CA4	2	P2.2 (I/O)	0	I: 0; O: 1	0
		CAOUT	0	1	1
		Timer_A3.CCI0B	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK/ DMAE0/CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		ADC12CLK	0	1	1
		DMAE0	0	0	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

(1) X: Don't care

6.3 P2.5, Input/Output With Schmitt Trigger and External R_{OSC} for DCO

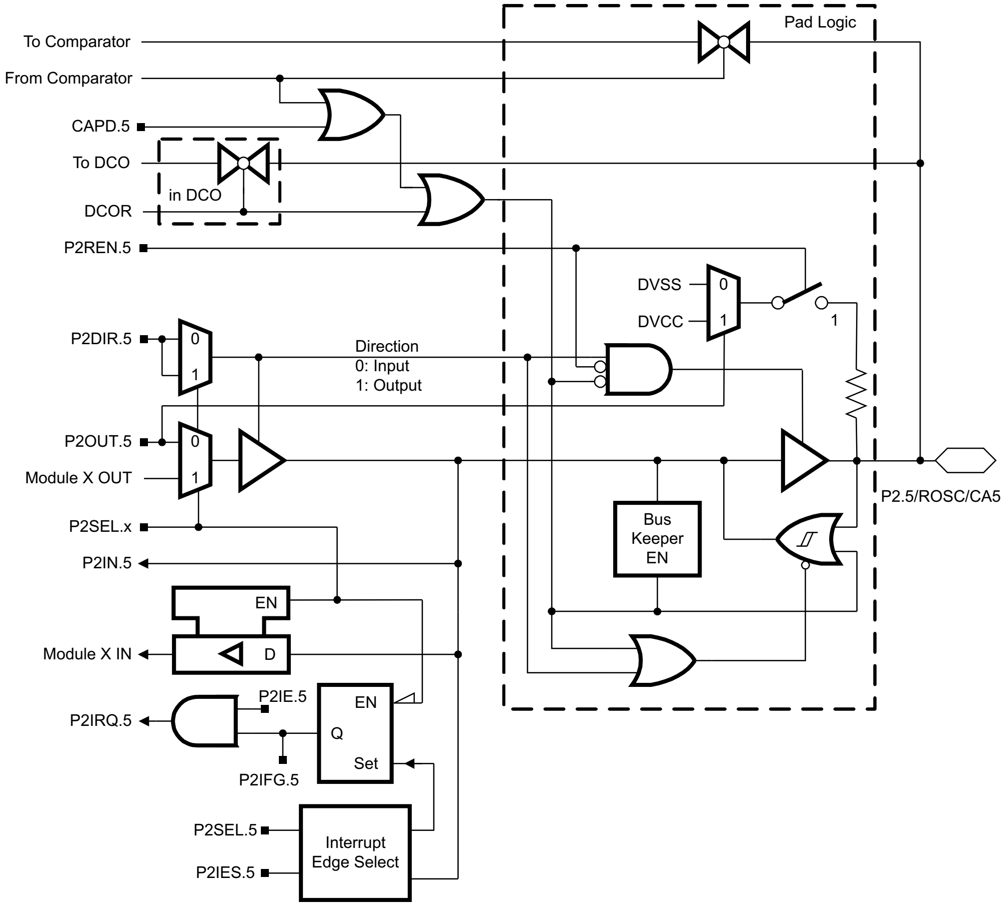


Figure 6-3. Port P2 (P2.5) Pin Schematic

Table 6-3. Port P2 (P2.5) Pin Functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS/SIGNALS[1]			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC} /CA5	5	P2.5 (I/O)	0	0	I: 0; O: 1	0
		R_{OSC} [2]	0	1	X	X
		DV_{SS}	0	0	1	1
		R_{OSC}	1 or selected	0	X	X

(1) X: Don't care
(2) If R_{OSC} is used it is connected to an external resistor.

6.4 Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger

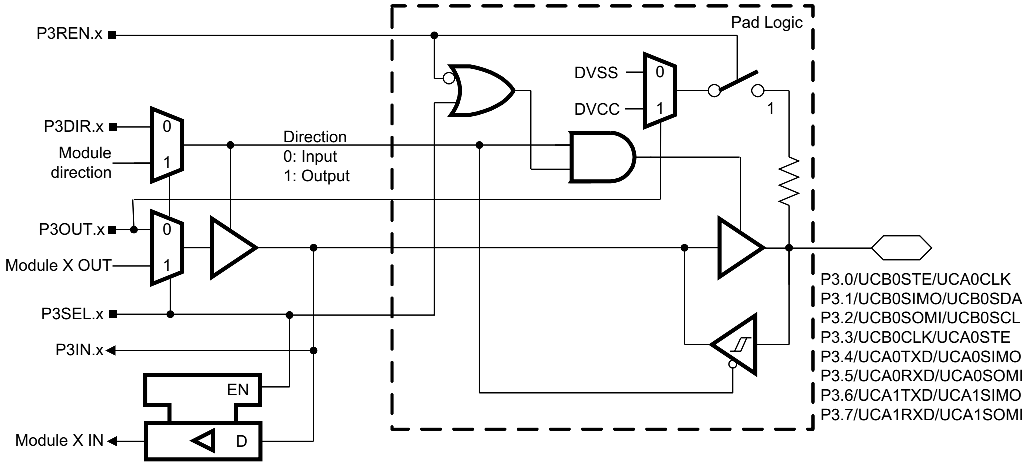


Figure 6-4. Port P3 (P3.0) Pin Schematic

Table 6-4. Port P3 (P3.0) Pin Functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK(2)(3)	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(2)(4)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(2)(4)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(2)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(2)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(2)	X	1
P3.6/UCA1TXD/UCA1SIMO	6	P3.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO(2)	X	1
P3.7/UCA1RXD/UCA1SOMI	7	P3.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI(2)	X	1

(1) X: Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) In case the I^{2}C functionality is selected the output drives only the logical 0 to V_{SS} level.

6.5 Port P4 Pin Schematic: P4.0 to P4.7, Input/Output With Schmitt Trigger

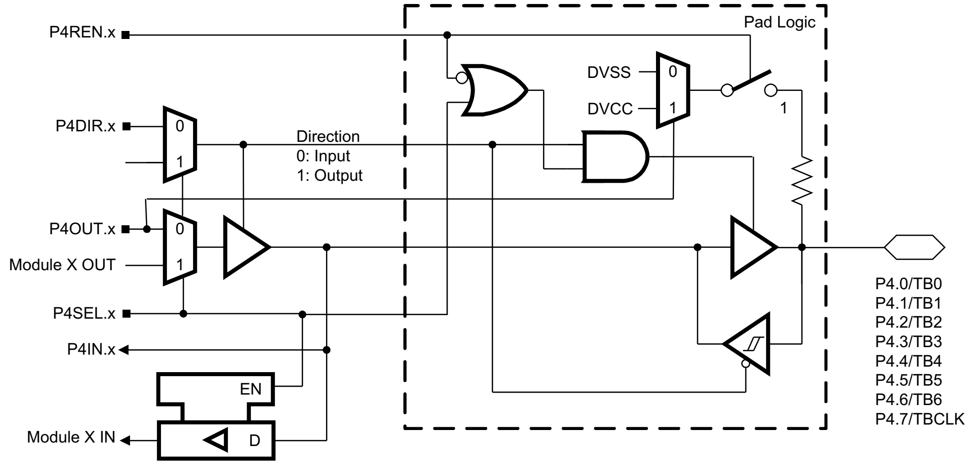


Figure 6-5. Port P4 (P4.0 to P4.7) Pin Schematic

Table 6-5. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3	1	1
P4.4/TB4	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4	1	1
P4.5/TB5	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5	1	1
P4.6/TB6	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	1	1

6.6 Port P5 Pin Schematic: P5.0 to P5.7, Input/Output With Schmitt Trigger

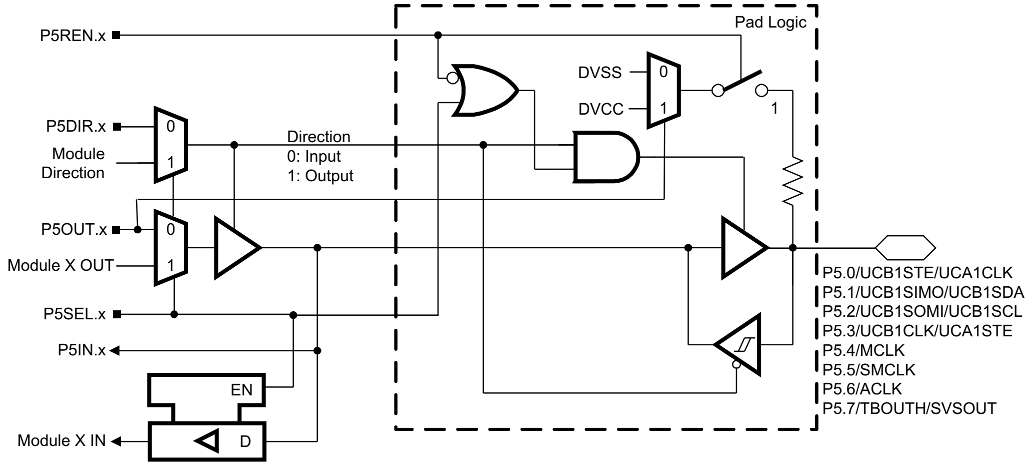


Figure 6-6. Port P5 (P5.0 to P5.7) Pin Schematics

Table 6-6. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/UCB1STE/UCA1CLK	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK(2)(3)	X	1
P5.1/UCB1SIMO/UCB1SDA	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA(2)(4)	X	1
P5.2/UCB1SOMI/UCB1SCL	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL(2)(4)	X	1
P5.3/UCB1CLK/UCA1STE	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE(2)	X	1
P5.4/MCLK	4	P5.0 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P5.5/SMCLK	5	P5.1 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P5.6/ACLK	6	P5.2 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P5.7/TBOUTH/SVSOUT	7	P5.7 (I/O)	I: 0; O: 1	0
		TBOUTH	0	1
		SVSOUT	1	1

(1) X: Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI A1/B1 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) In case the I^2C functionality is selected the output drives only the logical 0 to V_{SS} level.

6.7 Port P6 Pin Schematic: P6.0 to P6.4, Input/Output With Schmitt Trigger

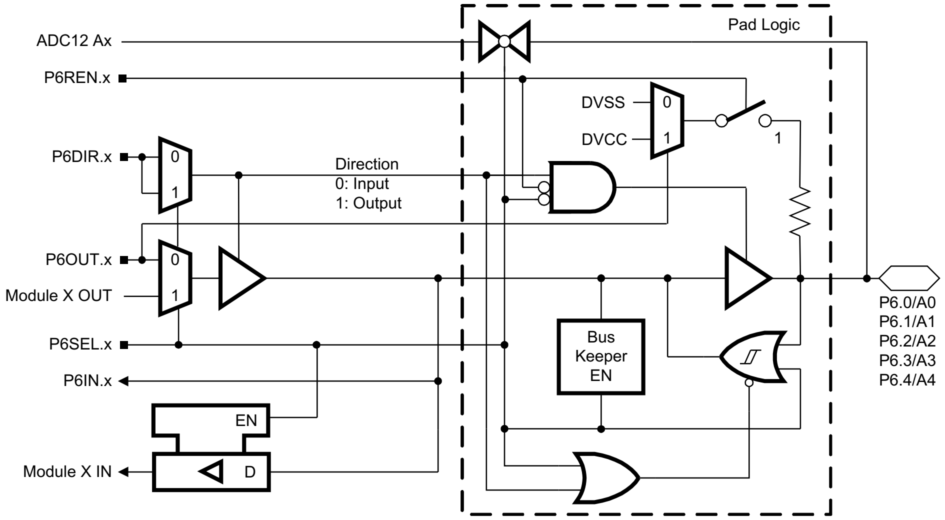


Figure 6-7. Port P6 (P6.0 to P6.4) Pin Schematic

Table 6-7. Port P6 (P6.0 to P6.4) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P6DIR.x	P6SEL.x
P6.0/A0	0	P6.0 (I/O)	I: 0; O: 1	0
		A0[2]	X	X
P6.1/A1	1	P6.1 (I/O)	I: 0; O: 1	0
		A1[2]	X	X
P6.2/A2	2	P6.2 (I/O)	I: 0; O: 1	0
		A2[2]	X	X
P6.3/A3	3	P6.3(I/O)	I: 0; O: 1	0
		A3[2]	X	X
P6.4/A4	4	P6.3 (I/O)	I: 0; O: 1	0
		A4[2]	X	X

(1) X: Don't care
(2) The ADC12 channel Ax is connected to AVss internally if not selected.

6.8 Port P6 Pin Schematic: P6.5 and P6.6, Input/Output With Schmitt Trigger

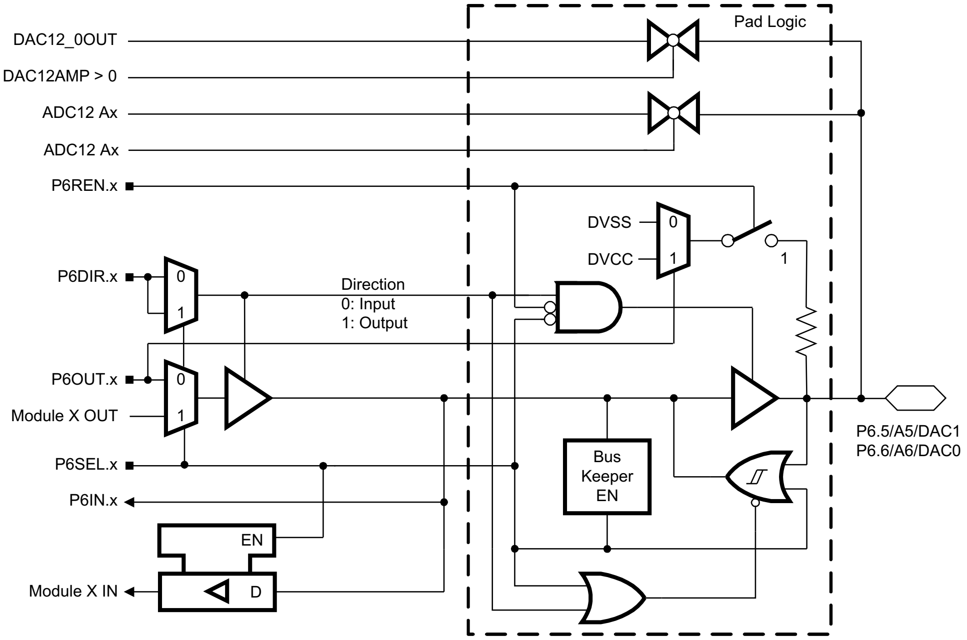


Figure 6-8. Port P6 (P6.5 to P6.6) Pin Schematic

Table 6-8. Port P6 (P6.5 to P6.6) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P6DIR.x	P6SEL.x	CAPD.x or DAC12AMP > 0
P6.5/A5/DAC1	5	P6.5 (I/O)	I: 0; O: 1	0	0
		DV_{SS}	1	1	0
		A5[2]	X	X	1
		DAC1 (DA12OPS = 1)[3]	X	X	1
P6.6/A6/DAC0	6	P6.6 (I/O)	I: 0; O: 1	0	0
		DV_{SS}	1	1	0
		A6[2]	X	X	1
		DAC1 (DA12OPS = 0)[3]	X	X	1

(1) X: Don’t care
(2) The ADC12 channel Ax is connected to AVss internally if not selected.
(3) The DAC outputs are floating if not selected.

6.9 Port P6 Pin Schematic: P6.7, Input/Output With Schmitt Trigger

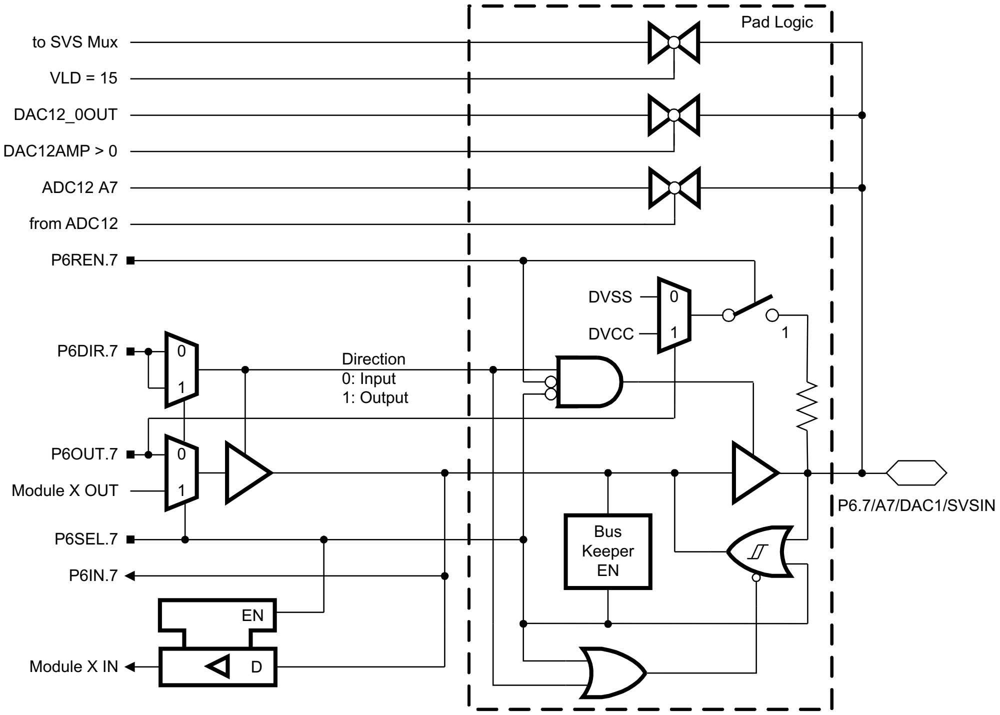


Figure 6-9. Port P6 (P6.7) Pin Schematic

Table 6-9. Port P6 (P6.7) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P6DIR.x	P6SEL.x
P6.7/A7/DAC1/SVSIN	7	P6.7 (I/O)	I: 0; O: 1	0
		DV_{SS}	1	1
		A7[2]	X	X
		DAC1 (DA12OPS = 0)[3]	X	X
		SVSIN (VLD = 15)	X	X

[1] X: Don't care
[2] The ADC12 channel Ax is connected to AVss internally if not selected.
[3] The DAC outputs are floating if not selected.

6.10 Port P7 Pin Schematic: P7.0 to P7.7, Input/Output With Schmitt Trigger

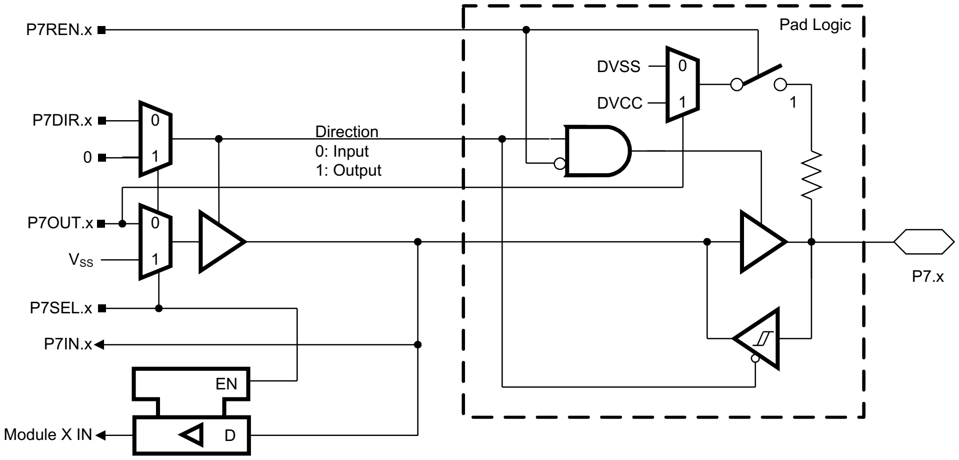


Figure 6-10. Port P7 (P7.0 to P7.7) Pin Schematic

Table 6-10. Port P7 (P7.0 to P7.7) Pin Functions[1]

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P7DIR.x	P7SEL.x
P7.0	0	P7.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.1	1	P7.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.2	2	P7.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.3	3	P7.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.4	4	P7.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.5	5	P7.5 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.6	6	P7.6 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.7	7	P7.7 (I/O)	I: 0; O: 1	0
		Input	X	1

(1) 80-pin KGD only.

6.11 Port P8 Pin Schematic: P8.0 to P8.5, Input/Output With Schmitt Trigger

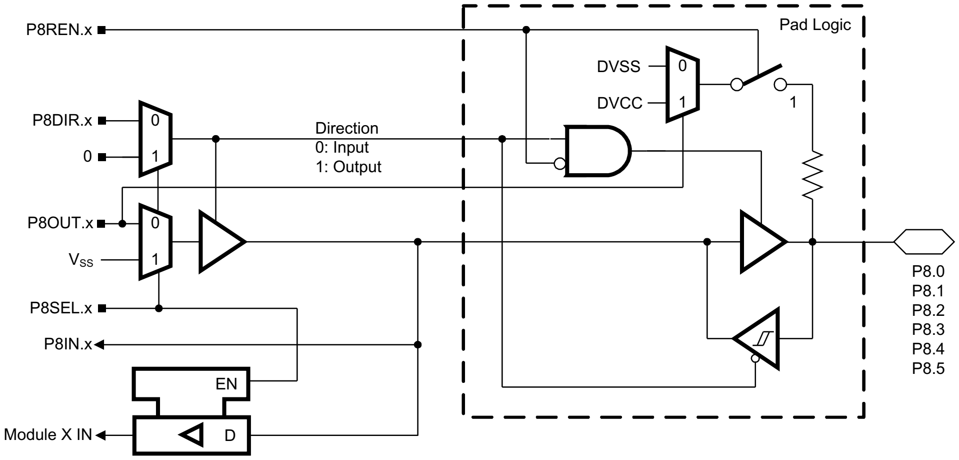


Figure 6-11. Port P8 (P8.0 to P8.5) Pin Schematic

Table 6-11. Port P8 (P8.0 to P8.5) Pin Functions(1)

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.0	0	P8.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.1	1	P8.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.2	2	P8.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.3	3	P8.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.4	4	P8.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.5	5	P8.5 (I/O)	I: 0; O: 1	0
		Input	X	1

(1) 80-pin KGD only.

6.12 Port P8 Pin Schematic: P8.6, Input/Output With Schmitt Trigger

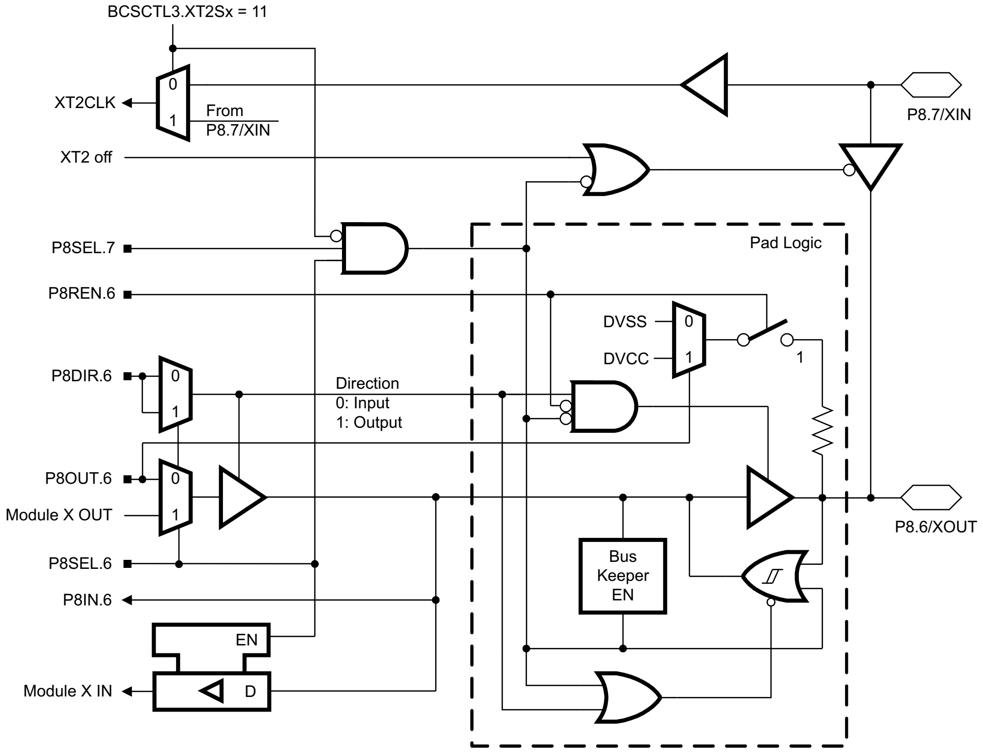


Figure 6-12. Port P8 (P8.6) Pin Schematic

Table 6-12. Port P8 (P8.6) Pin Functions[1]

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.6/XOUT	6	P8.6 (I/O)	I: 0; O: 1	0
		XOUT (default)	0	1
		DV_{SS}	1	1

(1) 80-pin KGD only.

6.13 Port P8 Pin Schematic: P8.7, Input/Output With Schmitt Trigger

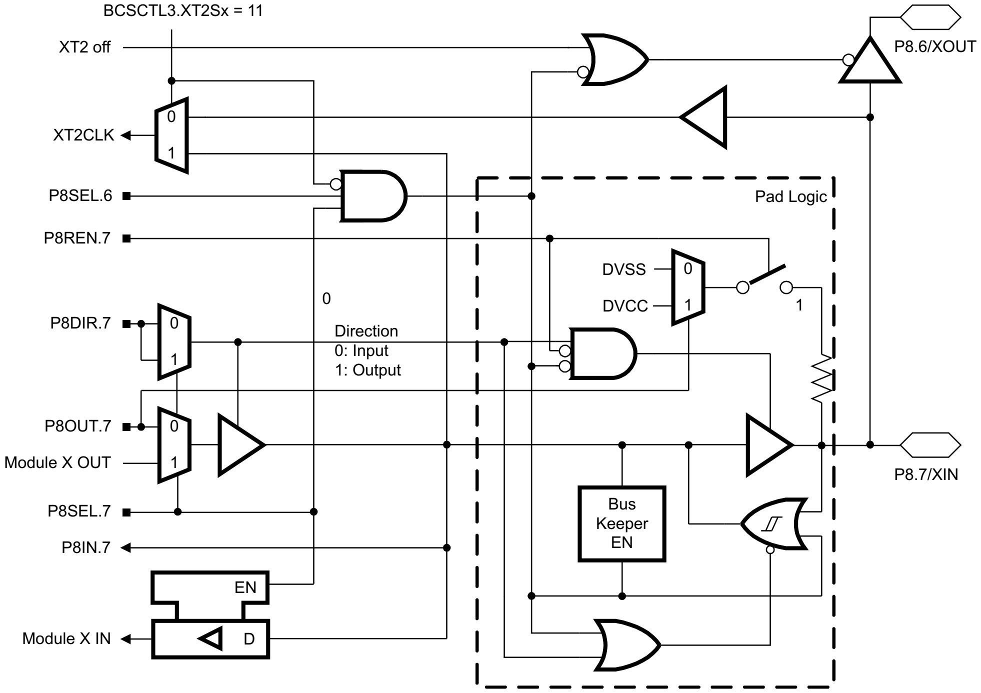


Figure 6-13. Port P8 (P8.7) Pin Schematic

Table 6-13. Port P8 (P8.7) Pin Functions(1)

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.7/XIN	6	P8.7 (I/O)	I: 0; O: 1	0
		XIN (default)	0	1
		V_{SS}	1	1

(1) 80-pin KGD only.

6.14 JTAG Pins: TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger

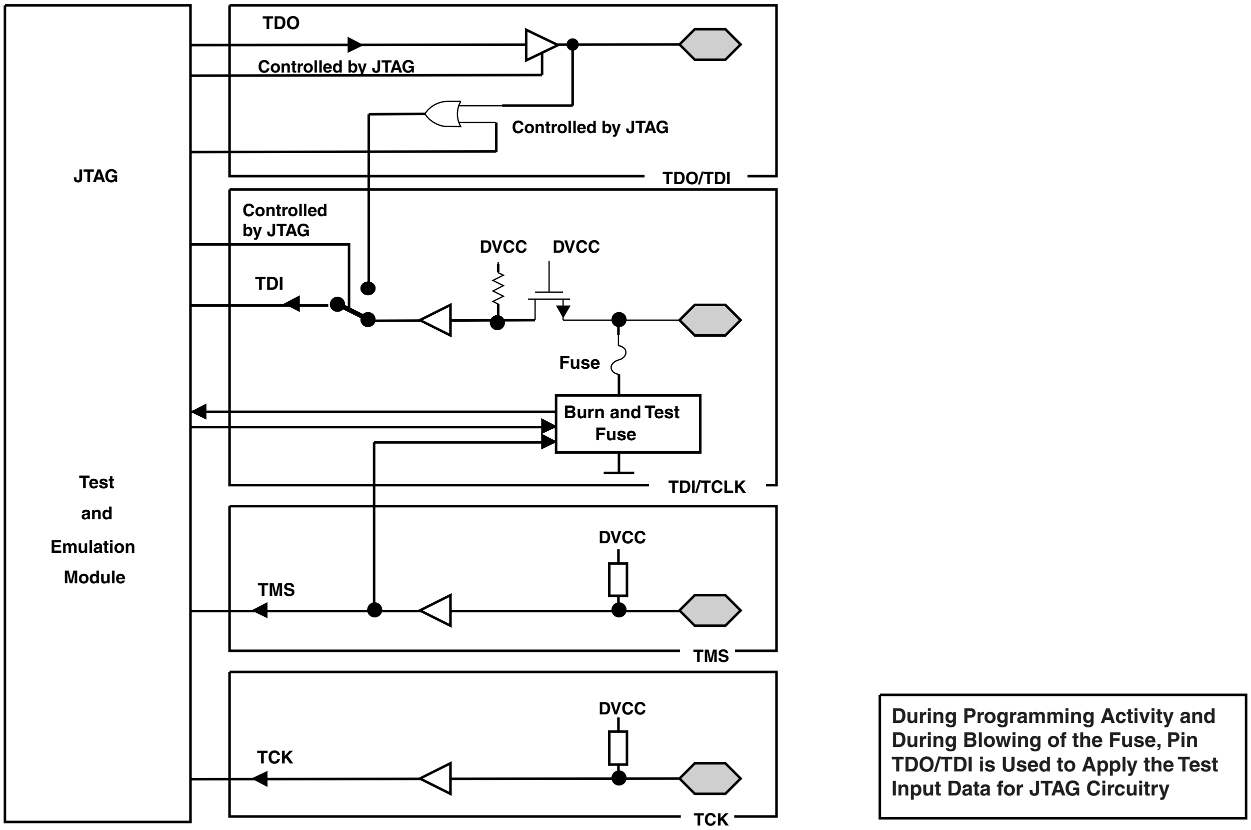


Figure 6-14. JTAG Module

6.15 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-15). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

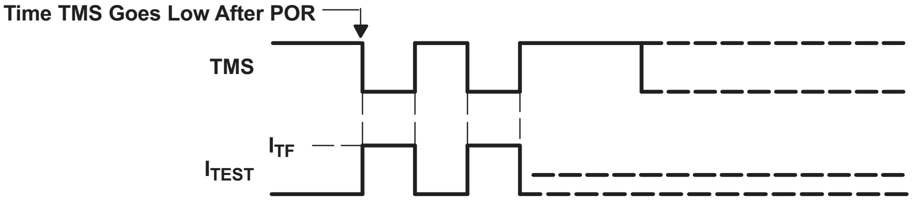


Figure 6-15. Fuse Check Mode Current

7 Device and Documentation Support

7.1 Development Tool Support

All MSP430 microcontrollers include an embedded emulation module (EEM) allowing advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and programming interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (parallel port)
- Debugging and programming interface with target board
  - MSP-FET430U64
  - MSP-FET430U80
- Standalone target board
  - MSP-TS430PM64
- Production programmer
  - MSP-GANG430

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (MSP430F2619S-HT). In the upper right-hand corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-ro-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2619S64KGD1	ACTIVE	XCEPT	KGD	0	36	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 150		Samples
MSP430F2619SKGD1	ACTIVE	XCEPT	KGD	0	36	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 150		Samples
MSP430F2619SPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	M430F2619SPM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

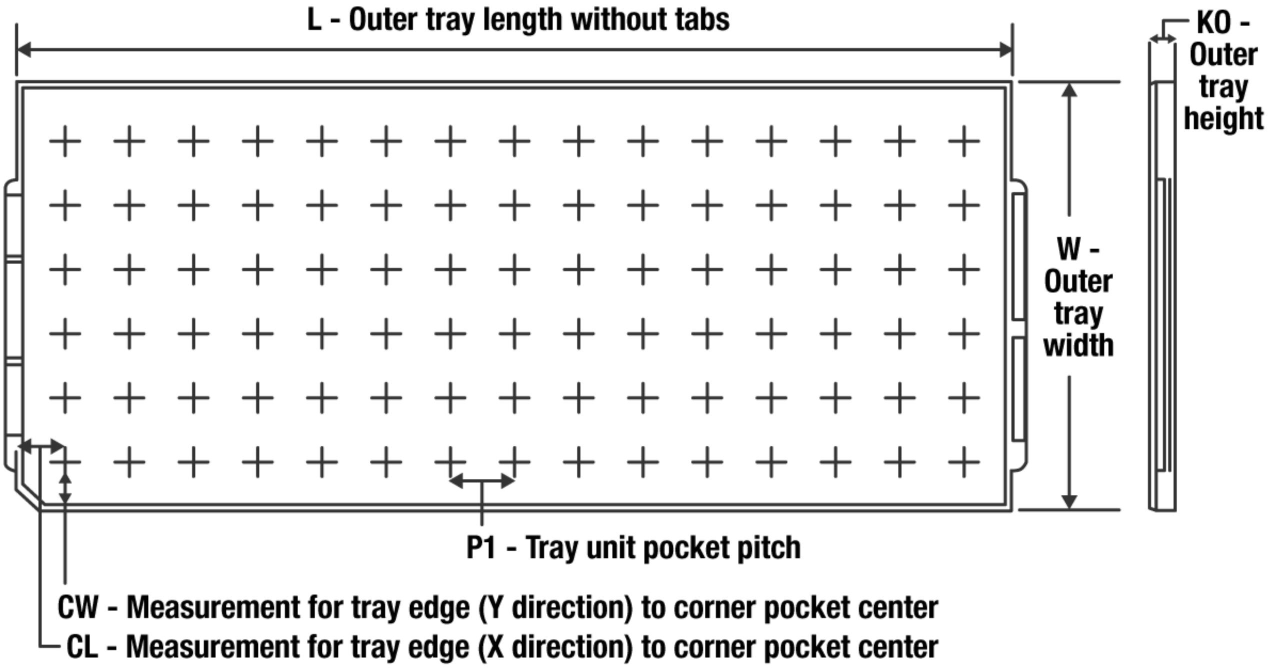
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

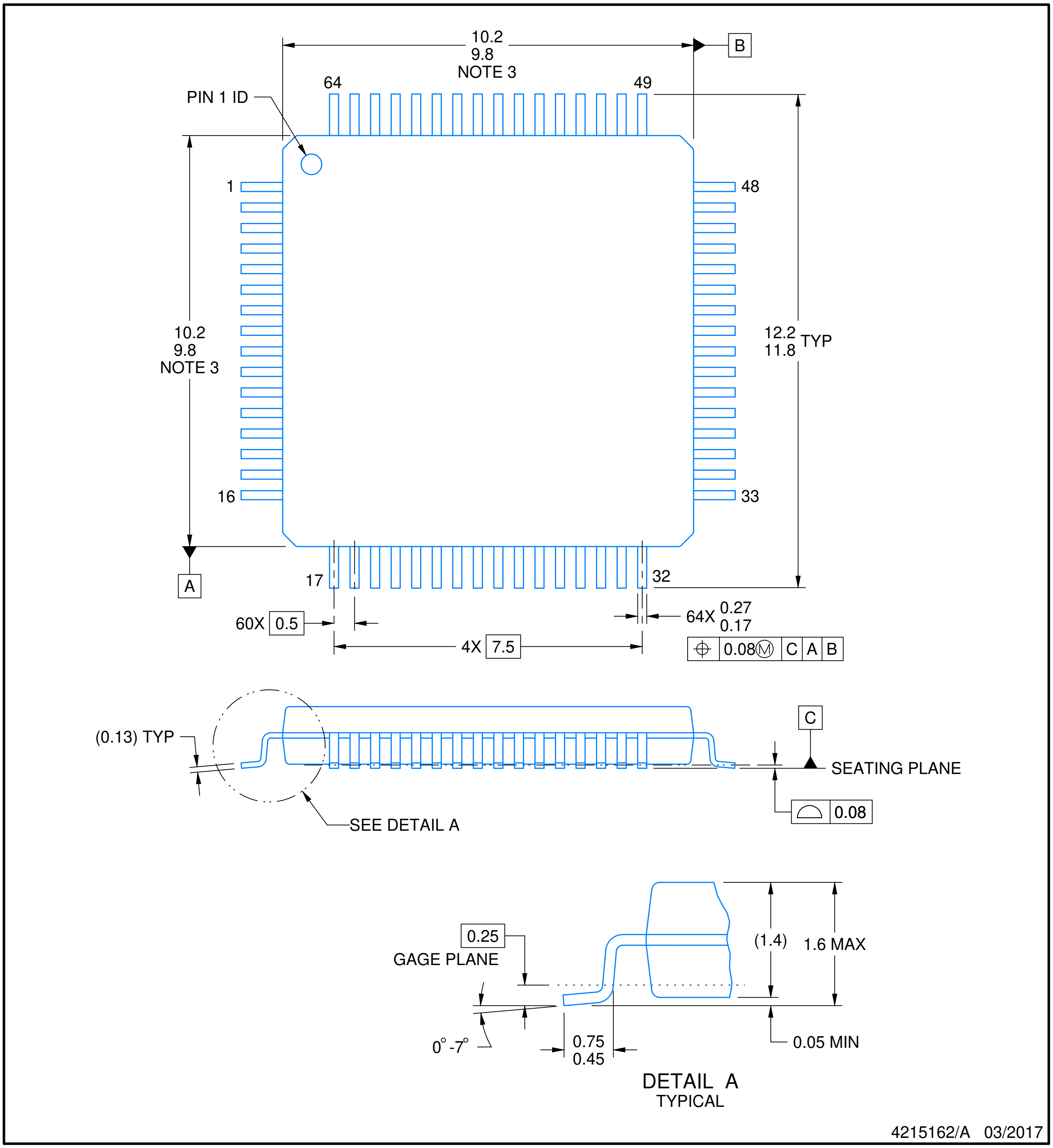
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

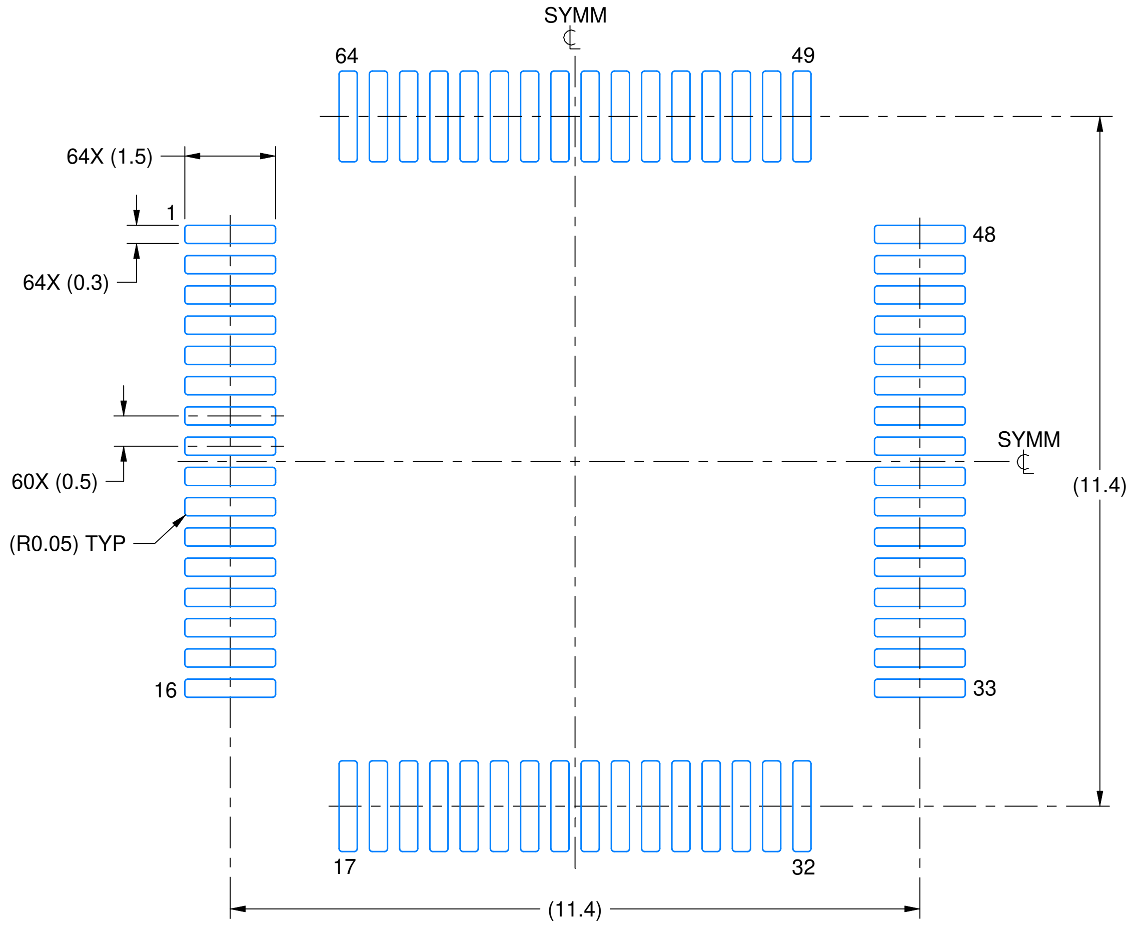
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F2619SPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

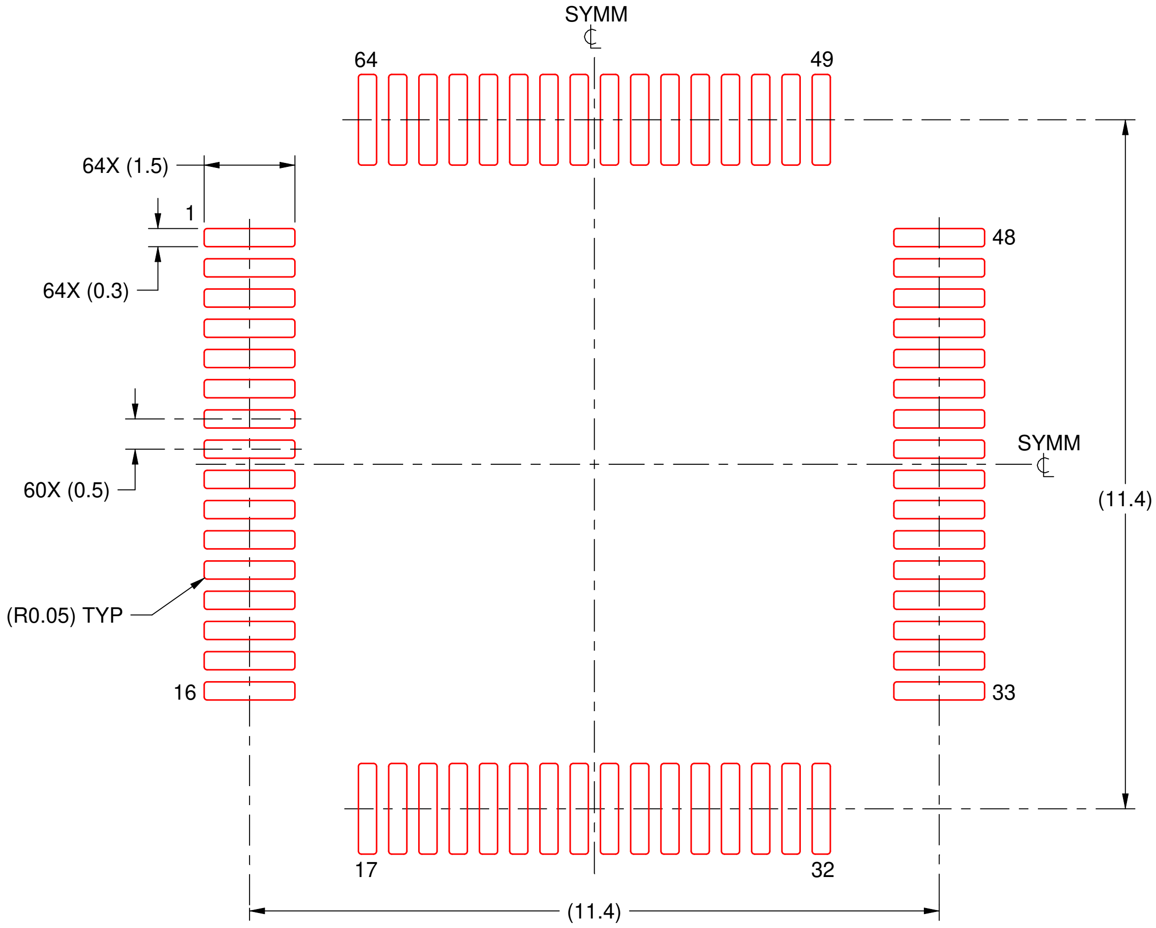


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated