DS3486 Quad RS-422, RS-423 Line Receiver

Check for Samples: DS3486

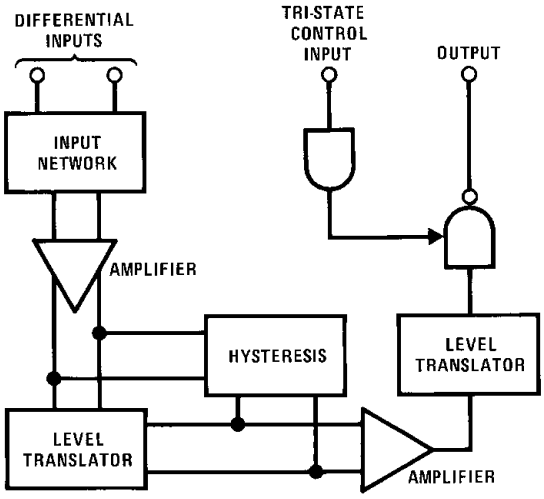
FEATURES

- **Four Independent Receivers**
- **TRI-STATE Outputs**
- **Internal Hysteresis −140 mV (typ)**
- **Fast Propagation Times −19 ns (typ)**
- **TTL Compatible Outputs**
- **5V Supply**
- **Pin Compatible and Interchangeable with MC3486**

DESCRIPTION

Texas Instruments' quad RS-422, RS-423 receiver features four independent receivers which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Block and Connection Diagrams



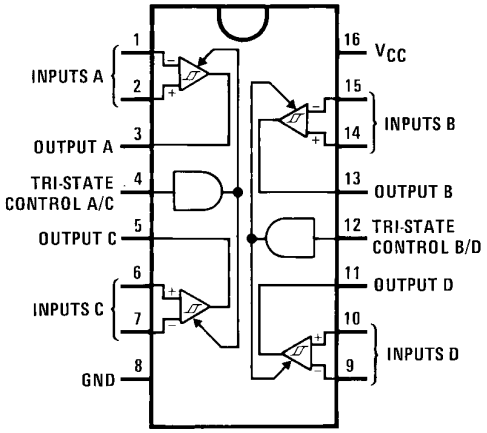


Figure 1. Dual-In-Line Package
Top View
D-16 (SOIC) Package or NFG0016E (PDIP) Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	±25V
Input Differential Voltage, V_{ID}	±25V
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation (3) at 25°C	
Molded PDIP Package	1362 mW
SOIC Package	1002 mW
SOIC Package Thermal Resistance	
θ_{JA}	+124.5°C/W
θ_{JC}	+41.2°C/W

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Derate PDIP molded package 10.2 mW/°C above 25°C. Derate SOIC package 8.01 mW/°C above 25°C.

Operating Conditions

	Max	Min	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage	−7.0	7.0	V
Range, V_{ICR}			

Electrical Characteristics (1)

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V.)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)			2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage		−7V ≤ V_{IC} ≤ 7V, V_{IH} TRI-STATE = 2V I_O = −0.4 mA, V_{OH} ≥ 2.7V		0.070	0.2	V
			I_O = 8 mA, V_{OL} ≥ 0.5V		0.070	−0.2	V
$I_{IB\ (D)}$	Input Bias Current		V_{CC} = 0V or 5.25V, Other Inputs at 0V				
			V_I = −10V			−3.25	mA
			V_I = −3V			−1.50	mA
			V_I = 3V			1.50	mA
			V_I = 10V			3.25	mA
	Input Balance		−7V ≤ V_{IC} ≤ 7V, $V_{IH(3C)}$ = 2V, (2)				
		V_{OH}	I_O = −0.4 mA, V_{ID} = 0.4V	2.7			V
		V_{OL}	I_O = 8 mA, V_{ID} = −0.4V			0.5	V

(1) All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
(2) Refer to EIA RS-422/3 for exact conditions.

Electrical Characteristics [1] (continued)

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)}$ = 3V, V_{IL} = 0.8V, V_{OL} = 0.5V			−40	µA
		$V_{I(D)}$ = −3V, V_{IL} = 0.8V, V_{OH} = 2.7V			40	µA
I_{OS}	Output Short-Circuit Current	$V_{I(D)}$ = 3V, V_{IH}TRI-STATE = 2V,	−15		−100	mA
		V_O = 0V, [3]				
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)	V_{IL} = 0.5V			−100	µA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)	V_{IH} = 2.7V			20	µA
		V_{IH} = 5.25V			100	µA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	I_{IN} = −10 mA			−1.5	V
I_{CC}	Power Supply Current	All Inputs V_{IL} = 0V			85	mA

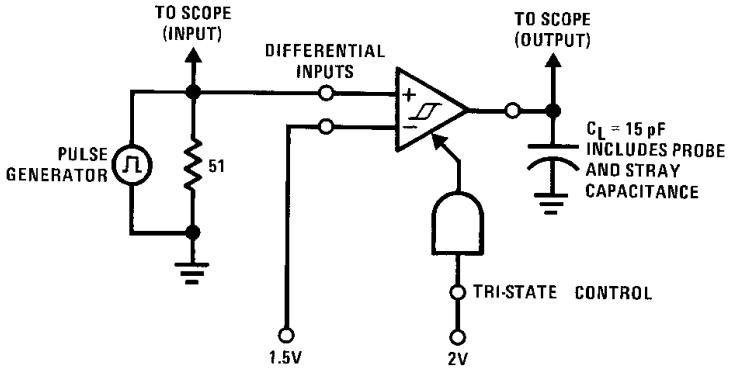
(3) Only one output at a time should be shorted.

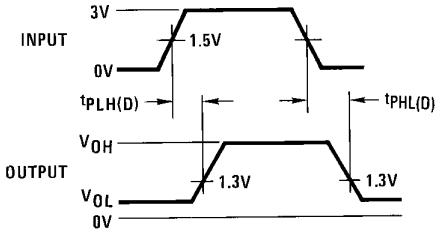
Switching Characteristics

(Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

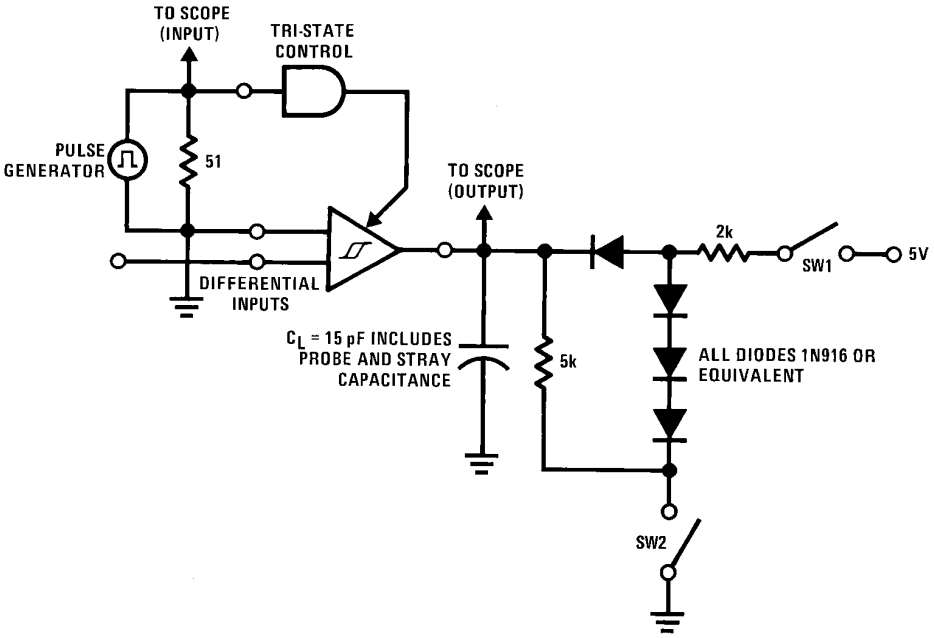
AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



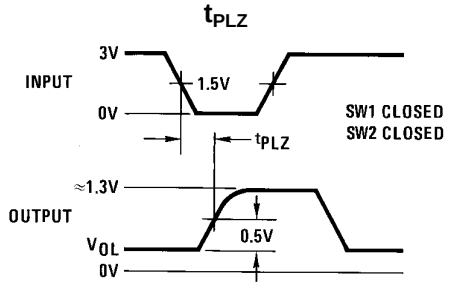


Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

Figure 2. Propagation Delay Differential Input to Output



1.5V for t_{PHZ} and t_{PLZ}
1.5V for t_{PLZ} and t_{PZL}
Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle



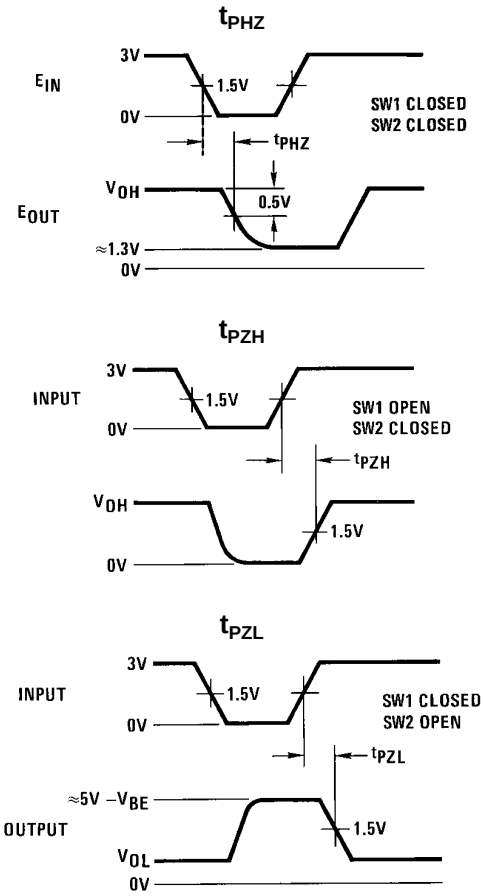


Figure 3. Propagation Delay TRI-STATE Control Input to Output

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3486M	LIFEBUY	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DS3486M	
DS3486M/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3486M	Samples
DS3486MX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3486M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

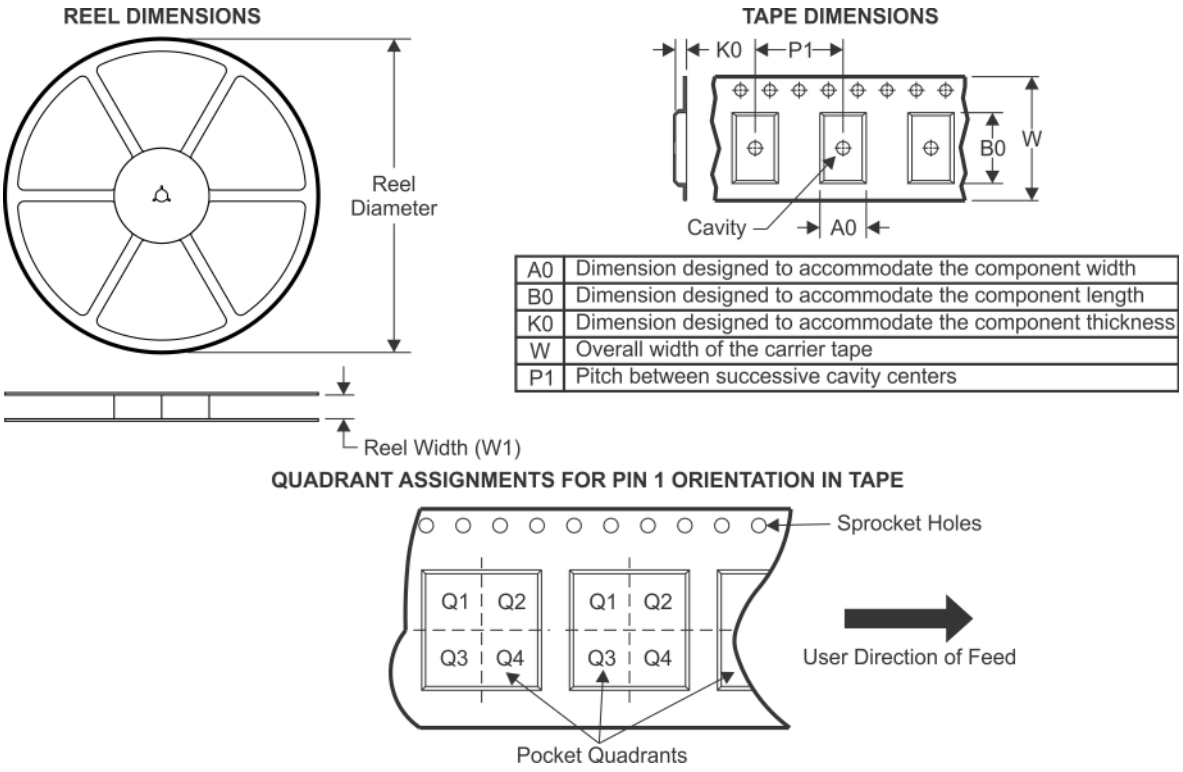
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

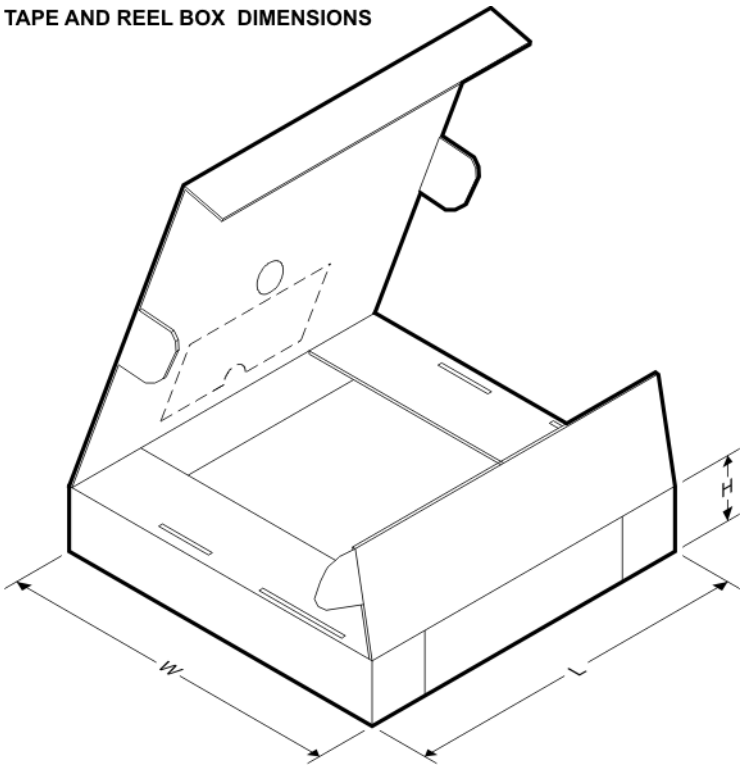


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3486MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

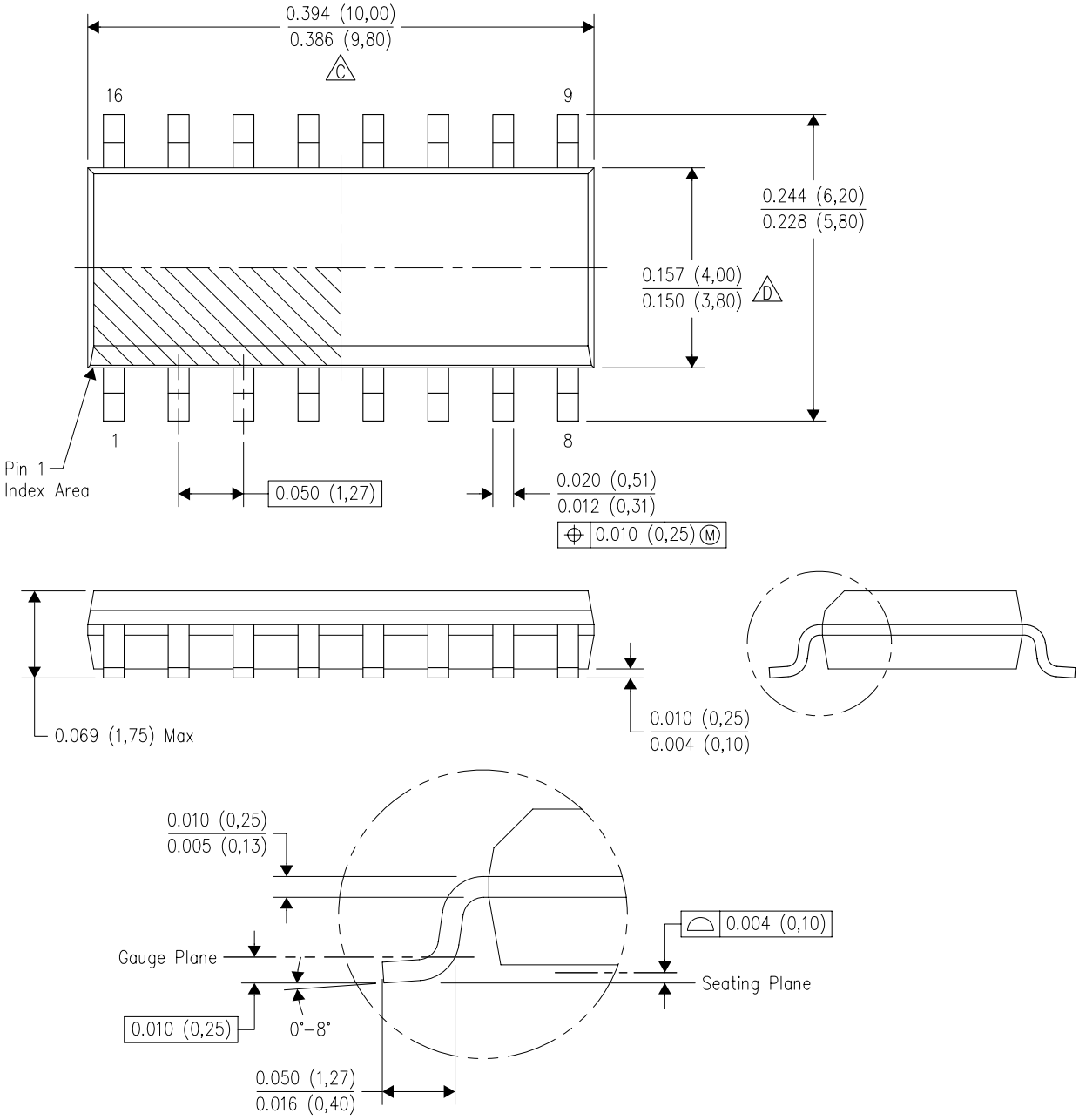
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3486MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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