# RD2-4020

# DisplayPort to Quad-LVDS Output

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# 1. Purpose and scope

This document provides description and setup instructions for the DisplayPort™ Receiver STDP4020 reference design board [RD2-4020_400-534] targeted for DisplayPort to LVDS conversion applications.

# 2. Description

The STDP4020 is an integrated circuit featuring a four lane DisplayPort receiver, quad LVDS & LVTTL transmitter with I2S and SPDIF audio outputs for digital audio-video conversion application. This device also includes SPI interface, I2C Slave (Host Interface), I2C Master Interface, UART (GProbe) interface, and general-purpose IO pins. The RD2-4020 is a low cost compact four layer board that includes necessary interfaces and features to fully demonstrate the STDP4020 receiver functionalities. This reference design meets the following:

1. Stand-alone operation: Includes necessary firmware (either IROM or external SPI) to work independently; this means the intended functionalities are performed without depending on external (Host) controllers.
2. Slave configuration: Provision to configure the device by an external Host controller through the Host Interface to I2C (most likely when no SPI Flash is used).

## 2.1. Set Up Instructions

The picture below is a connection diagram showing the RD2-4020 board used for transferring a PC DisplayPort signal into a quad channel LVDS output. This board uses the standard DisplayPort connector recommended in the DP specification to connect the DisplayPort output of a PC or equivalent source device and a quad channel LVDS output connector to connect to a commercial LVDS display or external circuit board that can receive quad LVDS signals.
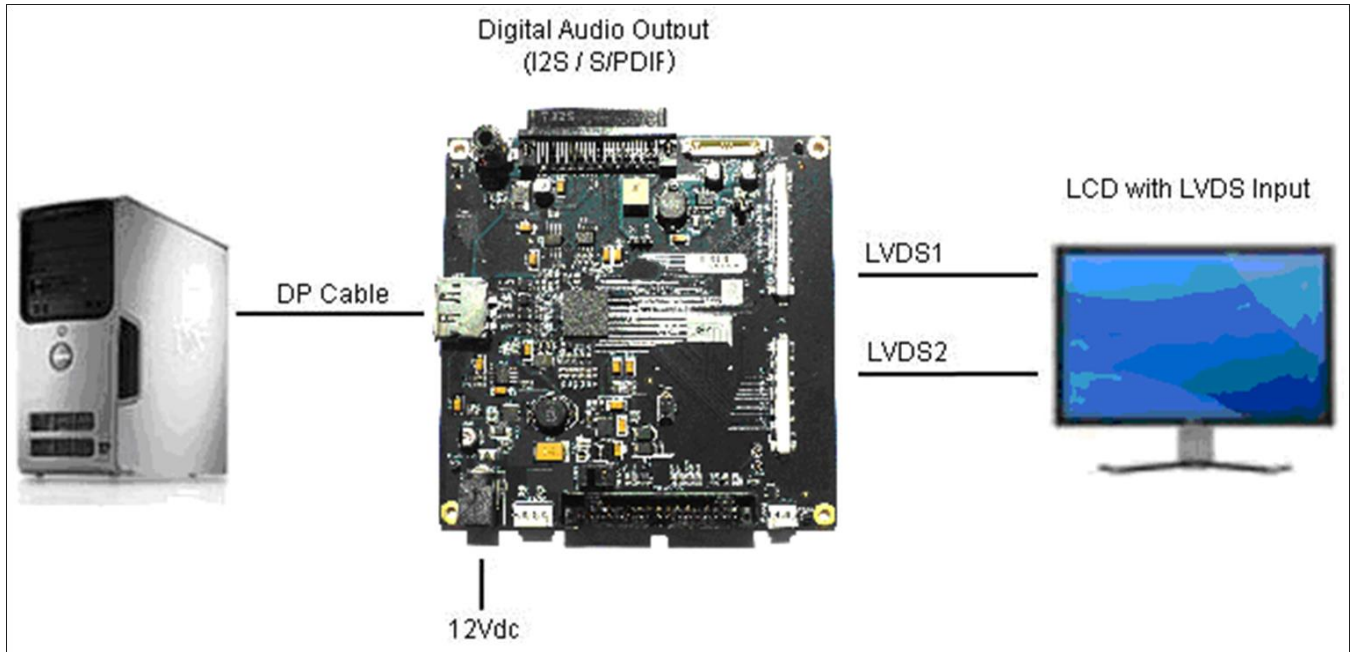
**Figure 1. Connection Diagram: PC DP Signal to LVDS Stream**

*Note:* *The LVDS output is also configurable as dual channel or single channel, depending on the use cases.*

1.  Connect the DisplayPort output from a PC source to the RD2-4020 reference board using a DP cable (not provided with board).

2.  Connect the output to an LVDS panel using LVDS cable (typically provided quad/dual channel cable, depending on order type). Quad channel contains two cables (51 pin and 41 pin connector type) and dual/single channel has single cable (41 pin connector).

3.  Connect the 12 V (4A) DC power brick (supplied with board) for powering the board.

4.  Connect an SPDIF audio cable (not provided) to connect the audio out from the board to an external speaker or audio processor board. You can also order an audio processor board at Kinetic for evaluating SPDIF or I2S (2 Ch) audio from the RD2-4020 board. A DisplayPort PC source that supports DP-Audio is required for evaluating digital audio output of the RD2-4020 board.

5.  Once the connection is established, power ON the PC, LVDS display, and the RD2-4020 (DP receiver) board. An image should pop up on the screen and you should hear the audio within 5-6 seconds.

*Note:* *The default configuration is quad channel LVDS video output and SPDIF audio out. For dual channel LVDS output, change the bootstrap setting Boot[5] to GND (populate R609 and remove 608). STDP4020 register setting changes are required in order to transmit audio on I2S output. This can be done through I2C host configuration or through firmware changes.*

The RD2-4020 supports video resolution from 640 x 480 up to 2560 x 1600 and audio up to 8 Ch.

## 2.1.1. I2C Host Port

Host connector (CN4010) allows configuration of the STDP4020 IC from an external host (microcontroller) through conventional I2C interface. User can plug two wires into pin 5 and pin 6 of this connector to access

the I2C port of the chip. STDP4020 default device ID is 0xE6/0xE7, but can be changed through bootstrap settings. Refer to the STDP4020 datasheet for further details.

## 2.1.2. In-System Programming (ISP)

RD2-4020 uses SPI Flash to store the firmware. In case of a new firmware upgrade, one of the following methods can be used.

1. ISP through DisplayPort connector: Allows programming the SPI Flash through DisplayPort input connector. Requires DP ISP board and GProbe software tool (contact Kinetic).
2. ISP through UART connector: Allows programming the SPI Flash through UART (RS232) connector. Requires GProbe board (RS232 converter circuit) and GProbe software tool (contact Kinetic).

## 2.1.3. Diagnosis

If the image does not come up, follow the steps below for diagnosis.

*Note:   The diagnosis requires the Kinetic GProbe software and hardware tool. Contact Kinetic for the GProbe software and board.*

1. Install the GProbe diagnostic tool on a computer and set the baud rate to 115,200.
2. Connect GProbe board (not supplied) to the serial port (or USB port if using USB version) of the computer.
3. Connect the other end of the GProbe board to connector (CN403 UART port) on the RD2-4020 board using 4-wire cable (part of the GProbe board).

*Note:   CHECK POLARITY while connecting the cable; Pin 1 is marked on the board. The 4-wire cable connection from CN403 to GProbe board is 1 to 1.*

4. Hit the Reset button on the RD2-4020 board (RESET SW402). You will see the firmware version and date of firmware in the GProbe window. This indicates the DP receiver IC is functional. If the message does not appear, reprogram the Flash using the ISP method described in the GProbe user guide.
5. Using an oscilloscope, check the video input and output from the STDP4020.

*Note:   Refer to the STDP4020 datasheet for pin out descriptions.*
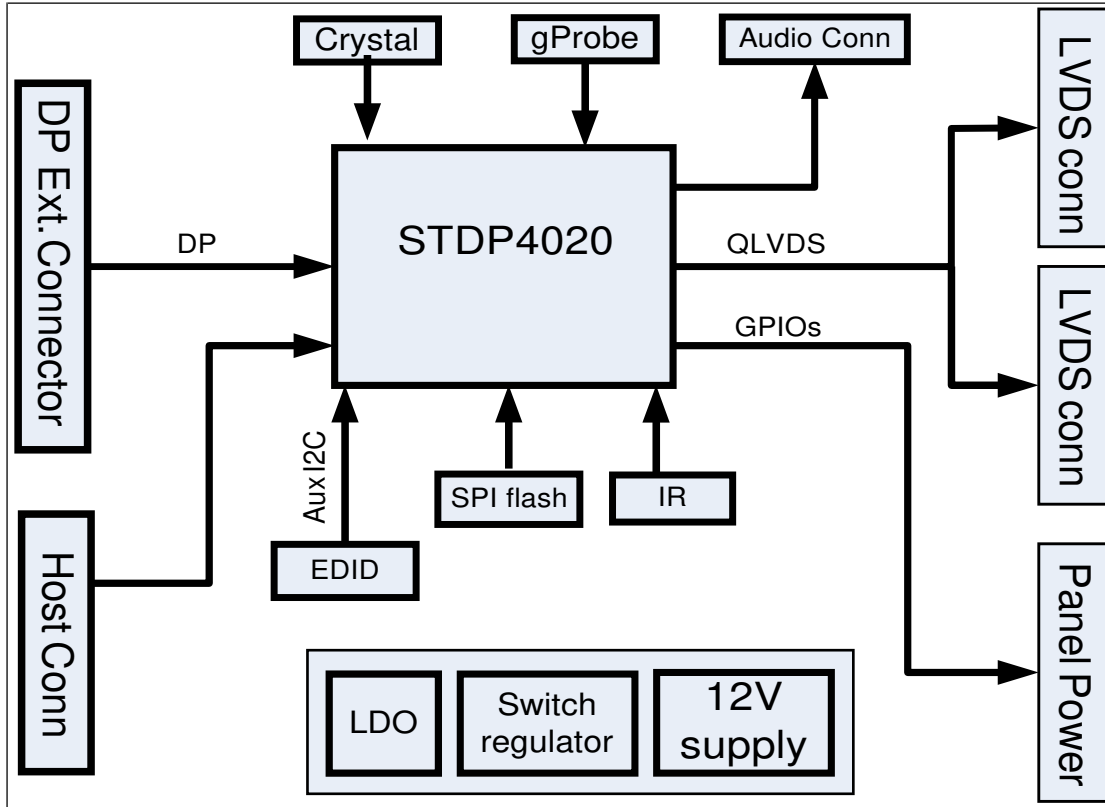
## 3. Board Description
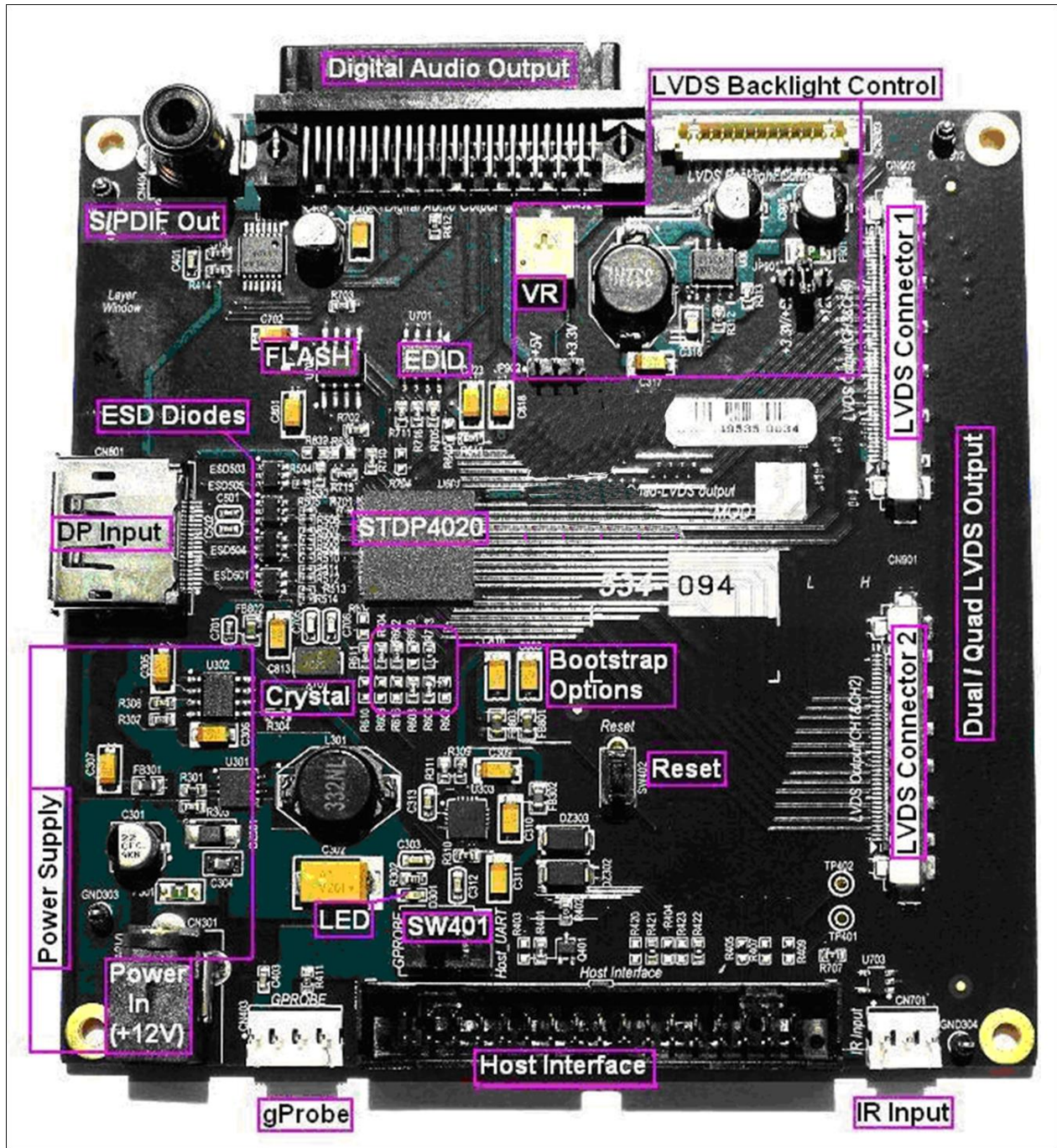


**Figure 2. Block Diagram**

**Figure 3. Board Picture**

## 3.1. Principal Components and Functions

Below is a summary of all necessary connectors, switches, and other components. Please refer to the latest board schematics for further details.

**Table 3.1-1. Principal Components and Functions**

| Label | Description | RefDes |
|---|---|---|
| Power Input (+12V) | Input 12 V, down conversion to 5 V, 3.3 V, and 1.2 V. This board uses a switch regulator for 5 V and an LDO [**low- dropout**] for 3.3 V and 1.2 V. Note the analog and digital supplies (3.3A and 3.3D or 1.2A and 1.2D) are isolated using ferrite beads. | CN301 |
| STDP4020 | The STDP4020 is capable of receiving and converting DisplayPort signals into Quad LVDS output up to 400 MHz pixel rate with flexible channel and lane swapping options. The STDP4020 supports RGB and YCC video color formats with color depth of 12 (YCC 4:2:2 only), 10, and 8 bits. | U601C |
| DP Input | DisplayPort Receiver | CN501 |
| Flash | The board includes an SPI Flash of 2 MB to hold the firmware. The SPI Flash can be programmed (ISP) through DP AUX Channel or through UART interface. | U702 |
| Dual/Quad LVDS Output | The RD2-4020 features two LVDS output connectors for Quad or Dual LVDS outputs. Connector1: 902 (51 pin), Connector2: 901 (41 pin) | CN901 CN902 |
| LVDS Backlight Control | LVDS Backlight control | CN903 |
| VR | Brightness manual adjustment. | VR901 |
| Digital Audio Output | Digital Audio Output [S/PDIF, I2S]: This board supports both compressed and uncompressed audio formats. The extracted audio signal is transferred on a digital audio output bus. This device comprises four I2S audio output ports supporting up to eight channel LPCM audio and a single wire SPDIF output for encoded audio. | CN402 |
| S/PDIF out | Standard S/PDIF output | CN404 |
| Host Interface | Host Interface (I2C): This board includes a provision to access the STDP4020 device from an external host controller through the Host Interface (I2C port) connection. | CN401 |
| GProbe | GProbe Interface (+3.3V logic): The board also includes a GProbe connector that connects to the STDP4020 UART port for communication with external PC sources for debug purposes. The Kinetic GProbe tool (software) and PC serial port interface board together create a debug environment for device debug and firmware update. The GProbe interface is also used for ISP purposes. | CN403 |
| Reset | Reset Button, when pressed, triggers a system master reset through the internal reset circuitry. The reset button is used for system reset and debug purposes and is not required for production board design as the STDP4020 produces an internal reset during power ON. | SW402 |
| IR Input | An IR connector for interfacing the IR receiver | CN701 |
| LED | Single LED for indicating the power on status. | D301 |
| Crystal | An external crystal of 27 MHz. The design makes use of internal oscillator circuitry. | X701 |
| ESD Diodes | ESD protection diodes for DisplayPort signal (main lanes, AUX and HPD line). The board implements low cost ESD diodes. | ESD501 ESD503 ESD504 ESD505 |
| EDID | EDID Option: Currently not populated, to allow pass through. | U701 |
| SW401 | Switches UART between Host Interface & GProbe Interface | SW401 |
| Bootstrap Options | The bootstrap options can be configured for:<br>– Dual/Quad LVDS<br>– IROM/SPI Flash<br>Refer to section 4.4 for more details | R606 R607 R608 R609 |
| Backlight Control | Select output signal voltage, +3.3V or +5V (see mark on PCB). | JP903 |

## 3.2. Connector descriptions

The RD2-4020 has the following connectors.

**CN301** – +12V DC 4A Power Input Jack

**CN403** – GProbe Interface (4x1 pin keyed header) connects to the UART port of the STDP4020. Use Kinetic GProbe board and interface cable for connecting the board to an external PC that has GProbe software running.

| Pin 1 | +5V |
|-------|-----|
| Pin 2 | GPROBE_TX |
| Pin 3 | GPROBE_RX |
| Pin 4 | GND |

**CN401** – I2C Host Interface (header 17X2) connector for connecting external host (microcontroller). This is used only when an external host controller accesses the DisplayPort receiver; not used for normal operation. In normal operation, internal MCU controls the overall functioning of the DisplayPort receiver (refer to the schematics for complete pin description for the Host Interface).

| Pin 1 | +5V |
|-------|-----|
| Pin 2 | +5V |
| Pin 3 | GND |
| Pin 4 | GND |
| Pin 5 | I2C_SCL |
| Pin 6 | I2C_SDA |
| Pin 7 | HOST_Tx |
| Pin 8 | HOST_Rx |
| Pin 9 | RESET from Host |
| Pin 10 | NC |
| Pin 11 | GND |
| Pin 12 | GND |
| Pin 13 | AUX_UART_TX |
| Pin 14 | AUX_UART_RX |
| Pin 15 | AUX_I2C_SCL |
| Pin 16 | AUX_I2C_SDA |
| Pin 17 | NC |
| Pin 18 | NC |
| Pin 19 | GND |
| Pin 20 | GND |
| Pin 21 | NC |
| Pin 22 | NC |
| Pin 23 | IRQ/LCD_CN |
| Pin 24 | IR_IN |
| Pin 25 | I2C_MST_SCL |
| Pin 26 | I2C_MST_SDA |
| Pin 27 | GND |
| Pin 28 | GND |
| Pin 29 | LCD_POWER |
| Pin 30 | MST |
| Pin 31 | TP401 |
| Pin 32 | ODC_EN |
| Pin 33 | TP402 |
| Pin 34 | FPS_DET |

**CN402** – I2S Digital Audio Output (52 pin) connector.

| | |
|---|---|
| **Pin A1** | NC |
| **Pin A2 & A3** | GND |
| **Pin A4 through A6** | NC |
| **Pin A7** | GND |
| **Pin A8 & A9** | NC |
| **Pin A10** | I2S_3 |
| **Pin A11** | I2S_2 |
| **Pin A12** | I2S_1 |
| **Pin A13** | NC |
| **Pin A14** | I2S_0 |
| **Pin A15** | I2S_0 |
| **Pin A16 & A17** | GND |
| **Pin A18** | I2S_MCLK |
| **Pin A19 through A21** | NC |
| **Pin A22** | I2S_BCLK |
| **Pin A23** | +5V |
| **Pin A24** | I2S_WCLK |
| **Pin A25** | +5V |
| **Pin A26** | +5V |
| **Pin B1** | GND |
| **Pin B2 & B3** | NC |
| **Pin B4 & B5** | GND |
| **Pin B6 & B7** | NC |
| **Pin B8 & B9** | GND |
| **Pin B10 through B13** | NC |
| **Pin B14 & B15** | GND |
| **Pin B16 through B18** | NC |
| **Pin B19 & B20** | GND |
| **Pin B21** | +5V |
| **Pin B22** | NC |
| **Pin B23** | +5V |
| **Pin B24** | NC |
| **Pin B25** | +5V |
| **Pin B26** | GND |

**CN404** – S/PDIF Output

| Pin 1 | GND |
|-------|-----|
| **Pin 2** | I2S_0 |
| **Pin 3** | GND |

**CN501** – DisplayPort Receiver MOLEX 47272-0002 connector and pin out details.

| Pin 1 | ML_L3N |
|-------|--------|
| **Pin 2** | GND |
| **Pin 3** | ML_L3P |
| **Pin 4** | ML_L2N |
| **Pin 5** | GND |
| **Pin 6** | ML_L2P |
| **Pin 7** | ML_L1N |
| **Pin 8** | GND |
| **Pin 9** | ML_L1P |
| **Pin 10** | ML_L0N |
| **Pin 11** | GND |
| **Pin 12** | ML_L0P |
| **Pin 13** | GND |
| **Pin 14** | GND |
| **Pin 15** | AUX_P |
| **Pin 16** | GND |
| **Pin 17** | AUX_N |
| **Pin 18** | HPD_OUT |
| **Pin 19** | GND |
| **Pin 20** | +3V3_AVDD |

**CN901 & CN902** – Quad/Dual LVDS output (refer to the schematics for complete pin out details)

**CN901 [LVDS Connector2]**

| | |
|---|---|
| **Pin 1** | GND |
| **Pin 2** | GND |
| **Pin 3** | LVDS_45P |
| **Pin 4** | LVDS_45N |
| **Pin 5** | LVDS_44P |
| **Pin 6** | LVDS_44N |
| **Pin 7** | GND |
| **Pin 8** | LVDS_CLK4P |
| **Pin 9** | LVDS_CLK4N |
| **Pin 10** | GND |
| **Pin 11** | LVDS_43P |
| **Pin 12** | LVDS_43N |
| **Pin 13** | LVDS_42P |
| **Pin 14** | LVDS_42N |
| **Pin 15** | LVDS_41P |
| **Pin 16** | LVDS_41N |
| **Pin 17** | GND |
| **Pin 18** | GND |
| **Pin 19** | LVDS_35P |
| **Pin 20** | LVDS_35N |
| **Pin 21** | LVDS_34P |
| **Pin 22** | LVDS_34N |
| **Pin 23** | GND |
| **Pin 24** | LVDS_CLK3P |
| **Pin 25** | LVDS_CLK3N |
| **Pin 26** | GND |
| **Pin 27** | LVDS_33P |
| **Pin 28** | LVDS_33N |
| **Pin 29** | LVDS_32P |
| **Pin 30** | LVDS_32N |
| **Pin 31** | LVDS_31P |
| **Pin 32** | LVDS_31N |
| **Pin 33** | GND |
| **Pin 34** | NC |
| **Pin 35** | NC |
| **Pin 36** | NC |
| **Pin 37** | NC |
| **Pin 38** | NC |
| **Pin 39** | NC |
| **Pin 40** | NC |
| **Pin 41** | NC |

**CN902** [LVDS Connector1]

| | |
|---|---|
| **Pin 1** | GND |
| **Pin 2** | GND |
| **Pin 3** | GND |
| **Pin 4** | GND |
| **Pin 5** | NC |
| **Pin 6** | GND |
| **Pin 7** | GND |
| **Pin 8** | GND |
| **Pin 9** | GND |
| **Pin 10** | GND |
| **Pin 11** | LVDS_25P |
| **Pin 12** | LVDS_25N |
| **Pin 13** | LVDS_24P |
| **Pin 14** | LVDS_24N |
| **Pin 15** | GND |
| **Pin 16** | LVDS_CLK2P |
| **Pin 17** | LVDS_CLK2N |
| **Pin 18** | GND |
| **Pin 19** | LVDS_23P |
| **Pin 20** | LVDS_23N |
| **Pin 21** | LVDS_22P |
| **Pin 22** | LVDS_22N |
| **Pin 23** | LVDS_21P |
| **Pin 24** | LVDS_21N |
| **Pin 25** | GND |
| **Pin 26** | GND |
| **Pin 27** | LVDS_15P |
| **Pin 28** | LVDS_15N |
| **Pin 29** | LVDS_14P |
| **Pin 30** | LVDS_14N |
| **Pin 31** | GND |
| **Pin 32** | LVDS_CLK1P |
| **Pin 33** | LVDS_CLK1N |
| **Pin 34** | GND |
| **Pin 35** | LVDS_13P |
| **Pin 36** | LVDS_13N |
| **Pin 37** | LVDS_12P |
| **Pin 38** | LVDS_12N |
| **Pin 39** | LVDS_11P |
| **Pin 40** | LVDS_11N |
| **Pin 41** | GND |
| **Pin 42** | FPS_DET |
| **Pin 43** | ODC_EN |
| **Pin 44** | 3D_VIDEO |
| **Pin 45** | LVDS_VDD |
| **Pin 46** | NC |
| **Pin 47** | AUX_I2C_SCL |
| **Pin 48** | AUX_I2C_SDA |
| **Pin 49** | MST |
| **Pin 50** | NC |
| **Pin 51** | GND |

**LVDS output configuration table**

| | | |
|---|---|---|
| **Quad LVDS output** | CN901 | CN902 |
| **Dual LVDS Output** | CN901 | NC |

**CN903** – Backlight Control

| | |
|---|---|
| **Pin 1** | +12V |
| **Pin 2** | +12V |
| **Pin 3** | +12V |
| **Pin 4** | +5V |
| **Pin 5** | +5V |
| **Pin 6** | +5V |
| **Pin 7** | GND |
| **Pin 8** | GND |
| **Pin 9** | GND |
| **Pin 10** | GND |
| **Pin 11** | LVDS_VDD |
| **Pin 12** | LVDS_VDD |
| **Pin 13** | LVDS_VDD |
| **Pin14** | +3V3_DVDD |

**CN701** – IR Input

| | |
|---|---|
| **Pin 1** | GND |
| **Pin 2** | +5V |
| **Pin 3** | IR_IN |

## 3.3. Switches

**Host Interface Switch: (SW401):** This switch selects the use of GProbe connector or Host Interface connector.

**SW401** – Host Interface

| Pin 1 | HOST_TX |
|-------|---------|
| Pin 2 | UART_TX |
| Pin 3 | GPROBE_TX |
| Pin 4 | HOST_RX |
| Pin 5 | UART_RX |
| Pin 6 | GPROBE_RX |

**SW403** – UART (TTL)

| Pin 1 | +5V |
|-------|-----|
| Pin 2 | GPROBE_TX |
| Pin 3 | GPROBE_RX |
| Pin 4 | GND |

**SW901** – LVDS_VDD and GND

## 3.4. Stuffing Options

### 3.4.1. Dual/quad TTL

**Dual TTL configuration:** stuff R609, unstuff R608

**Quad TTL configuration:** stuff R608, unstuff R609

### 3.4.2. IROM/SPI-Flash

**OCM boot from IROM code:** stuff R607, unstuff R606

**OCM boot from external ROM code:** stuff R606, unstuff R607