PRELIMINARY

Integrated Circuit Systems, Inc.

ICS873039

LOW SKEW, ÷2/4,÷4/6, LVPECL-TO-3.3V LVPECL / ECL CLOCK GENERATOR

GENERAL DESCRIPTION

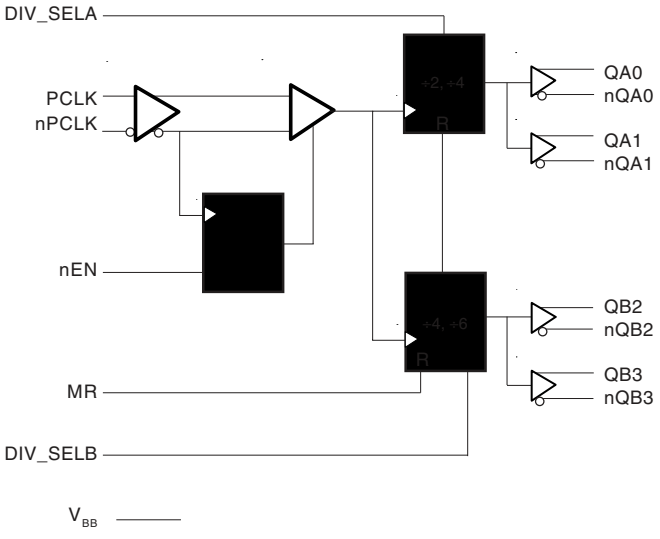
The ICS873039 is a low skew, high performance LVPECL-to-3.3V LVPECL / ECL Clock Generator/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS873039 has one LVPECL differential clock input pair. The PCLK, nPCLK pair can accept LVPECL, LVDS, CML, SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS873039 ideal for clock distribution applications demanding well defined performance and repeatability.

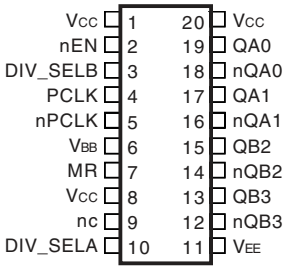
FEATURES

- 2 divide by 2/4 differential 3.3V LVPECL outputs; 2 divide by 4/6 differential 3.3V LVPECL outputs
- 1 differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum input frequency: 3.2GHz
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nPCLK input
- Output skew: 20ps (typical)
- Part-to-part skew: 85ps (typical)
- Propagation delay: 690ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Compatible with MC100LVEL39

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS873039
20-Lead SOIC, 300MIL
M Package
7.5mm x 12.8mm x 2.25 package body
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 8, 20	V_{CC}	Power		Positive supply pins.
2	nEN	Input	Pulldown	Clock enable.
3	DIV_SELB	Input	Pulldown	Selects divide value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
4	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
5	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
6	V_{BB}	Output		Bias voltage.
7	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low, and the inverted outputs (nQX) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
9	nc	Unused		No connect.
10	DIV_SELA	Input	Pulldown	Selects divide value for Bank A outputs as described in Table 3. LVCMOS / LVTTL interface levels.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQB3, QB3	Output		Differential output pair. LVPECL interface levels.
14, 15	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
16, 17	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
18, 19	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		KΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs			
MR	nOE	DIV_SELA	DIV_SELB	QA0, QA1	nQA0, nQA1	QB2, QB3	nQB2, nQB3
1	X	X	X	LOW	HIGH	LOW	HIGH
0	1	X	X	Not Switching	Not Switching	Not Switching	Not Switching
0	0	0	0	÷2	÷2	÷4	÷4
0	0	0	1	÷2	÷2	÷6	÷6
0	0	1	0	÷4	÷4	÷4	÷4
0	0	1	1	÷4	÷4	÷6	÷6

NOTE: After nCLK_EN switches, the clock outputs stop switching following a rising and falling input clock edge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	46.2°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current			65		mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			2.275			2.295			2.33		V
V_{OL}	Output Low Voltage; NOTE 1			1.545			1.52			1.535		V
V_{IH}	Input High Voltage(Single-Ended)		2.075			2.075			2.075			V
V_{IL}	Input Low Voltage(Single-Ended)				1.765			1.765			1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86			1.86			1.86			V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			1.475			1.495			1.53		V
V_{OL}	Output Low Voltage; NOTE 1			0.745			0.72			0.735		V
V_{IH}	Input High Voltage(Single-Ended)		1.275			1.275			1.275			V
V_{IL}	Input Low Voltage(Single-Ended)				0.965			0.965			0.965	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			-1.025			-1.005			-0.97		V
V_{OL}	Output Low Voltage; NOTE 1			-1.755			-1.78			-1.765		V
V_{IH}	Input High Voltage(Single-Ended)		-1.225			-1.225			-1.225			V
V_{IL}	Input Low Voltage(Single-Ended)				-1.535			-1.535			-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44			-1.44			-1.44			V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

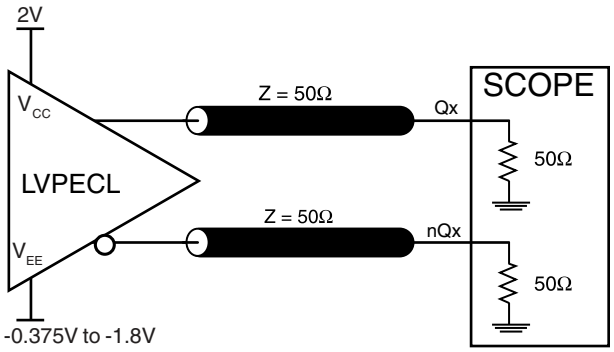
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V OR V_{CC} = 2.375 TO 3.8V; V_{EE} = 0V

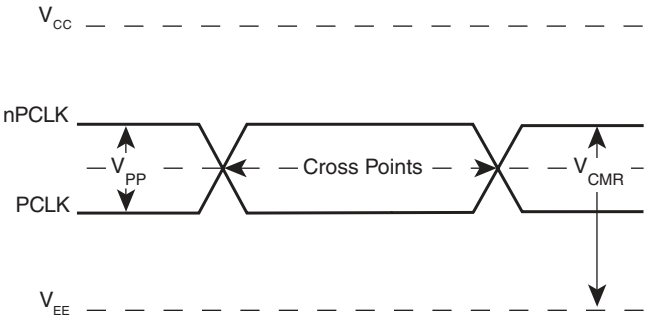
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Input Frequency				3.2			3.2			3.2	GHz
t_{PD}	Propagation Delay; NOTE 1			690			690			690		ps
*t*sk(o)	Output Skew; NOTE 2, 4			20			20			20		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			85			85			85		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			0.03			0.03			0.03		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		200			200			200		ps

All parameters are measured ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

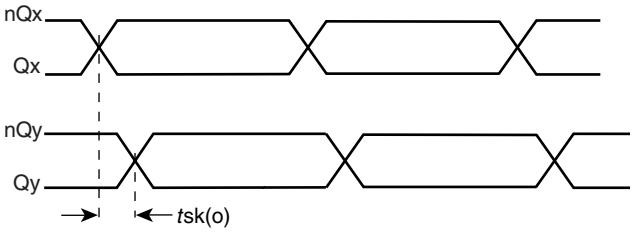
PARAMETER MEASUREMENT INFORMATION



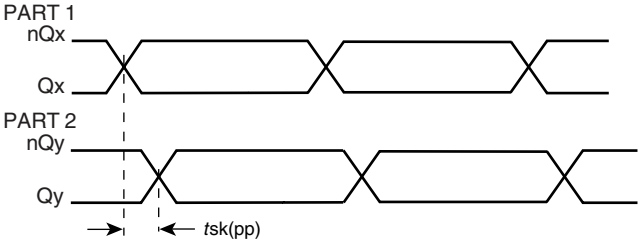
3.3V OUTPUT LOAD AC TEST CIRCUIT



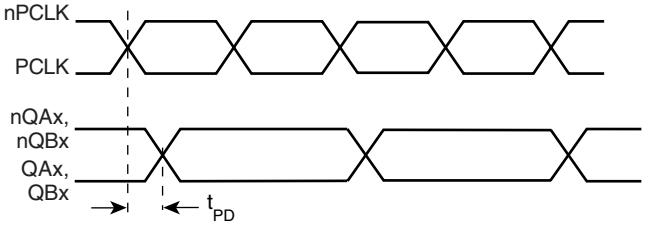
DIFFERENTIAL INPUT LEVEL



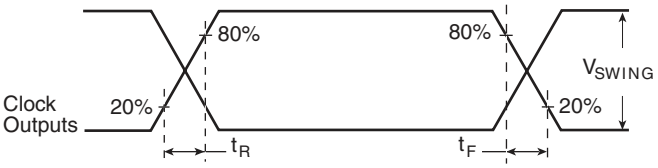
OUTPUT SKEW



PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 1A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

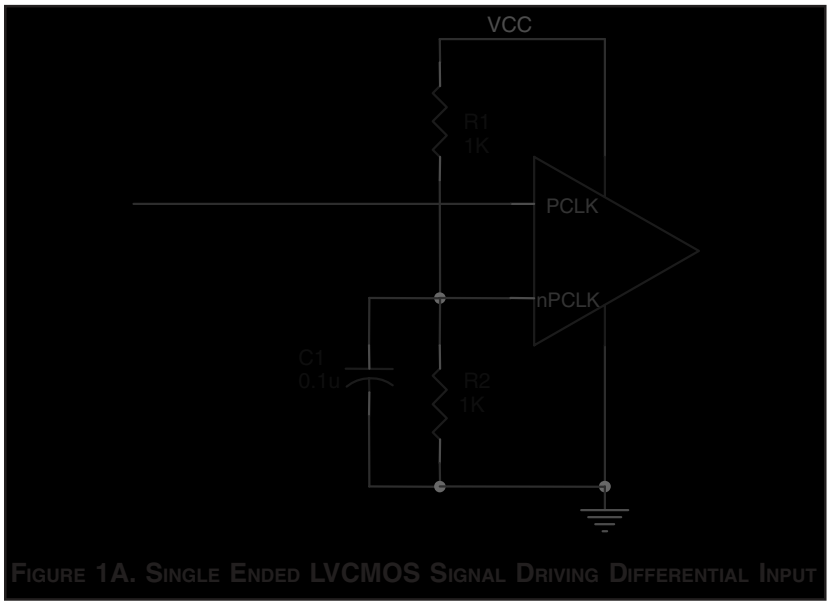


FIGURE 1A. SINGLE ENDED LVCMOS SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input.

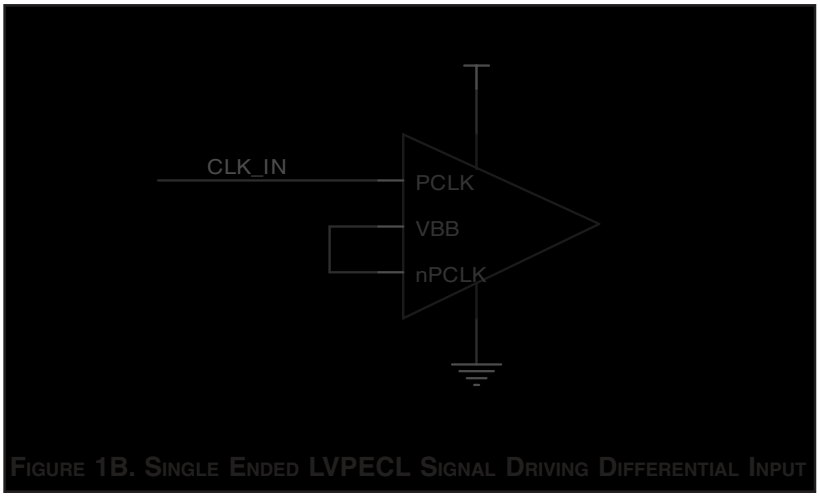


FIGURE 1B. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

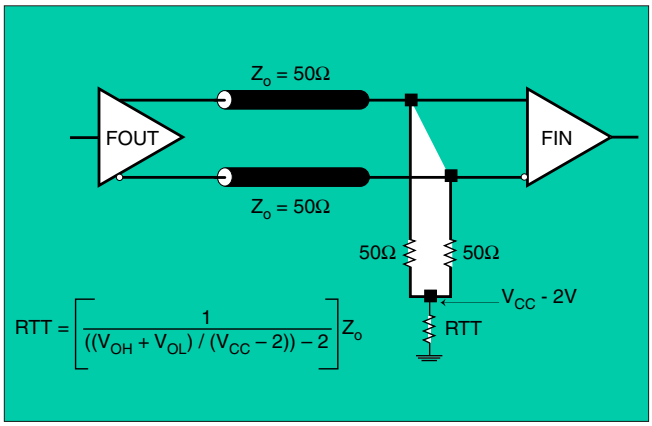


FIGURE 2A. LVPECL OUTPUT TERMINATION

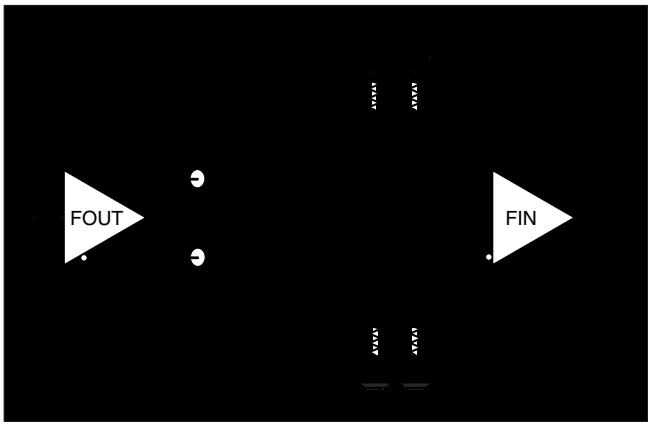


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

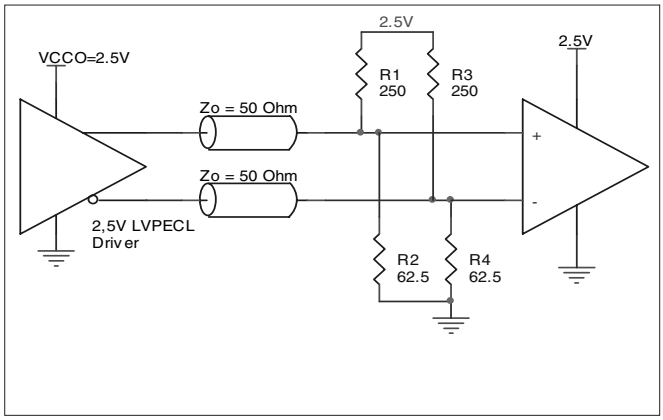


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

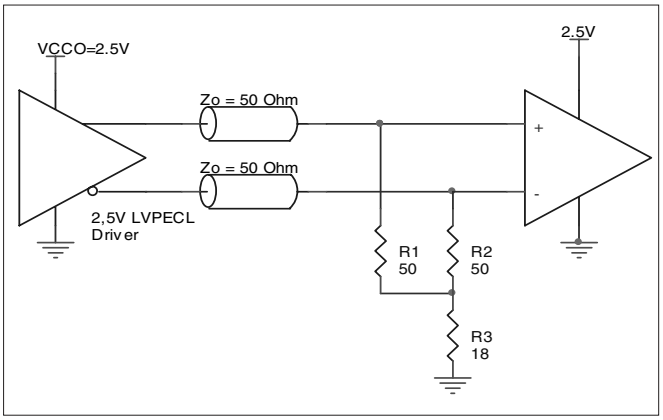


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

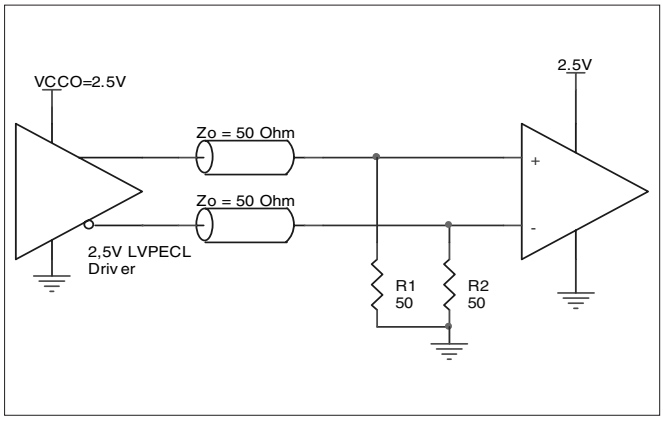


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

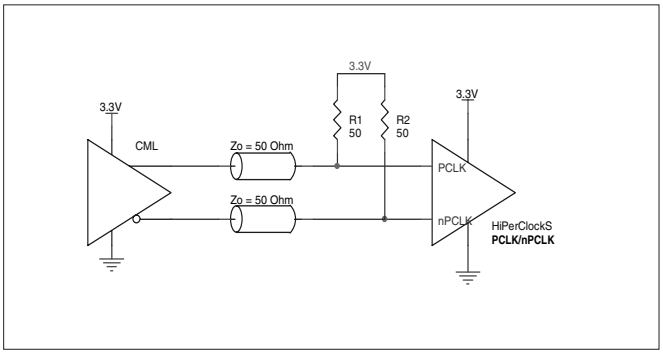


FIGURE 4A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

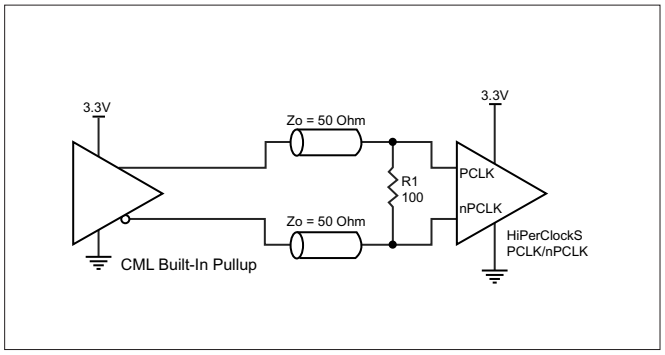


FIGURE 4B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

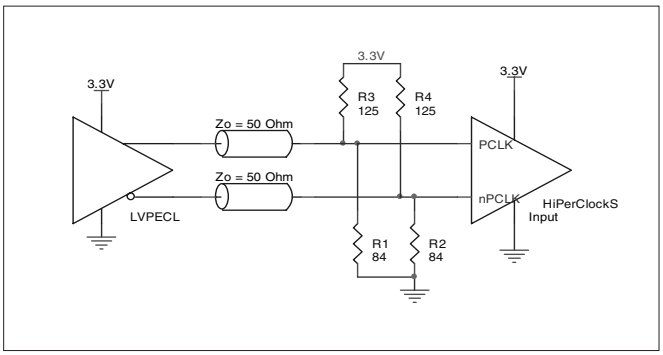


FIGURE 4C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

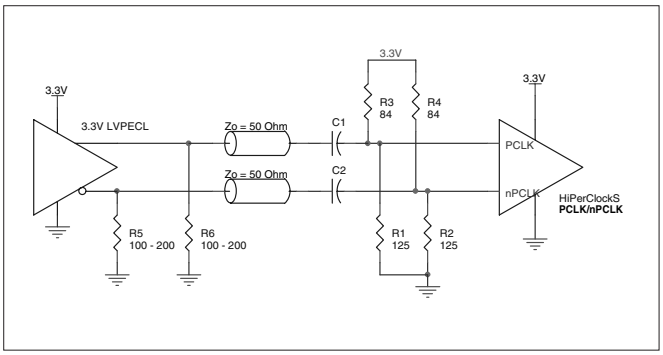


FIGURE 4D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

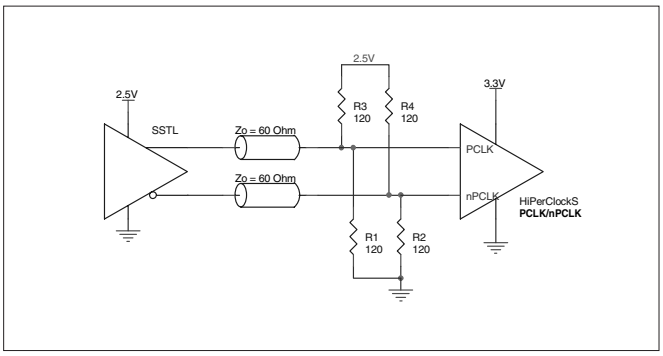


FIGURE 4E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

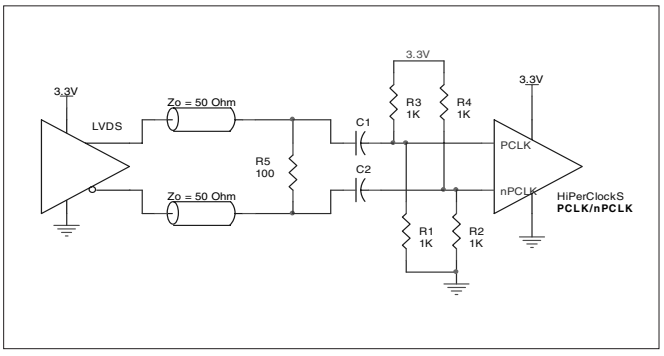


FIGURE 4F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS873039.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS873039 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 65mA = **247mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.2mW = **120.8mW**

Total Power $_{MAX}$ (3.8V, with all outputs switching) = 247mW + 120.8mW = **367.8mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
85°C + 0.368W * 39.7°C/W = 99.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN SOIC FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 5.

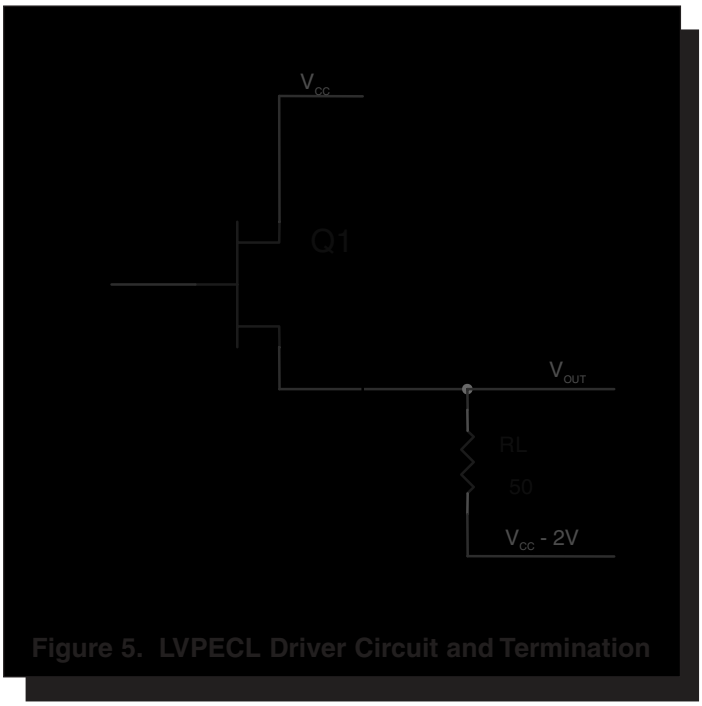


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.67V$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.67V$

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS873039 is: 434

PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

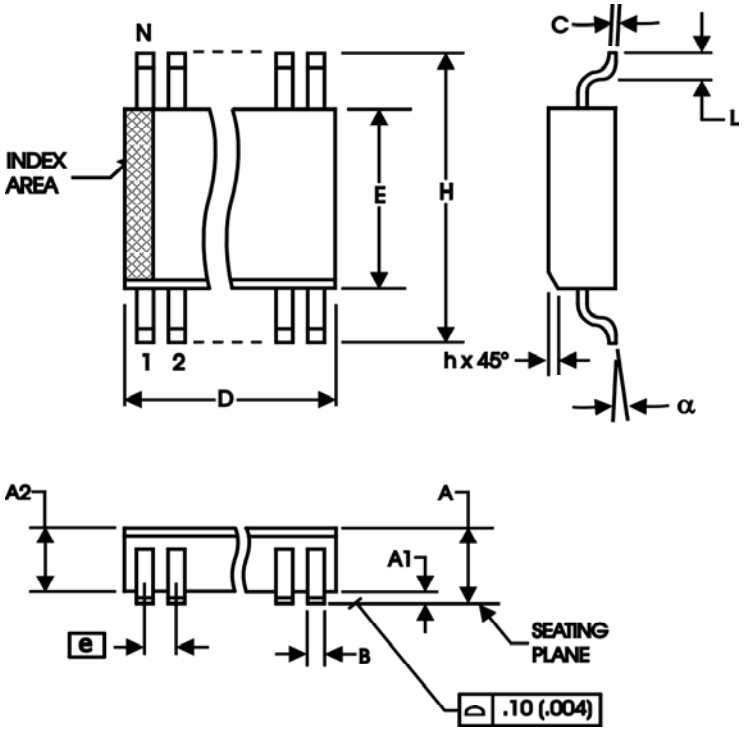


TABLE 8 PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS873039AM	ICS873039AM	20 lead SOIC	38 per Tube	-40°C to 85°C
ICS873039AMT	ICS873039AM	20 lead SOIC on Tape and Reel	1000	-40°C to 85°C