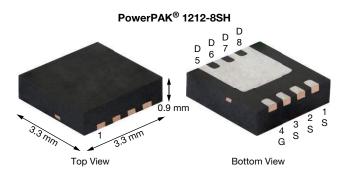


www.vishay.com

Vishay Siliconix

# N-Channel 30 V (D-S) Fast Switching MOSFET



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	30
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0075
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0082
Q <sub>g</sub> typ. (nC)	18
I <sub>D</sub> (A)	17.8
Configuration	Single

#### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> tested

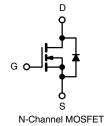




ROHS COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- Synchronous rectification
- · Load switch



ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH112DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (	T <sub>A</sub> = 25 °C, unless	s otherwise no	oted)			
PARAMETER		SYMBOL	10 S	STEADY STATE	UNIT	
Drain-source voltage	V <sub>DS</sub>	30	30			
Gate-source voltage	$V_{GS}$	±12	±12	V		
Continuous drain current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	17.8	11.3		
	T <sub>C</sub> = 70 °C		14.2	9.1		
Pulsed drain current		I <sub>DM</sub>	60	60	А	
Continuous source current (diode conduction) a		I <sub>S</sub>	3.2	1.3		
Single avalanche current		I <sub>AS</sub>	20	20		
Single avalanche energy L = 0.1 mH		E <sub>AS</sub>	20	20	mJ	
Manian and a substitution of the substitution	T <sub>C</sub> = 25 °C	Б	3.8	1.5	14/	
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 70 °C	P <sub>D</sub>	2	0.8	W	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-50 to +150		°C	
Soldering recommendations (peak temperature) b, c			260			

#### Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction to ambient 8	t ≤ 10 s	В	24	33	°C/W
Maximum junction-to-ambient <sup>a</sup>	Steady state	$R_{thJA}$	65	81	
Maximum junction-to-foot (drain)	Steady state	R <sub>thJC</sub>	1.9	2.4	

#### Note

a. Surface mounted on 1" x 1" FR4 board

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	1.5	V	
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	±100	nA	
Zara gata valtaga drain aurrent		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	5		
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
5	Б	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17.8 A	-	0.0060	0.0075	Ω	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$	-	0.0065	0.0082		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 17.8 A	-	97	-	S	
Diode forward voltage a	V <sub>SD</sub>	$I_S = 3.2 \text{ A}, V_{GS} = 0$	-	0.7	1.2	V	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	2610	-		
Output capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	340	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>		-	145	-		
Total gate charge	Qg		-	18	27		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 17.8 \text{ A}$	-	6.2	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	3.1	-	1	
Gate resistance	$R_g$	f = 1 MHz	0.5	1.2	1.8	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	10	15		
Rise time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$	-	10	15		
Turn-off delay time	t <sub>d(off)</sub>	$I_D\cong 1$ A, $V_{GEN}=10$ V, $R_g=6~\Omega$	-	65	100	ns	
Fall time	t <sub>f</sub>		-	10	15		
Body diode reverse recovery time t <sub>rr</sub>		1 2 2 A di/d+ 100 A/va	-	30	60		
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 3.2 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	18	-	nC	

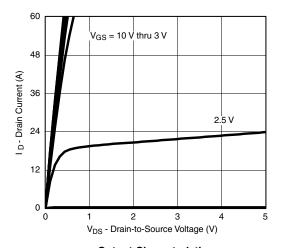
#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

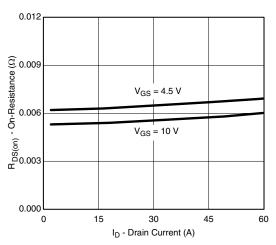
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



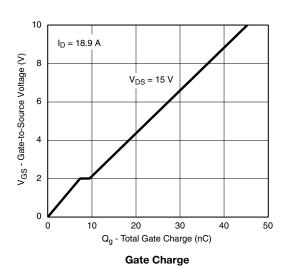
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### **Output Characteristics**



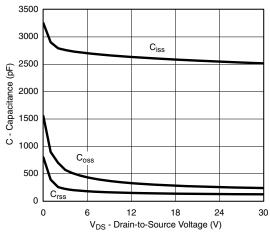
On-Resistance vs. Drain Current



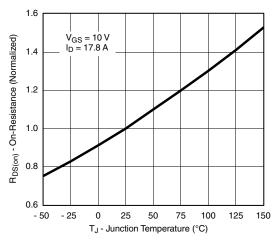
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**Transfer Characteristics** 



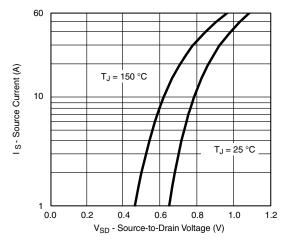
Capacitance



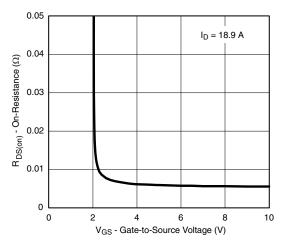
On-Resistance vs. Junction Temperature



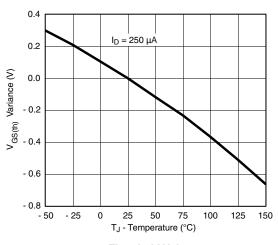
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



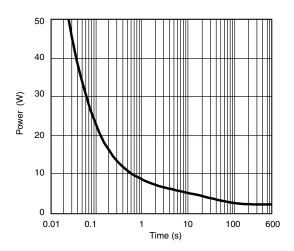
Source-Drain Diode Forward Voltage



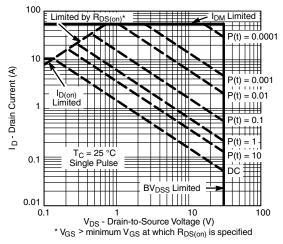
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



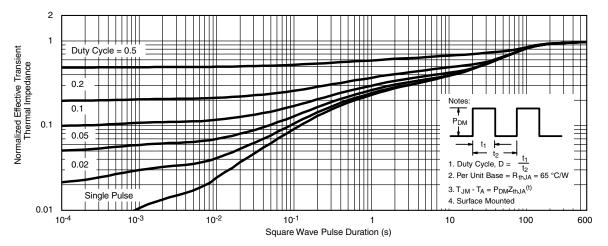
Single Pulse Power, Junction-to-Ambient



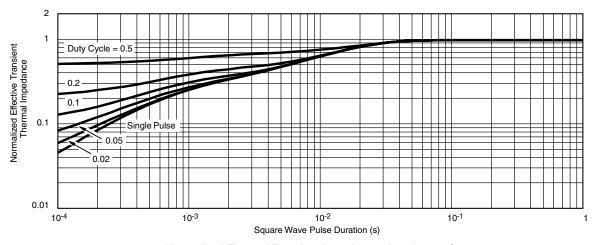
Safe Operating Area, Junction-to-Ambient



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

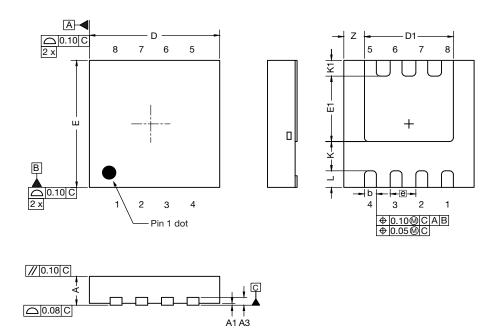


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?79345">www.vishay.com/ppg?79345</a>.

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# Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH

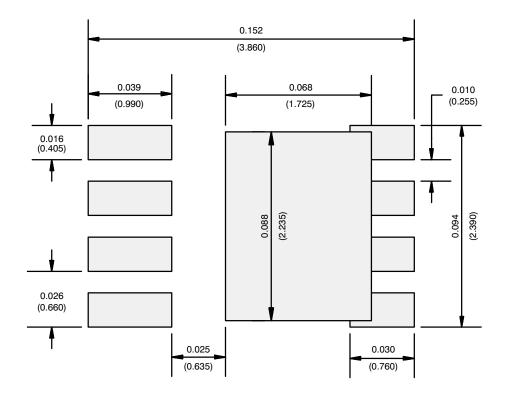


DIM.	MILLIMETERS			INCHES				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.82	0.90	0.98	0.032	0.035	0.038		
A1	0.00	-	0.05	0.000	-	0.002		
A3		0.20 ref.			0.008 ref.			
b	0.25	0.30	0.35	0.010	0.012	0.014		
D	3.20	3.30	3.40	0.126	0.130	0.134		
D1	2.15	2.25	2.35	0.085	0.089	0.093		
Е	3.20	3.30	3.40	0.126	0.130	0.134		
E1	1.60	1.70	1.80	0.063	0.067	0.071		
е		0.65 bsc.			0.026 bsc.			
K		0.76 ref.			0.030 ref.			
K1	0.41 ref.			0.016 ref.				
L	0.33	0.43	0.53	0.013	0.017	0.021		
Z	0.525 ref.			0.021 ref.				
	Rev. C, 07-Dec-2020					0.021 ref.		

DWG: 6062



## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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