STANDARD MICROSYSTEMS CORPORATION

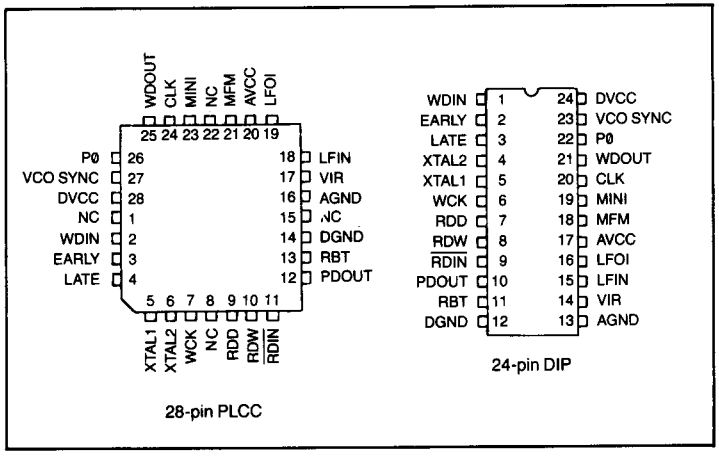
FDC92C81
PRELIMINARY

Self Tuning Analog Floppy Disk Data Separator (AFDDS)

FEATURES

- ☐ 1 Mb/s, 750, 500, 300, 250 and 125 Kb/s disk data rates
- ☐ Analog Data Separator performs complete data separation for floppy disk drives. Separates FM or MFM encoded data. 3½", 5¼" and 8" compatible.
- ☐ No adjustments necessary
- ☐ Provides clock for FDC765A
- ☐ High Performance Dual Gain Analog Phase Locked Loop
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator
- ☐ 300 Kb/s with clock frequency change and no filter change
- ☐ On-chip VCO
- ☐ Fabricated in Low Power CMOS
- ☐ TTL Compatible I/O
- ☐ Single +5V Supply

PIN CONFIGURATION



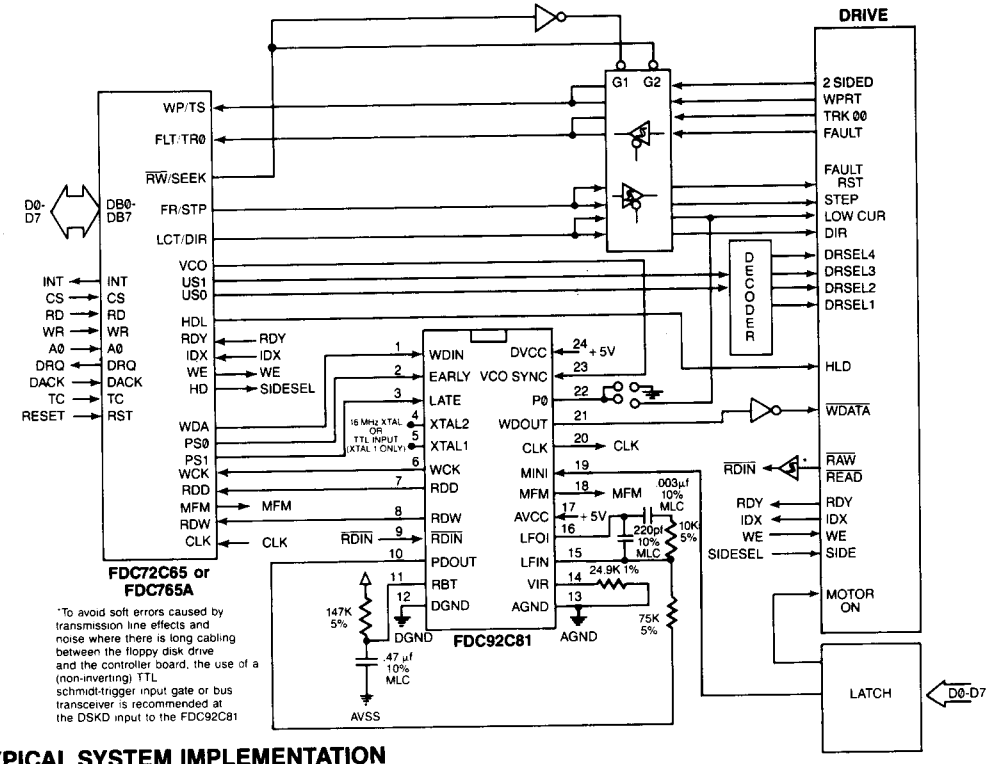
GENERAL DESCRIPTION

The FDC92C81 is a high performance CMOS Dual Gain Analog Floppy Disk Data Separator (AFDDS). The FDC92C81 is compatible with 3.5", 5.25" and 8" floppy disk drives, and provides all clocks required by the industry standard FDC765A and FDC72C65 floppy disk controllers.

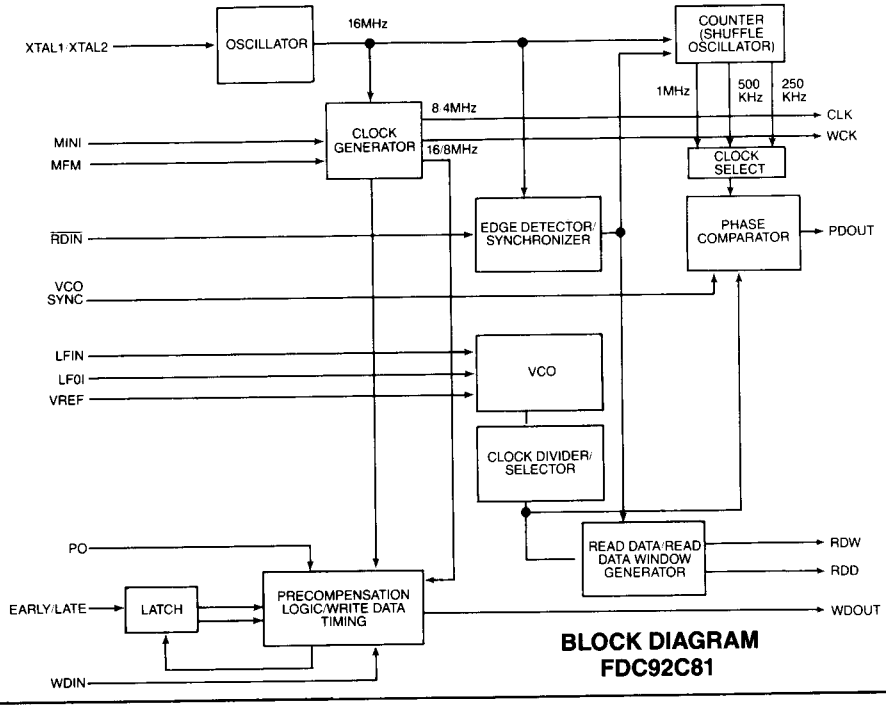
The FDC92C81 incorporates all the active components necessary to implement analog floppy disk data separation, eliminating the need for discrete transistors. Only a crystal and a few external resistors and capacitors are required. Using the FDC92C81 and a floppy disk controller chip, a system designer can build a highly reliable, cost efficient double or single density floppy disk subsystem requiring no tuning adjustments.

Three different user selectable values for write precompensation assure reliable positioning of data when writing to disk.

SECTION VI



TYPICAL SYSTEM IMPLEMENTATION



BLOCK DIAGRAM FDC92C81

TABLE 1—FDC92C81 DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	I/O	DESCRIPTION
1	Write Data In	WDIN	I	This input contains the serial clock and data bits which may be precompensated and output to the drive.
2	Early	EARLY	I	Used for precompensation. When high, the write data bit will be written early. Refer to table below.
3	Late	LATE	I	Used for precompensation. When high, the write data bit will be written late. EARLY / LATE / PULSE POSITION 0 / 0 / nominal 1 / 0 / early 0 / 1 / late 1 / 1 / not used
4 5	Crystal Crystal	XTAL2 XTAL1	O I	A 16.000 MHz parallel resonant crystal may be connected between XTAL1 and XTAL2. If a TTL signal is used in place of a crystal, the signal should be connected to XTAL1 while XTAL2 is left unconnected.
6	Write Clock	WCK	O	This output contains the clock which controls the rate at which data is written to the drive. See table for MINI pin.
7	Read Data	RDD	O	This output contains the reclocked encoded bit stream from the drive.
8	Read Data Window	RDW	O	This output is a function of the internal VCO frequency which tracks and properly frames the encoded drive bit stream for reliable clocking into the floppy disk controller.
9	Read Data In	$\overline{\text{RDIN}}$	I	This input is the read data from the floppy disk drive. The input is active low. The leading edge (high to low transition) is used for all frequency tracking operations.
10	Phase Detect Out	PDOUT	O	The output of the phase detect circuit. A 75K 5% resistor is connected between this output and LFIN.
11	Bias Reference	RBT	I	An external 147K 5% resistor connected between this pin and AVCC establishes a bias reference current for the VCO. This input should not be forced low.
12	Digital Ground	DGND		Digital Ground
13	Analog Ground	AGND		Analog Ground
14	Voltage to Current Reference	VIR	I	A 24.9K 1% metal film resistor connected between this pin and AVSS establishes a current reference for the on-chip voltage to current converter which is part of the VCO.
15	Low-pass Filter In	LFIN	I	This is the input to the low pass filter amplifier. A resistor is connected between this input and PDOUT and a low pass filter is connected between this input and LFOI.
16	Low-pass Filter	LFOI	I/O	This pin is the output of the low pass filter amplifier and the input to the VCO.
17	Analog Vcc	AVCC		+5V analog power supply
18	MFM Mode	MFM	I	When this input is high, the chip is in MFM mode. When low, the chip is in the FM mode.
19	MINI	MINI	I	This input, along with the input PØ specifies the amount of precompensation to be used. See table for the PØ pin. This input along with MFM controls the CLK and WCK outputs. MFM / MINI / WCK / CLK 0 / 0 / 500KHz / 8MHz 0 / 1 / 250KHz / 4MHz 1 / 0 / 1MHz / 8MHz 1 / 1 / 500KHz / 4MHz
20	Clock	CLK	O	This output is a 4MHz or 8MHz clock. See table above.
21	Write Data Out	WDOUT	O	This output is the precompensated serial write data to the floppy disk drive.

TABLE 1—FDC92C81 DESCRIPTION OF PIN FUNCTIONS CONTINUED

PIN NO.	NAME	SYMBOL	I/O	DESCRIPTION
22	Precompensation	P0	I	This input along with the MINI input specifies the amount of precompensation to be used. MINI / PO / PRECOMP 0 / 0 / 0.0ns 0 / 1 / 62.5ns 1 / 0 / 0.0ns 1 / 1 / 125.0ns
23	VCO Sync	VCO SYNC	I	VCO locks to clock when low and to data when high.
24	Digital Vcc	DVCC		+5V digital power supply.

MODE GAIN IMPLEMENTATION

The phase locked loop gain of the FDC92C81 is controlled by switching between two modes of operation, shuffle oscillator and arm on data. The mode change is via VCO SYNC. The shuffle oscillator mode is considered the high gain mode and the arm on data mode is considered the low gain mode.

Arm On Data Mode

The purpose of the arm on data mode is to reduce the gain so that the chip can handle higher amounts of bit jitter. In this mode, each code bit received from the drive resets the phase compare circuits and a counter (shuffle oscillator). The phase compare circuits are only armed for one compare cycle after each code bit. The counter is set such that ¼ bit cell after the phase compare reset has gone away, it creates an edge. (Only one compare is performed until the next code bit is received.) This edge is compared against the edges of the VCO by the phase compare circuits. The relationship between these edges is used to generate one pump-up or pump-down signal. Therefore, in this mode, each code bit causes only one update to the loop.

Shuffle Oscillator Mode

The shuffle oscillator mode allows for a fast lock to data time when attempting to acquire data synchronization. In this mode, each code bit received from the drive resets the phase compare circuits and a counter (shuffle oscillator). The phase compare circuits are always armed. The counter is set such that ¼ bit cell after the phase compare reset has gone away, it creates an edge. Each ½ bit cell thereafter creates an edge until reset by another code bit. This edge is compared against the edges of the VCO by the phase compare circuits. The relationship between these edges is used to generate pump-up/pump-down signals. In MFM codes, the minimum spacing between code bits is one bit cell, the maximum spacing is two bit cells. Therefore, in this mode, each code bit can cause up to four updates to the loop. This is how the gain of the loop is increased.

TYPICAL PERFORMANCE SPECIFICATIONS

PARAMETER	500KHz	300KHz	250KHz	UNITS
Bit Jitter				
Nominal Speed	380	620	760	nsec
+5% Speed	360	600	740	nsec
−5% Speed	380	660	840	nsec
Window Margin				
Early	480	800	860	nsec
Late	400	720	820	nsec
Lock to Encoded Data	less than 3 bytes			

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.3V
Negative Voltage on any Pin, with respect to Ground ..... −0.3V
Power Dissipation 0.25W
Positive Voltage on V_{CC} Pin, with respect to Ground 7.0V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power supply line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS TA = 0°C to 70°C, V_{CC} = 5.0V ±5% unless otherwi

PARAMETERS	MIN	TYP	MAX	UNITS	COMMEN
INPUT VOLTAGE					WDIN, EARLY, LATE, RDIN, PØ, SYNC
High Level V_{IL}	−0.3		0.8	V	
High Level V_{IH}	2.0		(VCC)	V	
INPUT VOLTAGE					XTAL 1, XTAL 2
Low level V_{IL}	−0.3		0.8	V	
High Level V_{IH}	3.2		(VCC)	V	
OUTPUT VOLTAGE					CLK, WCK, RDD, RDW, MFM, MINI, WDOUT
Low Level V_{OL}			0.4	V	I_{OL} = 1.6mA except CLK I_{OL} = 0.4mA, CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100uA except CLK I_{OH} = −400uA, CLK only
POWER SUPPLY CURRENT I_{CC}			TBD	mA	
INPUT LEAKAGE CURRENT I_{IL}			TBD	uA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE C_{IN}		TBD		pF	WDIN, EARLY, LATE, RDIN, PØ, SYNC, XTAL 1

AC ELECTRICAL CHARACTERISTICS TA = 0°C to 70°C, V_{CC} = 5.0V ±5% unless otherw

PARAMETERS	SMBL	MIN	TYP	MAX	UNIT	LOAD	
Read data width	T_1	40			ns	20pf	
Window setup time	T_2	15			ns	20pf	
Window hold time	T_3	15			ns	20pf	
Window cycle time	T_4		2 1 4 2		us us us us	20pf	MFM = 0 MINI = 0 MFM = 1 MINI = 0 MFM = 0 MINI = 1 MFM = 1 MINI = 1
WCK high	T_5	80	250	350	ns	20pf	
WCK cycle time	T_6		4 2 1		us us us	20pf 20pf 20pf	125KHz data rate 250KHz data rate 500KHz data rate
CLK high	T_7	40			ns	20pf	
CLK low	T_8	40			ns	20pf	
CLK period	T_9	120		500	ns	20pf	
WDOUT width	T_{9a}	250	315	350	us	20pf	x2 if mini = 1
CLK ↑ to WCK ↑ delay	T_{10}	0		40	ns		

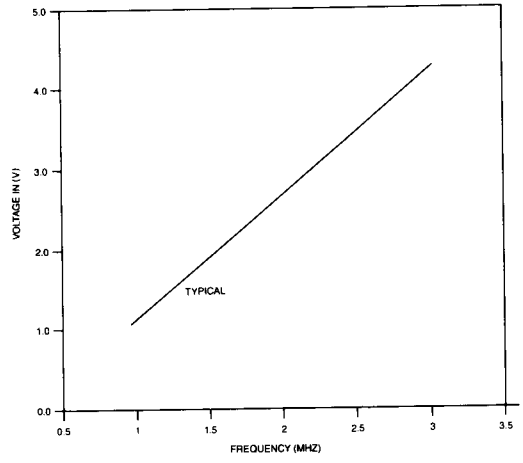
AC ELECTRICAL CHARACTERISTICS CONTINUED

PARAMETERS	SMBL	MIN	TYP	MAX	UNIT	LOAD	COM.
CLK ↑ to WCK ↓ delay	T_{11}	0		40	ns		
WDOUT early rising edge to WDOUT nom. rising edge	T_{12}	Desired Precomp Value					see table for pin 22
WDOUT nom. rising edge to WDOUT late rising edge	T_{13}	Desired Precomp Value					see table for pin 22
Pre-shift delay time from WCK positive edge	T_{14}	20		100	ns		
WDIN delay time rising edge of WCK to rising edge of WDIN, falling edge of WCK to falling edge of WDIN	T_{15}	20		100	ns		
WDIN width	T_{16}	30	200	300	ns		
Read data width	T_{17}	100			ns		
Read data cycle time	T_{18}		2 2 4 4		us us us us		500 Kb/s MFM, 250 Kb/s FM 250 Kb/s MFM, 125 Kb/s FM

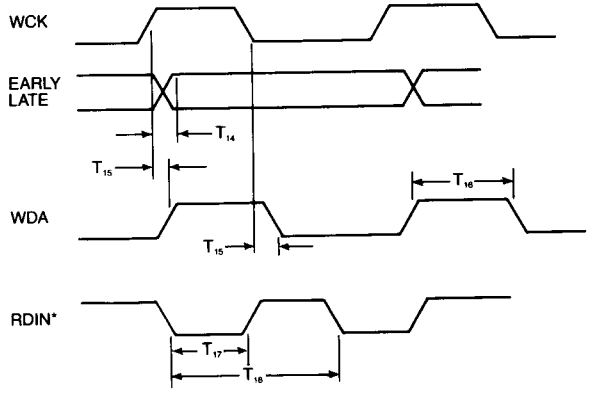
The following inputs are DC levels: MFM, MINI, P_0.

TYPICAL VCO VOLTAGE IN VS. FREQUENCY

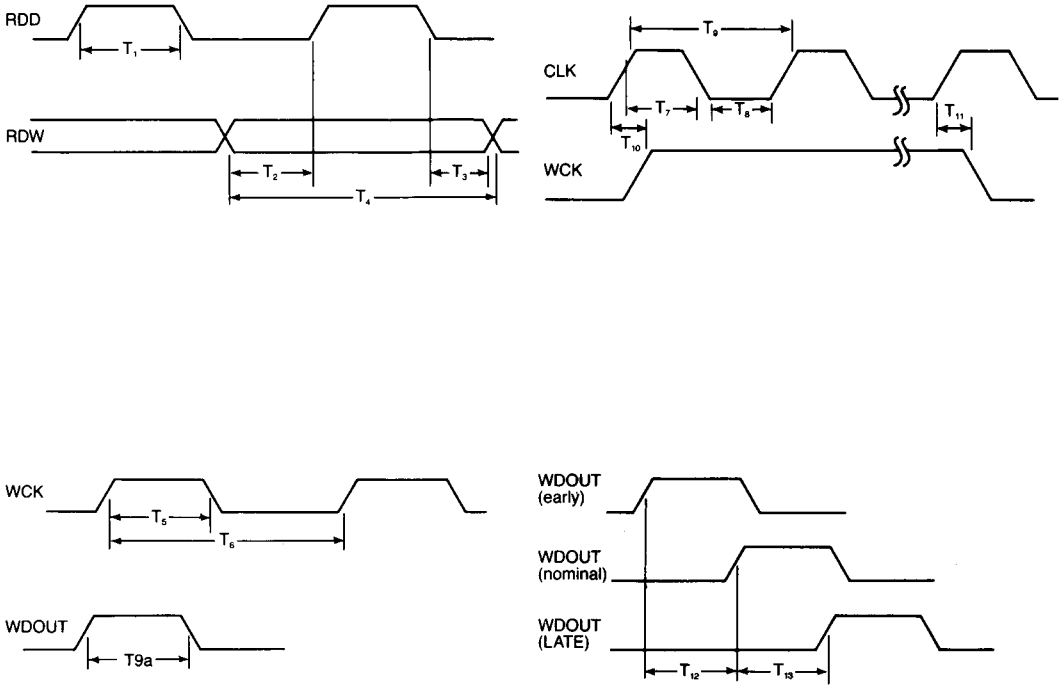
FDC92C81



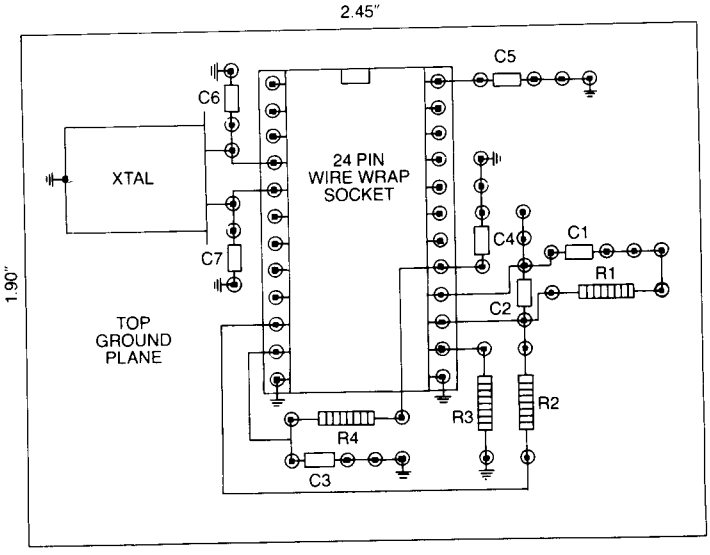
INPUT TIMING



OUTPUT TIMING



NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.



RESISTOR VALUES	
R1	10K 5%
R2	75K 5%
R3	24.9K 1% metal film
R4	147K 5%

CAPACITOR VALUES	
C1	.003 uf 10% MLC
C2	220 pf 10% MLC
C3	.47 uf 10% MLC
C4	.22 uf 10%
C5	.22 uf 10%
C6	60 pf 10%
C7	60 pf 10%

REDUCE TO
2.500 ±.005"

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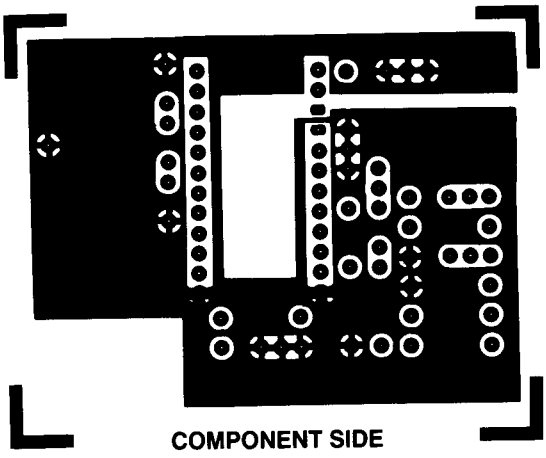
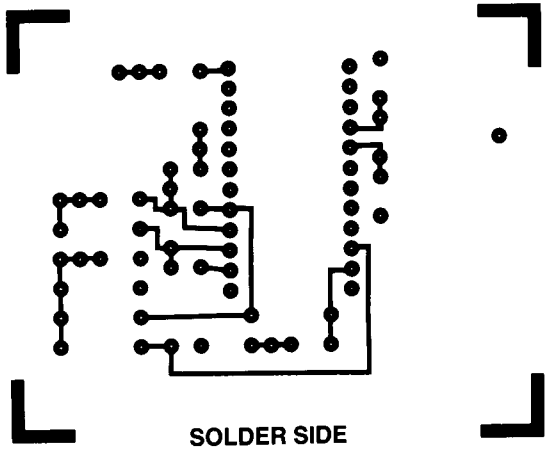
2.500 ±.005"



COMPONENT SIDE



SOLDER SIDE

NOTE: The printed circuit board artwork shown above is included for illustration only. Camera ready artwork is available through your SMC representative or regional sales office.

Blank PC boards (based on the illustrations above) are also available to facilitate evaluation and design. Contact your SMC representative or regional sales office for more information.

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