BURR - BROWN®

DAC650

12-Bit, 500MHz DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- 500MHz UPDATE RATE
- GUARANTEED SPURIOUS PERFORMANCE
- LOW GLITCH
- FAST SETTLING
- INTERNAL EDGE-TRIGGERED LATCH
- LASER TRIMMED ACCURACY
- INTERNAL REFERENCE
- CLEAN LOW-NOISE OUTPUT

APPLICATIONS

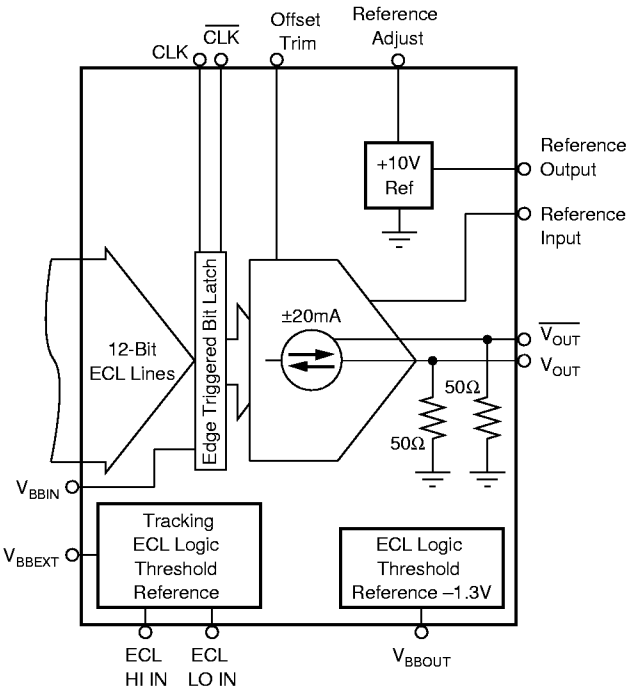
- DIRECT DIGITAL SYNTHESIS
- ARBITRARY WAVEFORM GENERATION
- HIGH RESOLUTION GRAPHICS
- COMMUNICATIONS LOCAL OSCILLATORS
  - Spread Spectrum
  - Base Stations
  - Digitally Tuned Receivers
- HIGH-SPEED MODEMS

DESCRIPTION

The DAC650 is a high performance 12-bit digital to analog converter for high frequency waveform generation. It is complete with an internal low drift reference and edge-triggered data latch. The internal segmentation and latching provide for minimal output glitch energy.

The ECL compatibility provides for low digital noise at high update rates. The 50Ω output resistance and low output capacitance simplify transmission line design and filtering at the output. Complementary outputs are offered for increased performance while driving transformers or differential amplifiers.

The DAC650 combines precision thin film and bipolar technology with high speed gallium arsenide to create a high performance, cost effective solution for modern waveform synthesis systems.



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SPECIFICATIONS

ELECTRICAL

Over full specified temperature range, using the internal +10V reference and rated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	DAC650JL-4 MIN	DAC650JL-4 TYP	DAC650JL-4 MAX	UNITS
TEMPERATURE RANGE					
Specification: DAC650JL-4	Ambient	0		+70	°C
θ_{CA}	27		°C/W		
θ_{JC}	13		°C/W		
DIGITAL INPUTS					
Logic	12 Parallel Input Lines		ECL Compatible		
Resolution			12	Bits	
ECL Logic Input Levels(1): V_{IL}	Logic "0"	–1.475	–1.8	–2	V
I_{IL}			1.0	10	µA
V_{IH}	Logic "1"	–1.115	–0.8	–0.6	V
I_{IH}			1.0	10	µA
Logic Threshold Voltage		–1.2	–1.3	–1.4	V
DIGITAL TIMING					
Input Data Rate		DC		500	MHz
CLK Pulse Width Low		1.0			ns
Set-Up Time	2.0	1.8		ns	
Hold Time (Referred to CLK)		–500	–600		ps
Propagation Delay			1.5		ns
ANALOG OUTPUT					
Bipolar Output Current	R_L = 0Ω		±20		mA
Bipolar Output Voltage	R_L = ∞		±1.0		V
Output Resistance	V_{OUT}, V_{OUT} to Ground	49	50	51	Ω
Output Resistance Drift			50		ppm/°C
Output Capacitance			5		pF
TRANSFER CHARACTERISTICS					
Integral Linearity Error	Best Fit Straight Line			±0.16	%FSR
Differential Linearity Error	+25°C		±0.018	±0.036	%FSR
	Over Temperature		±0.018	±0.036	%FSR
Monotonicity			Typical		
Bipolar Gain Error	Output Voltage, R_L = ∞		±0.5	±1.0	%FSR
Bipolar Offset Error	Output Voltage, R_L = ∞			±0.5	%FSR
TIME DOMAIN PERFORMANCE					
Glitch EnergyMajor Carry		20		pV-s	
Output Rise Time	10% to 90%		300		ps
Output Fall Time	90% to 10%		350		ps
Settling Time(2): ±0.1%FSR	Major Carry, 1LSB Change		2.0		ns
REFERENCES					
V_{BB} Input Range (Pin 1)		–1.4	–1.3	–1.2	V
$V_{BB\ INT}$ Reference (Pin 68)		–1.4	–1.3	–1.2	V
$V_{BB\ EXT}$ Tracking Reference (Pin 67)	$ECL_{HI\ IN}$ = –0.8V, $ECL_{LO\ IN}$ = –1.8V	–1.4	–1.3	–1.2	V
Internal Reference Voltage (Ref Out)		9.95	10	10.05	V
Ref in Resistance			4950		Ω
Ref in Operating Voltage Range		4.5	10.0	11.0	V
DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range(3)					
f_O = 1MHz, f_{CLK} = 100MHz	+25°C, Span = DC to $f_{CLK}/2$	65	68		dBc(4)
f_O = 10MHz, f_{CLK} = 100MHz	+25°C, Span = DC to $f_{CLK}/2$	59	63		dBc
f_O = 30MHz, f_{CLK} = 200MHz	+25°C, Span = DC to $f_{CLK}/2$	50	52		dBc
f_O = 80MHz, f_{CLK} = 200MHz	+25°C, Span = DC to $f_{CLK}/2$	47	50		dBc
f_O = 80MHz, f_{CLK} = 500MHz	+25°C, Span = DC to 150MHz	49	55		dBc
f_O = 100MHz, f_{CLK} = 500MHz	+25°C, Span = 50MHz to 150MHz	51	56		dBc
Output Noise	Full Scale Sine Wave Output		1.0		$\mu V/\sqrt{Hz}$
POWER SUPPLIES					
Supply Voltages: $+V_{CC}$	Operating, T_{MIN} to T_{MAX}	+14.25	+15	+15.75	V
$-V_{CC}$		–15.75	–15	–14.25	V
$+V_{DD1}$		+4.75	+5	+5.25	V
$-V_{DD2}$		–5.46	–5.2	–4.94	V
Power Supply Rejection	All Supplies, ±5% Change		0.05	0.08	%/%
Supply Currents: $+I_{CC}$	Operating		10	13	mA
$-I_{CC}$			–47	–50	mA
$+I_{DD1}$			53	57	mA
$-I_{DD2}$			–191	–265	mA
Power Consumption	Operating		2.0	2.6	W

NOTE: (1) V_{BBIN} (Pin 1) connected to $V_{BB\ INT}$ (Pin 68). (2) Settling time is influenced by load due to fast edge speeds. Use good transmission line techniques for best results. (3) Spurious Free Dynamic Range includes both harmonic and non-harmonic related spurs in the bandwidth indicated. (4) dBc is "dB referred to the fundamental amplitude."

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE (AMBIENT)
DAC650JL-4	68-Pin Ceramic, Gullwing	256	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

$\pm V_{CC}$	±18V
Logic Input	+0.5V to –5.5V
Case Temperature	–40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

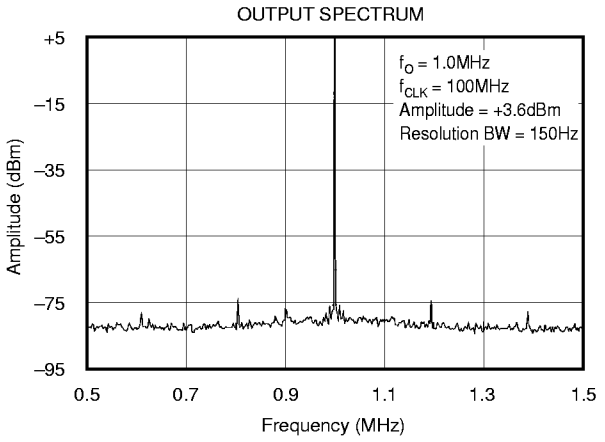
PIN DEFINITIONS

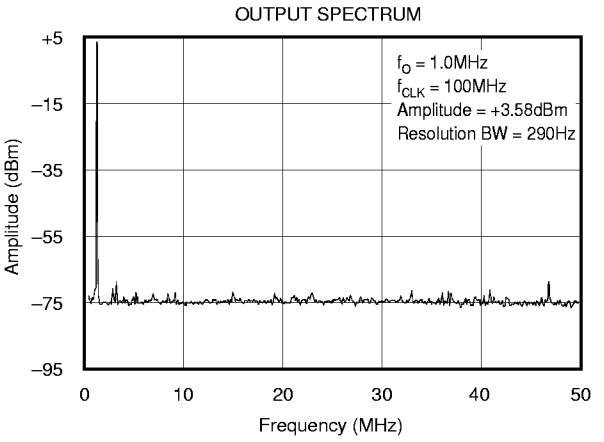
PIN #	DESIGNATION	DESCRIPTION	PIN #	DESIGNATION	DESCRIPTION
1	V_{BB}	Sets Logic Threshold for Bits 1-12	35	AGND	Ground for Analog Output Current
2	Bit 1	MSB	36	AGND	
3	Bit 2		37	AGND	
4	Bit 3		38	AGND	
5	Bit 4		39	$\overline{V_{OUT}}$	Complementary Output Voltage
6	Bit 5		40	$\overline{V_{OUT}}$	
7	Bit 6		41	$\overline{V_{OUT}}$	
8	Bit 7		42	AGND	
9	Bit 8		43	AGND	
10	Bit 9		44	AGND	
11	Bit 10		45	V_{OUT}	Output Voltage
12	Bit 11		46	V_{OUT}	
13	Bit 12	LSB	47	V_{OUT}	
14	V_{EE}	Logic Power (–5.2V Nominal)[1]	48	AGND	
15	V_{EE}		49	AGND	
16	CLK	Clock	50	AGND	
17	CLK_{NOT}	Not Clock	51	AGND	
18	DNC	Do Not Connect	52	–15V	–15V Supply
19	V_{EE}		53	–15V	
20	V_{EE}		54	PWR GND	Ground for Analog Supplies
21	V_{EE}		55	+5V	+5V Supply
22	V_{EE}		56	+5V	+5V Supply
23	V_{EE}		57	V_{OS} ADJ	Offset Adjust
24	V_{EE}		58	PWR GND	Ground for Analog Supplies
25	V_{EE}		59	Ref_{ADJ}	Reference Out Adjust
26	V_{EE}		60	Ref_{OUT}	Reference Out (+10V, Buffered)
27	DGND	Ground for Logic	61	Ref_{IN}	Reference In (4.950kΩ)
28	DGND		62	+15V	+15V Supply
29	DGND		63	PWR GND	Ground for Analog Supplies
30	DGND		64	–5.2V Analog	Analog Power (–5.2V Nominal)[1]
31	DGND		65	ECL LO_{IN}	External ECL LOW input (optional)
32	DGND		66	ECL HI_{IN}	External ECL HI input (optional)
33	DGND		67	V_{BBEXT}	The buffered mean of LO_{EXT} and HI_{EXT}
34	DGND		68	V_{BBINT}	Internally generated –1.3V reference

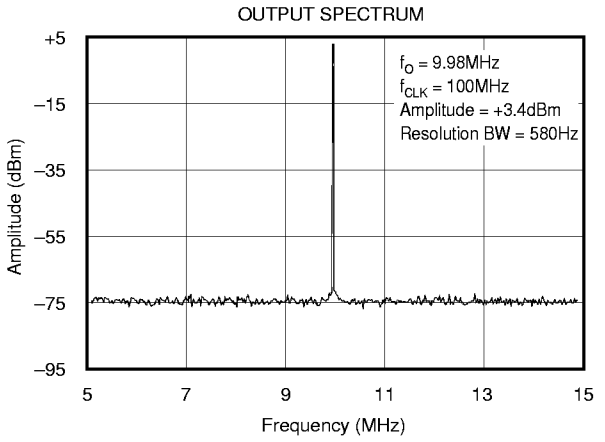
NOTE: (1) Both the –5.2V Logic and –5.2V analog pins should be powered from a common supply.

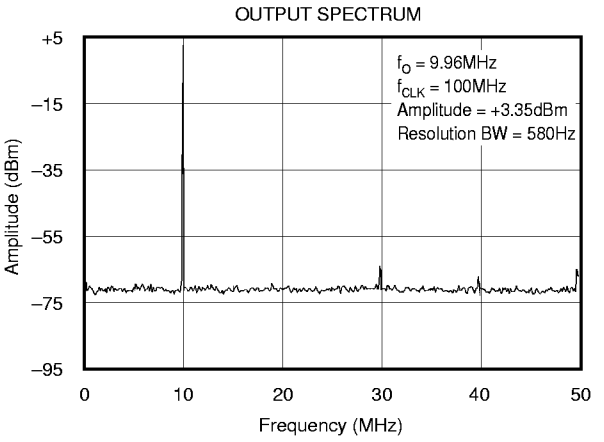
TYPICAL PERFORMANCE CURVES

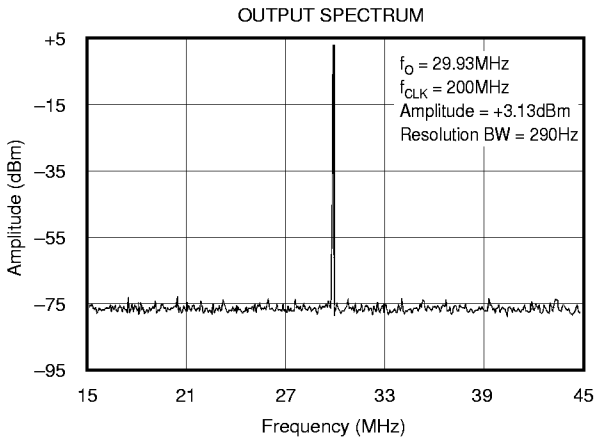
At T_A = +25°C, unless otherwise noted.

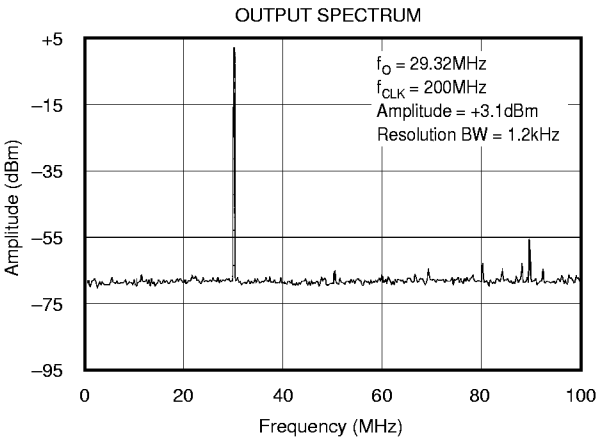








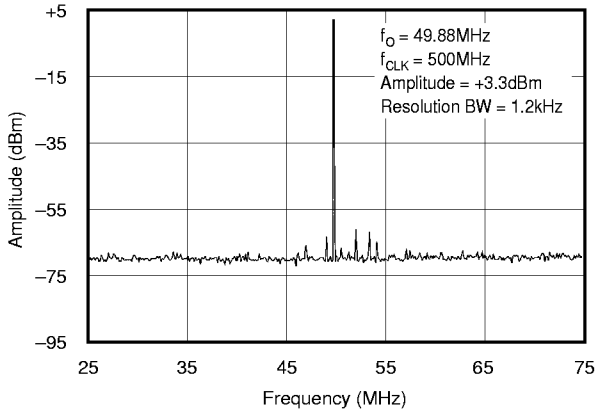




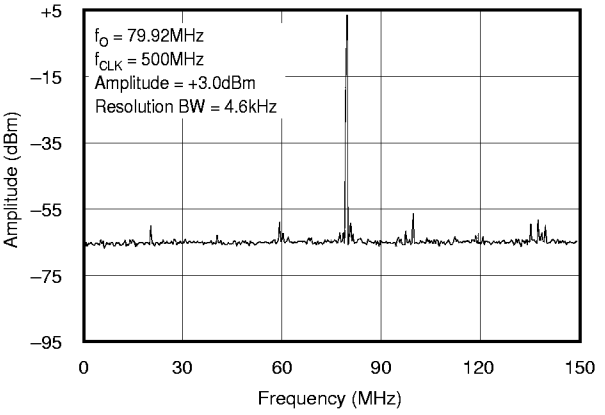
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, unless otherwise noted.

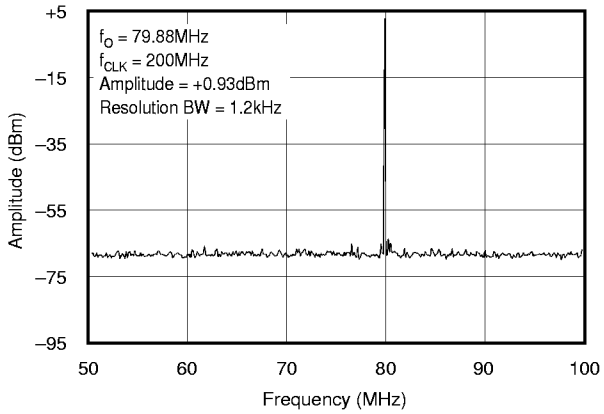
OUTPUT SPECTRUM



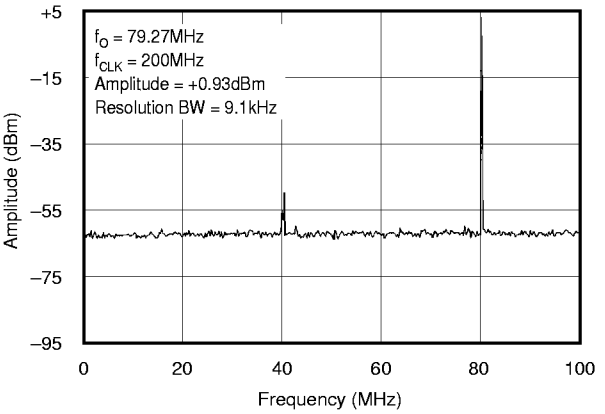
OUTPUT SPECTRUM



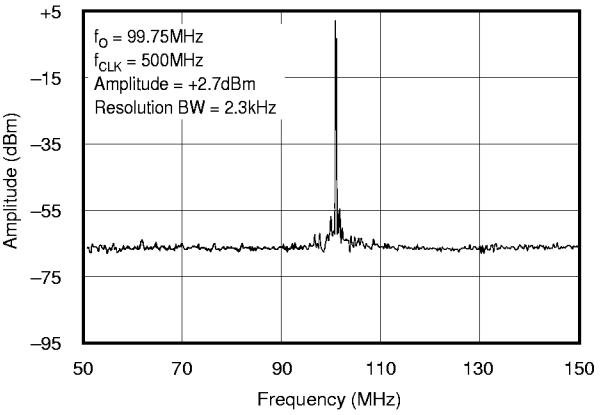
OUTPUT SPECTRUM



OUTPUT SPECTRUM



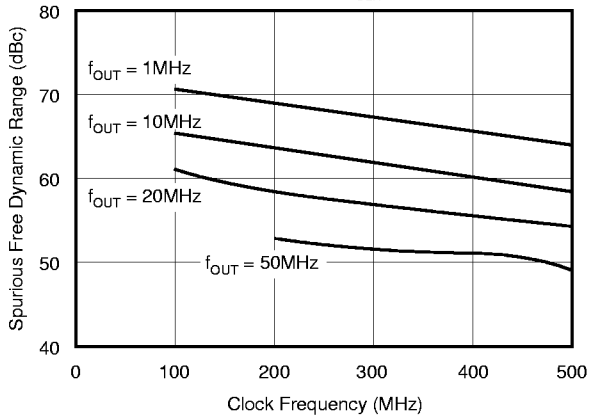
OUTPUT SPECTRUM



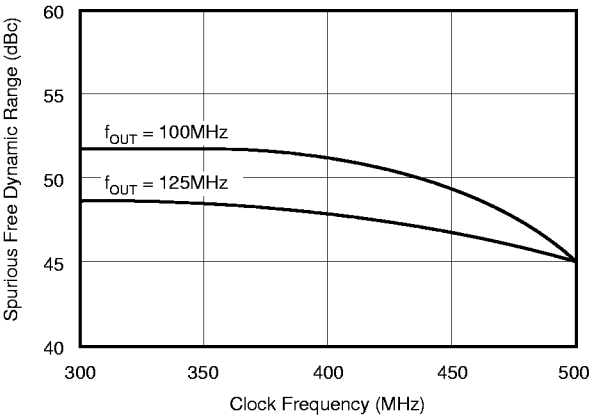
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, unless otherwise noted.

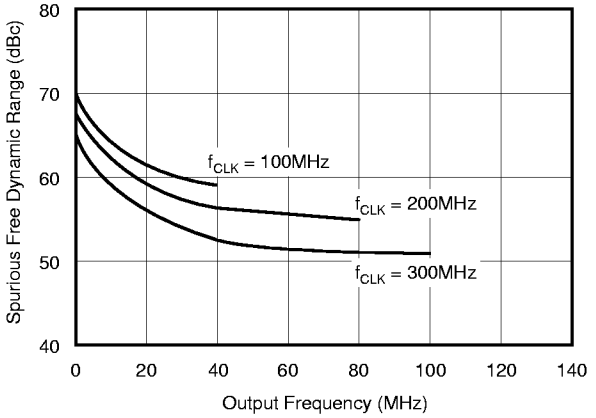
SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to $f_{CLK}/2$)



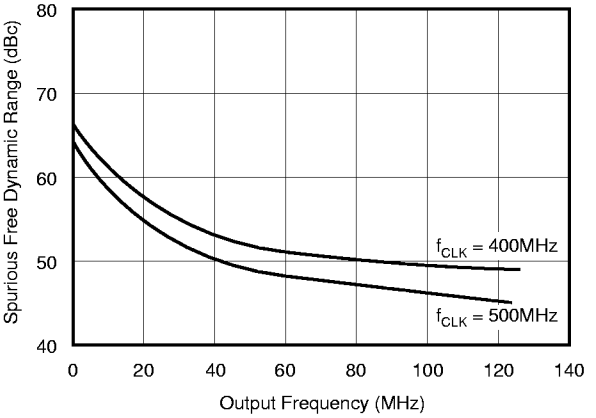
SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to 200MHz)



SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to $f_{CLK}/2$)



SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to 200MHz)



TECHNOLOGY OVERVIEW

The DAC650 uses a unique design approach to achieve very fast settling time and high resolution. This mixed-technology design uses two active chips: one gallium arsenide and the other silicon.

The GaAs MESFET die is used for those circuits which determine speed. This includes the latches, data decoders, and current switches. A silicon die with thin film is used for those circuits which determine accuracy, such as the precision references and current sources. The precision R-2R resistor ladders are laser trimmed to further increase the accuracy of the DAC650. A block diagram of the DAC650 is shown in Figure 1.

THEORY OF OPERATION

The DAC650 employs a familiar architecture where input bits switch on the appropriate current sources. Bits 1-3 are decoded into 7 segments before the first set of latches. A similar delay is given for the 9 least significant bits to minimize data skew. The edge triggered master-slave latches are driven by an internal clock buffer. This buffer placement has matched the clock lines to each of the 32 latches, thus minimizing output glitch energy.

There are 7 current sources for bits 1 to 3. Current sources for bits 4-8 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 9-12 are fed to the laser trimmed R-2R ladder for proper scale-down. The segmentation further minimizes output glitch which can cause spectral degradation.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder (100Ω) in parallel with 100Ω (Figure 1). With all of the current sources off, the output voltage is at +1V. With all current sources on (–40mA), the output voltage is at –1V. There is also a complementary $\overline{V_{OUT}}$ output that allows for a differential output signals. The full scale complementary outputs (V_{OUT} and $\overline{V_{OUT}}$) can be simply modeled as ±20mA in parallel with 50Ω. This gives an output swing of 1Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

A precision +10V reference is included in the DAC650. A 50Ω resistor should be connected between REF_{IN} and REF_{OUT} for the specified unadjusted gain. This internal reference has been laser trimmed to minimize offset and gain drift. Alternatively, an external reference may be used. Multiple DACs may be run from one master reference by connecting a 50Ω resistor from each REF_{IN} to the master REF_{OUT}. A 100Ω potentiometer may be used in place of the 50Ω resistor in order to provide a ±1% gain adjustment range (Figure 2).

A wider adjustment range of ±20% may be achieved by connecting a 10kΩ potentiometer from REF_{OUT} to ground, with the wiper connected to the REF_{ADJ} pin. Adjusting the output to more than 40mA full scale may degrade high frequency performance and reliability due to higher current densities and operating temperature. Alternatively, lower full scale currents will affect operation because there is less current available to charge internal and external capacitances.

It should be noted that the gain adjust techniques mentioned above affect the current output and thus the voltage output from the DAC650. The voltage output will also be affected by an external load acting in parallel with the 50Ω output impedance.

OFFSET ADJUST

The offset may be adjusted by connecting a potentiometer between the +5V supply and ground with the wiper connected to the offset adjust pin. The voltage on this pin with no connection is about 2V, with an equivalent impedance of 1.6kΩ. A 10kΩ potentiometer will give the necessary adjustment range. The full scale range of the DAC output may be offset so it is not symmetrical around zero, but the full scale range must also be adjusted so that the output swing does not exceed ±1V. Connecting the offset adjust pin to ground gives a unipolar output of 0 to –2V (with no load) or 0 to –1V (with a 50Ω load). This also reduces the current requirements for the +5V supply by 20mA.

DIGITAL INPUTS, LOGIC THRESHOLDS, and TERMINATION

The input logic levels and clock levels are ECL compatible. The data inputs are single ended ECL and the clock input is differential.

The internal impedance of the data and clock inputs is a high impedance (FET gate), and is clamped to the digital supply and ground to protect against ESD damage. ESD precautions should still be used when handling the DAC650.

The inputs will most likely be driven by high-speed ECL gate outputs. These outputs should be terminated using standard high-speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC650. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC650 analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 3). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. Above 256MHz, parallel termination of the transmission line at the package pin may be required for clean digital input.

The input data threshold level is set by connecting the appropriate voltage (–1.2V to –1.4V) to pin 1. The actual level may be provided 3 ways:

(1) The user connects the DAC650's internal –1.3V threshold reference directly to pin 1. This simple connection provides excellent noise margins for ECL levels.

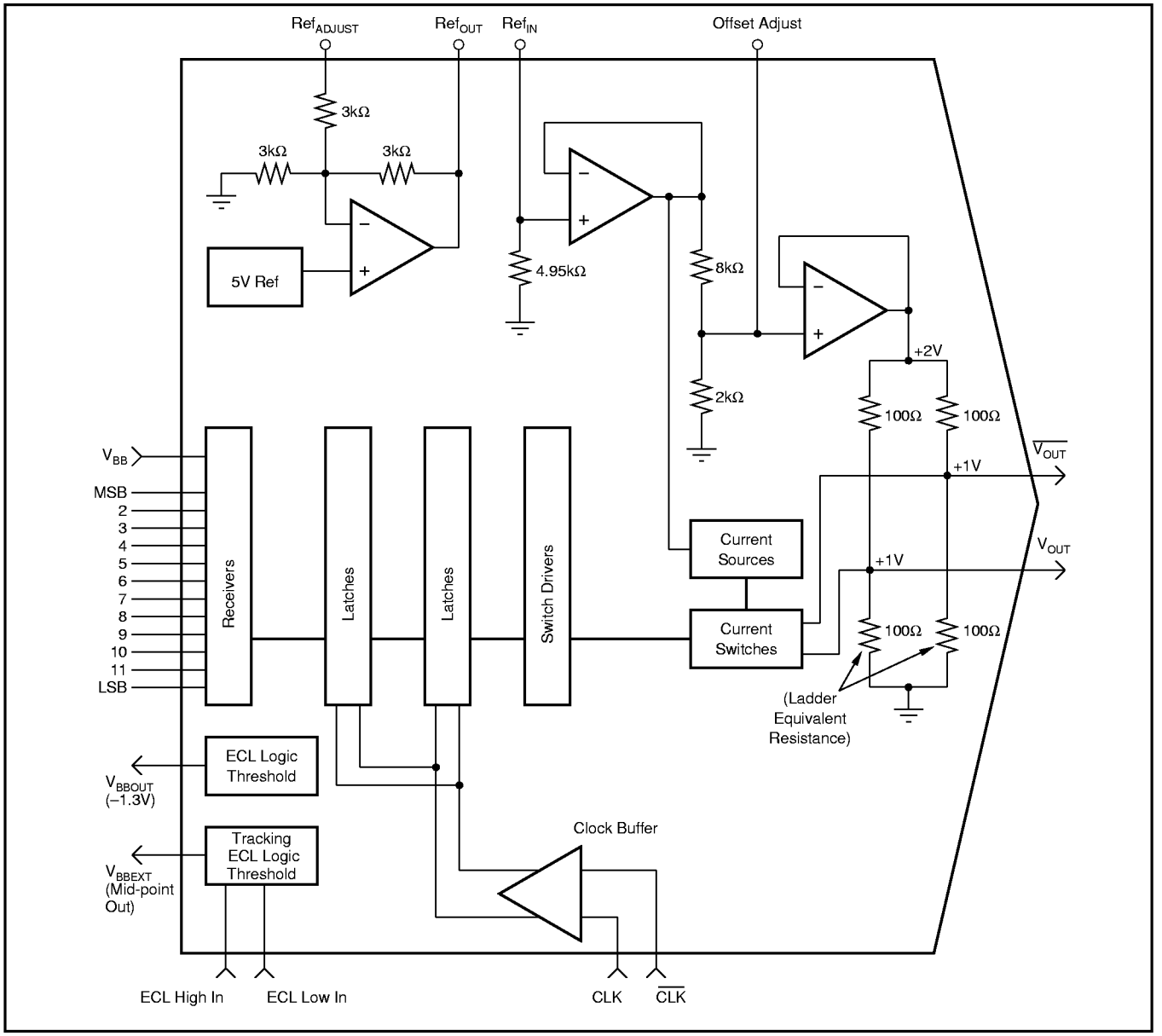


FIGURE 1. Functional Block Diagram of the DAC650.

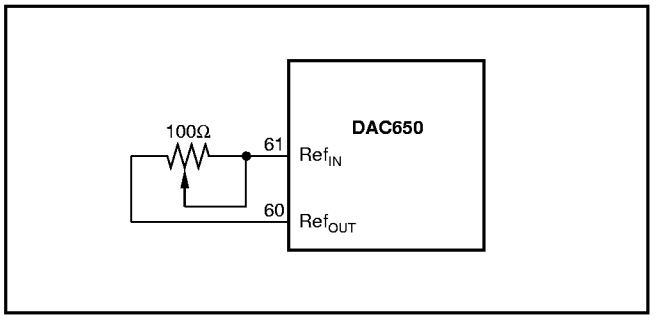


FIGURE 2. Using a Potentiometer for ±1% Gain Adjust.

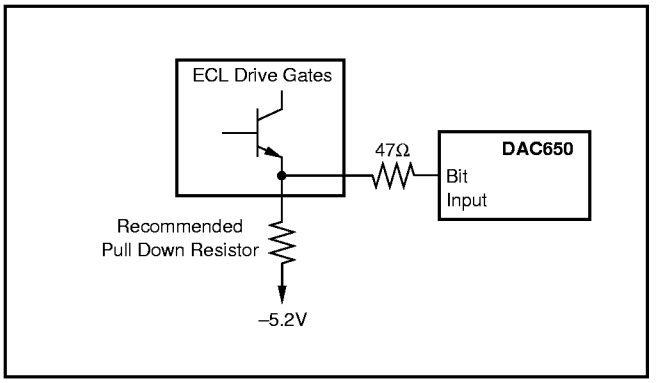


FIGURE 3. Series Bit Termination.

(2) An external V_{BB} system reference is applied to pin 1. This technique may allow data threshold levels to track the system over supply and temperature variations.

(3) The internal tracking ECL threshold reference (pin 67) is applied to pin 1. The output of the tracking ECL threshold reference is simply the average of two externally applied levels. These levels are a system logic low (pin 65) and system logic high (pin 66). This technique may provide increased noise margin for systems with levels slightly different from ECL. Leave pins 65-67 open if this option is not used.

TIMING

The DAC650 has an internal edge triggered latch. The output changes on the positive edge of CLK. This master-slave latching will assure that the 12 bits will arrive at the bit switches with a minimum of data skew. Data must have adequate setup and hold time for proper operation (refer to Figure 4). Note that the Hold time is negative. Therefore the data may change before the rising edge of clock and still be valid.

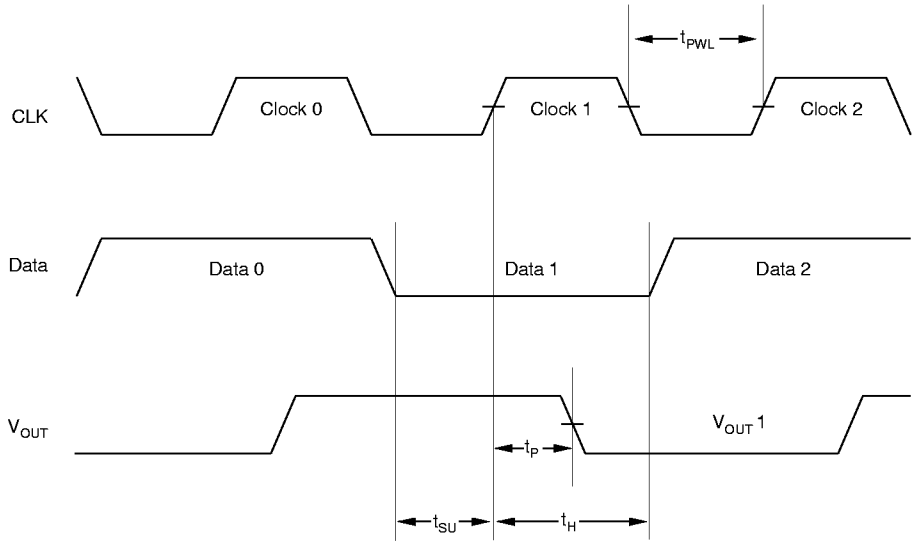
The DAC650 has a differential ECL clock input. This clock input can also be driven by a single-ended clock if desired by tying the $\overline{CLK}$ input to an external voltage of –1.3V. Using a true differential clock provides much improved digital feedthrough immunity, however.

DATA IN/VOUT CORRESPONDENCE

The each full scale output of the DAC650 may be modeled as either ±20mA current source in parallel with 50Ω or a ±1V voltage source in series with 50Ω. The nominal current and voltage bit weights are given in Table I and the input code vs output voltage relationships are given in Table II.

Transmission line techniques at the output are also recommended to minimize ringing and glitching. Ideally, both of the outputs should see the same termination, including any delay between the DAC650 and the load.

Since the outputs V_{OUT} and $\overline{V_{OUT}}$ are equal in magnitude but opposite in sign, they are ideal for driving RF transformers (Figures 5). The primary may be connected between the two outputs. The secondary may be floating or referenced to ground. This results in a 2X signal power and some cancellation of clock feedthrough, glitching, and distortion. Figures 6 and 7 give recommended output amplifiers.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		1.5		ns
t_{SU}	Setup time DATA must remain stable before CLK.	2.0	1.8		ns
t_H	Hold time DATA must remain stable after CLK.	–500	–600		ps
t_{PWL}	CLK pulse width low (50% to 50%).	1.0			ns

FIGURE 4. Timing Diagram for the DAC650.

If only one output is used, the unused output should be terminated identically. If the terminations cannot be identical and the unused output must be unterminated, the termination for the used output should be as close as possible to the DAC650.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. An example of a typical circuit configuration is given in Figures 8. The DAC650 has multiple ground pins to minimize pin impedances. All of the ground pins (analog and digital both) should be connected directly to the analog ground plane at the DAC650.

Wide busses for the power paths are recommended as good general practice. There are several internal power supply bypass capacitors, but external bypassing is still recommended. A 10µF tantalum capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

Pin 64, Analog V_{EE}, should be connected to the same supply as the digital V_{EE} pins (–5.2V).

BIT	VOLTAGE (No External Load)	CURRENT
1	1V	20mA
2	.5V	10mA
3	0.25V	5mA
4	0.125V	2.5mA
5	62.5mV	1.25mA
6	31.25mV	625µA
7	15.625mV	312.5µA
8	7.8125mV	156.25µA
9	3.9063mV	78.125µA
10	1.9531mV	39.06µA
11	976µV	19.53µA
12 (LSB)	488µV	9.76µA

TABLE I. Nominal Bit Weight Values.

INPUT BITS 1 2 3 4 5 6 7 8 9 10 11 12	V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0	+1.000	–1 + 488µV
0 0 0 0 0 0 0 0 0 0 0 1	+1 – 488µV	–1 + 976µV
0 0 0 0 0 0 0 0 0 0 1 0	+1 – 976µV	–1 + 1.464mV
•		
•		
•		
•		
0 1 0 0 0 0 0 0 0 0 0 0	0.50	–0.50 + 488µV
1 0 0 0 0 0 0 0 0 0 0 0	0.000	+488µV
1 1 1 1 1 1 1 1 1 1 1 1	–1 + 488µV	+1.000

TABLE II. Input Code vs Output Voltage Relationships.

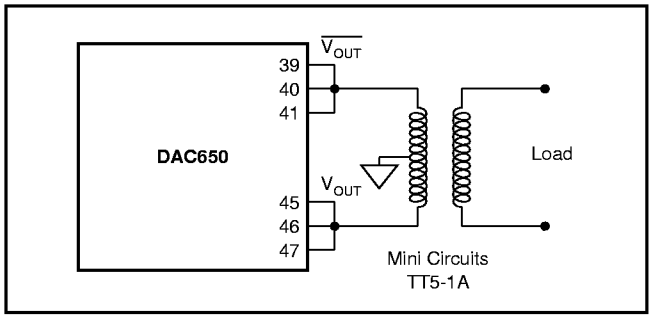


FIGURE 5. Using an RF Transformer at the Output of the DAC650. Filtering the Outputs Before the Transformer Improves the Performance in Some Applications.

MAXIMIZING PERFORMANCE

The DAC650 has been designed to give a very clean analog output with minimal noise, overshoot, and ringing. In addition to optimizing the layout and ground of the DAC650, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC650 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. We have defined Spurious Free Dynamic Range as any harmonic or non-harmonic spurs in the indicated bandwidth . In phase lock loop applications, the harmonics often fall outside the loop bandwidth of the PLL. In these cases, as well as cases where the output is filtered, Spurious

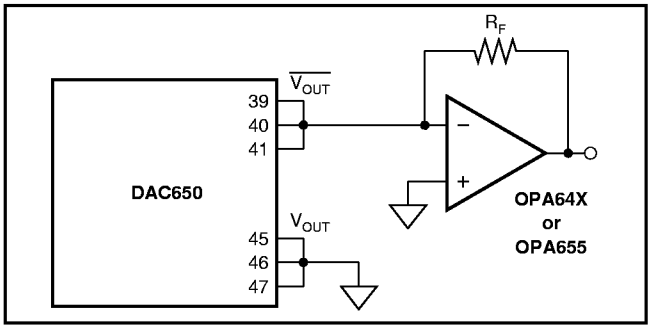


FIGURE 6. A High Speed Single Ended Amplifier at the Output. The Gain is $-R_F/50\Omega$.

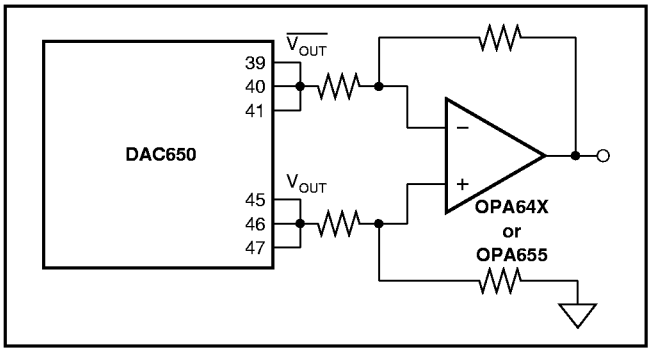


FIGURE 7. A High Speed Differential Amplifier at the Output.

Free Dynamic Range will generally be much better due to the harmonics falling outside the passband. Even with a bandpass filter, updating the DAC at greater than 4 times per cycle will (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (2) will keep the ($f_{CLK} - 2f_O$) spur and other even order spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/3f_{CLK}$ and (3) will keep the ($f_{CLK} - 3f_O$) spur and other spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/4f_{CLK}$. Making use of the high update rate of the DAC650 helps to lessen the problems of harmonics "folding back" into the passband.

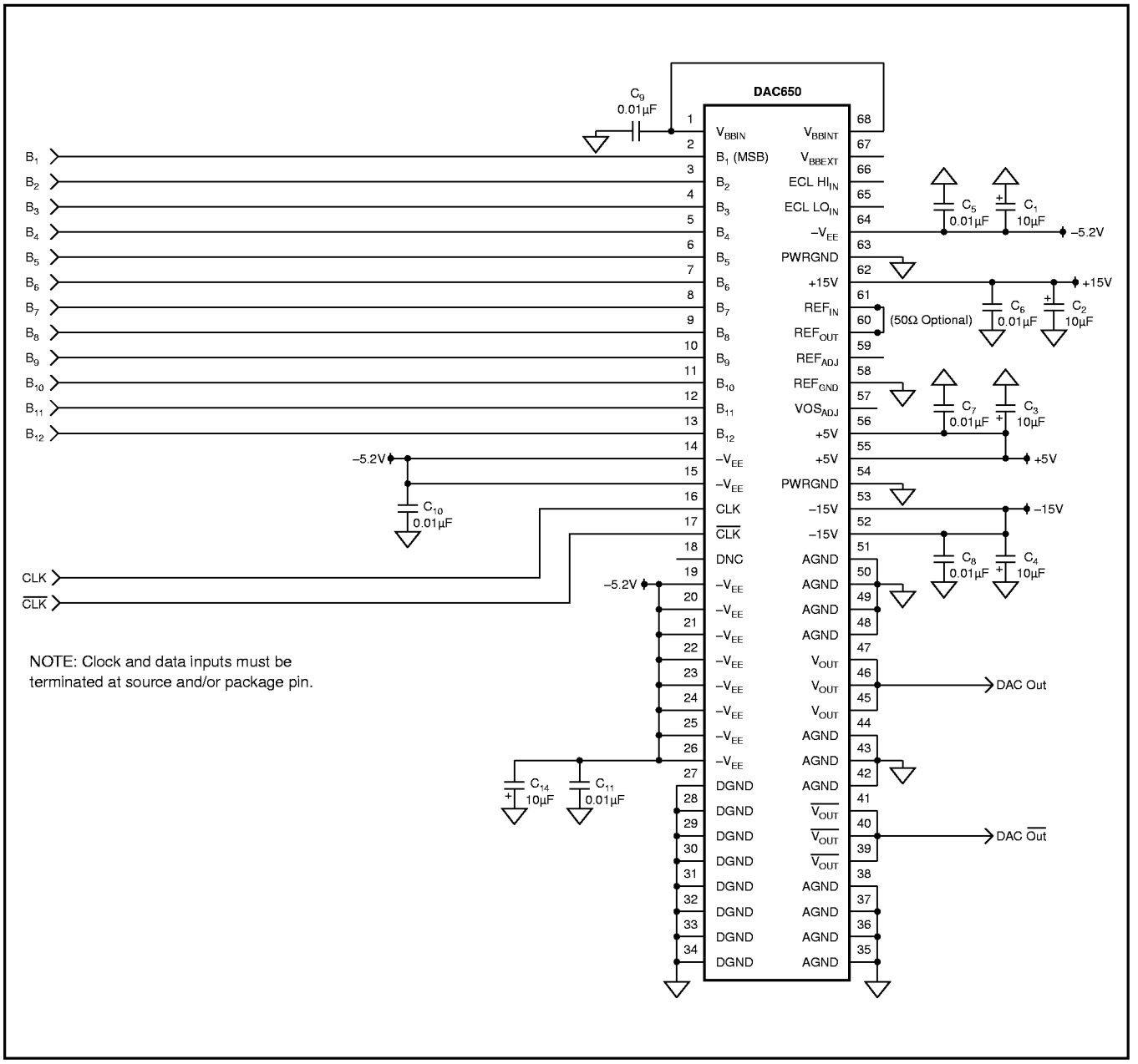


FIGURE 8. Typical DAC650 Connection Diagram.