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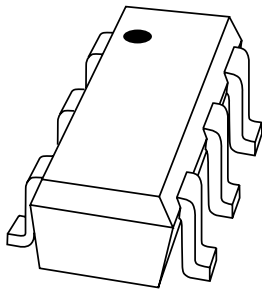
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Kind regards,

Team Nexperia

# DATA SHEET



**PBSS5320D**

20 V low  $V_{CEsat}$  PNP transistor

# 20 V low $V_{CEsat}$ PNP transistor

# PBSS5320D

### FEATURES

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation

### APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

### DESCRIPTION

PNP low  $V_{CEsat}$  transistor in a SOT457 (SC-74) plastic package.

### MARKING

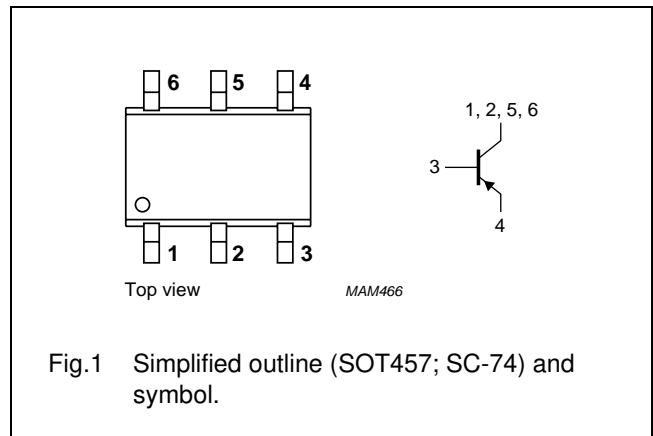
TYPE NUMBER	MARKING CODE
PBSS5320D	52

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	-20	V
$I_C$	collector current (DC)	-3	A
$I_{CM}$	peak collector current	-5	A
$R_{CEsat}$	equivalent on-resistance	133	m $\Omega$

### PINNING

PIN	DESCRIPTION
1	collector
2	collector
3	base
4	emitter
5	collector
6	collector



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–20	V
$V_{CEO}$	collector-emitter voltage	open base	–	–20	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–3	A
$I_{CM}$	peak collector current		–	–5	A
$I_B$	base current		–	–500	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	600	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	750	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.
2. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 6 cm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	208	K/W
		note 2	160	K/W

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.
2. Device mounted on a printed-circuit board, single side copper, tinplated, mounting pad for collector 6 cm<sup>2</sup>.

20 V low  $V_{CEsat}$  PNP transistor

PBSS5320D

**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MIN.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -20\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -20\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -1000\text{ mA}; \text{note 1}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -2000\text{ mA}; \text{note 1}$	150	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -5\text{ mA}$	–	–	–130	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–	–80	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–160	mV
		$I_C = -2\text{ A}; I_B = -20\text{ mA}; \text{note 1}$	–	–	–400	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–250	mV
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	–	–400	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	85	133	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	–1.2	–	–	V
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	50	pF
$F_T$	transition frequency	$I_C = -200\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	100	–	–	MHz

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

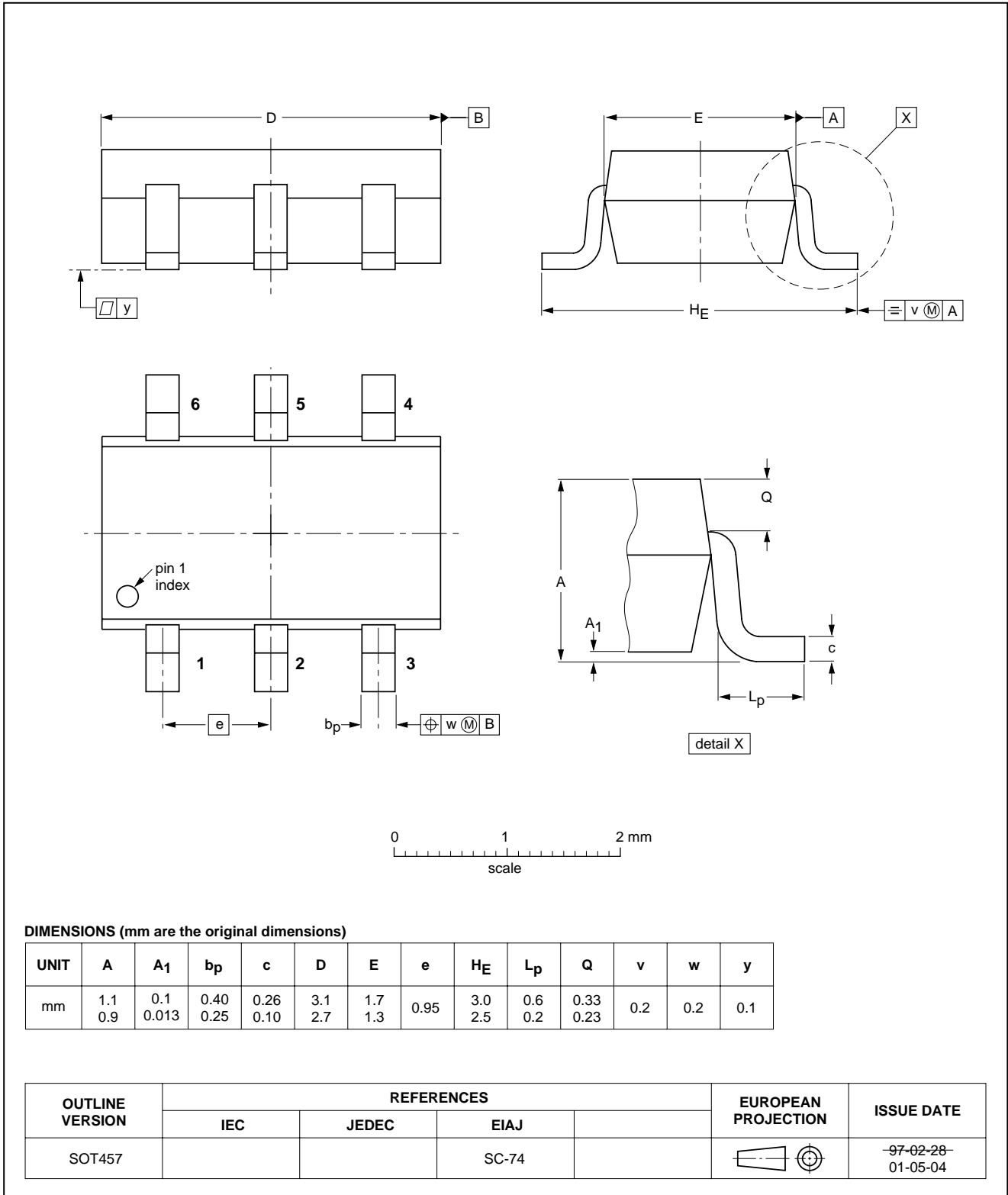
20 V low  $V_{CEsat}$  PNP transistor

PBSS5320D

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



20 V low  $V_{CEsat}$  PNP transistor

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**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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# ***NXP Semiconductors***

## **Customer notification**

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## **Contact information**

For additional information please visit: **<http://www.nxp.com>**

For sales offices addresses send e-mail to: **[salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)**

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