

Quad SPST/Dual SPDT Beyond-The-Rails Analog Switches

MAX14774, MAX14779

Product Highlights

- Design with Wide Signal Range
 - Wide $\pm 25\text{V}$ Analog Input Signal Range
 - Single 3.0V to 5.5V Supply Voltage
 - 1.62V to 5.5V Flexible Logic Input Levels
- High Performance Analog Switch
 - 2.5 Ω (max) On-Resistance at +85°C
 - 18m Ω (typ) On-Resistance Flatness
 - $\pm 100\text{nA}$ (max) On-Leakage Current at +85°C for MAX14774
 - $\pm 200\text{nA}$ (max) On-Leakage Current at +85°C for MAX14779
 - $\pm 200\text{mA}$ (max) Continuous Current Through Each Switch
 - Short Circuit Protection on Each Switch
 - 147MHz (typ) Signal Bandwidth for MAX14774
- Small 4mm x 4mm 20-Pin TQFN Package
- -40°C to +125°C Operating Temperature Range

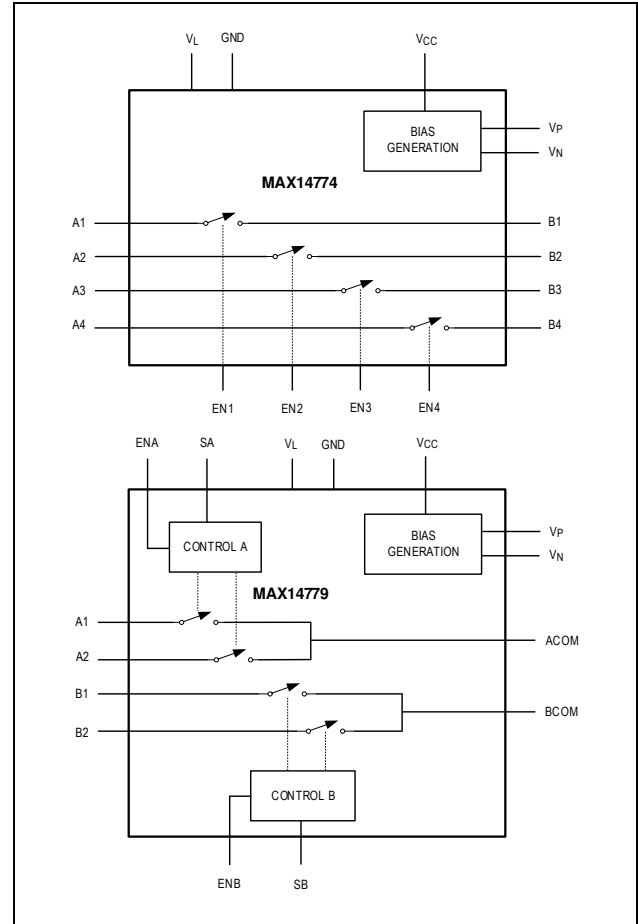
Key Applications

- ATE Systems
- Switching Full Speed USB, CAN, RS-232/485, TTL, Audio
- Instrumentation Systems

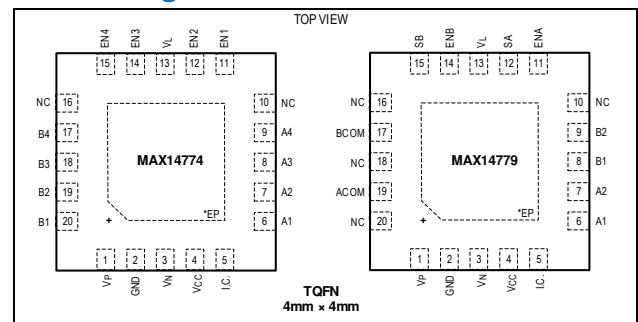
The MAX14774/MAX14779 analog switches support analog signals up to $\pm 25\text{V}$ using a single 3.0V to 5.5V supply. The MAX14774 has four independent analog switches with separate control inputs, while the MAX14779 has two SPDT analog switches. Both parts support separate logic level inputs, allowing flexible CMOS input levels from 1.62V to 5.5V.

The MAX14774/MAX14779 feature a 2.5 Ω (max) on-resistance and an 18m Ω (typ) flatness at +85°C. The MAX14774 has a low $\pm 100\text{nA}$ (max) on-leakage current at +85°C, while the MAX14779 has $\pm 200\text{nA}$ (max). Each switch can carry up to $\pm 200\text{mA}$ (max) of continuous current in either direction. The switches maintain the performance over the entire common-mode voltage range. Both parts are specified for -40°C to +125°C industrial temperature range and are available in a 20 pin (4mm x 4mm) TQFN package.

Simplified Block Diagram



Pin Configuration



[Ordering Information](#) appears at end of data sheet.

Absolute Maximum Ratings

V_{CC}, V_L to GND-0.3V to +6V
 EN₋, SA, SB to GND-0.3V to +6V
 A₋, B₋ to GND (V_N - 0.3V) to the lesser of (V_P + 0.3V) and (V_N + 70V)
 V_P to GND-0.3V to +52V
 V_N, EP to GND... The greater of -40V and (V_P - 70V) to +0.3V
 V_P to V_N-0.3V to +70V
 Absolute Voltage Difference Between I/Os (|A₋ - B₋|) +70V
 Continuous Current Into Any Pin ±200mA

Single-Layer Board (T_A = +70°C, derate 20.8mW/°C above +70°C) 1666.70mW
 Multilayer Board (T_A = +70°C, derate 30.3mW/°C above +70°C) 2424.20mW

Temperature Ratings

Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature -40°C to +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Continuous Power Dissipation

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20 TQFN	
Package Code	T2044+4C
Outline Number	21-100172
Land Pattern Number	90-0409
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ _{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ _{JC})	2°C/W
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ _{JA})	33°C/W
Junction-to-Case Thermal Resistance (θ _{JC})	2°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{CC} = 3.0V to 5.5V, V_L = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C.) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
V _{CC} Supply Voltage	V _{CC}			3.0		5.5	V
V _{CC} Supply Current	I _{CC}	EN ₋ = high	V _{CC} = 3.3V		2.15	4.53	mA
			V _{CC} = 5.5V		0.80	2.06	
Positive High Voltage Charge Pump Output Voltage	V _P	(Note 2)		30.60		36.50	V
Negative High Voltage Charge Pump Output Voltage	V _N	(Note 2)		-29.50		-24.94	V
Logic Level Supply Voltage	V _L			1.62		5.5	V
Logic Level Supply Current	I _L	EN ₋ , A ₋ , B ₋ = low or high		-1		+1	μA
SWITCH CHARACTERISTICS							
Analog Signal Range	V _{A-} , V _{B-}			-25		+25	V
Continuous Current Through Switch	I _{A-}	EN ₋ = high		-200		+200	mA
On-Resistance	R _{ON}	-25V ≤ V _{A-} , V _{B-} ≤ +25V, I _{IN} = ±200mA (Figure 1)	T _A = +85°C		1.15	2.5	Ω
			T _A = +125°C		1.15	3	
On-Resistance Flatness	ΔR _{ON}	-25V ≤ V _{A-} ≤ +25V, I _{IN} = ±200mA			18	120	mΩ
MAX14774 Off-Leakage Current	I _{L_OFFA}	-25V ≤ V _{A-} ≤ +25V, V _{B-} = 0V (Figure 2)	T _A = +85°C		-100	+100	nA
			T _A = +125°C		-300	+300	
	I _{L_OFFB}	-25V ≤ V _{B-} ≤ +25V, V _{A-} = 0V (Figure 2)	T _A = +85°C		-100	+100	
			T _A = +125°C		-300	+300	
MAX14779 Off-Leakage Current	I _{L_OFFA/B}	-25V ≤ V _{A-} , V _{B-} ≤ +25V, V _{ACOM} , V _{BCOM} = 0V (Figure 2)	T _A = +85°C		-200	+200	nA
			T _A = +125°C		-550	+550	
	I _{L_OFFACOM/B COM}	-25V ≤ V _{ACOM} , V _{BCOM} ≤ +25V, V _{A-} , V _{B-} = 0V (Figure 2)	T _A = +85°C		-200	+200	
			T _A = +125°C		-550	+550	
MAX14774 On-Leakage Current	I _{L_ON}	-25V ≤ V _{A-} ≤ +25V, B ₋ is unconnected (Figure 2)	T _A = +85°C		-100	+100	nA
			T _A = +125°C		-300	+300	
MAX14779 On-Leakage Current	I _{L_ON}	-25V ≤ V _{A-} , V _{B-} ≤ +25V, A _{COM} , B _{COM} is unconnected (Figure 2)	T _A = +85°C		-200	+200	nA
			T _A = +125°C		-550	+550	

($V_{CC} = 3.0V$ to $5.5V$, $V_L = 3.3V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$, $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Off Input-Output Leakage Current	$I_{L_IO_OFF}$	$V_{CC} = 0V$ or unconnected, $3V \leq V_{A_} - V_{B_} \leq 50V$. Current measured at A_, B_ pins (Figure 2)	-5		+5	μA
DIGITAL LOGIC (EN_, S_)						
Input Voltage Low Threshold	V_{IL}				$0.3 \times V_L$	V
Input Voltage High Threshold	V_{IH}		$0.7 \times V_L$			V
Input Logic Leakage Current	I_{IL}	$V_{S_}, V_{EN_} = 0V$ or V_L	-1		+1	μA
DYNAMIC CHARACTERISTICS						
Power-Up Time	t_{PWRON}	$V_{A_} = \pm 10V$, $C_{VP} = C_{VN} = 10nF$ (Figure 3) (Note 3)		2.2		ms
Enable Turn-On Time	t_{ON}	$V_{A_} = \pm 10V$, $R_L = 10k\Omega$ (Figure 4)	MAX14774	28	60	μs
			MAX14779	326	600	
Enable Turn-Off Time	t_{OFF}	$V_{A_} = \pm 10V$, $R_L = 10k\Omega$ (Figure 4)	MAX14774	48	160	μs
			MAX14779	48	160	
MAX14779 Break-Before-Make Time	t_{BBM}	$V_{A_} = \pm 10V$, $R_L = 10k\Omega$ (Figure 5)		289	500	μs
MAX14774 Off-Isolation	V_{ISO}	$V_{A_} = 1V_{RMS}$, $f = 100kHz$, $R_L = 50\Omega$, $C_L = 15pF$ (Figure 6)	$V_{CC} = 3V$ to $5.5V$	-80		dB
			$V_{CC} = 0V$ or unconnected	-75		
MAX14779 Off-Isolation	V_{ISO}	$V_{A_} = 1V_{RMS}$, $f = 100kHz$, $R_L = 50\Omega$, $C_L = 15pF$ (Figure 6)	$V_{CC} = 3V$ to $5.5V$	-80		dB
			$V_{CC} = 0V$ or unconnected	-75		
MAX14774 Crosstalk	V_{CT}	$V_{A_} = 1V_{RMS}$, $f = 100kHz$, $R_S = R_L = 50\Omega$, $C_L = 15pF$ (Figure 7)	$V_{CC} = 3V$ to $5.5V$	-90		dB
			$V_{CC} = 0V$ or unconnected	-75		
MAX14779 Crosstalk	V_{CT}	$V_{A_} = 1V_{RMS}$, $f = 100kHz$, $R_S = R_L = 50\Omega$, $C_L = 15pF$ (Figure 7)	$V_{CC} = 3V$ to $5.5V$	-90		dB
			$V_{CC} = 0V$ or unconnected	-80		
-3dB Bandwidth	BW	$V_{A_} = 2V_{PP}$, $R_S = R_L = 50\Omega$, $C_L = 15pF$ (Figure 8)	MAX14774	147		MHz
			MAX14779	78		
Charge Injection	Q	$V_{A_} = GND$, $C_L = 1nF$ (Figure 9)	MAX14774	780		pC
			MAX14779	850		
MAX14774 Input Capacitance	C_{ON}	A_, B_ pins, $f = 12MHz$, EN_ = high		37		pF
	C_{OFF}	At A_ when B_ = GND, or at B_ when A_ = GND, $f = 1MHz$, EN_ = low		31		
	C_{ON}	A_, B_ pins, $f = 12MHz$, EN_ = high		61		pF

($V_{CC} = 3.0V$ to $5.5V$, $V_L = 3.3V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$, $T_A = +25^{\circ}C$.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX14779 Input Capacitance	C_{OFF}	At ACOM when $A_- = GND$ or at BCOM when $B_- = GND$, $f = 1MHz$, $EN_- = low$		54		
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising		+162		$^{\circ}C$
Thermal Shutdown Threshold Hysteresis	T_{HYST}			23		$^{\circ}C$
ESD PROTECTION						
All pins	V_{ESD}	Human Body Model		± 2		kV

Note 1: All units are production tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 2: Do not use V_P or V_N to power external circuitry. Connect at least 10nF/100V capacitor to both V_P and V_N with respect to GND.

Note 3: Power-up time is the time needed for V_P and V_N to reach steady-state.

Timing Diagrams and Test Circuits

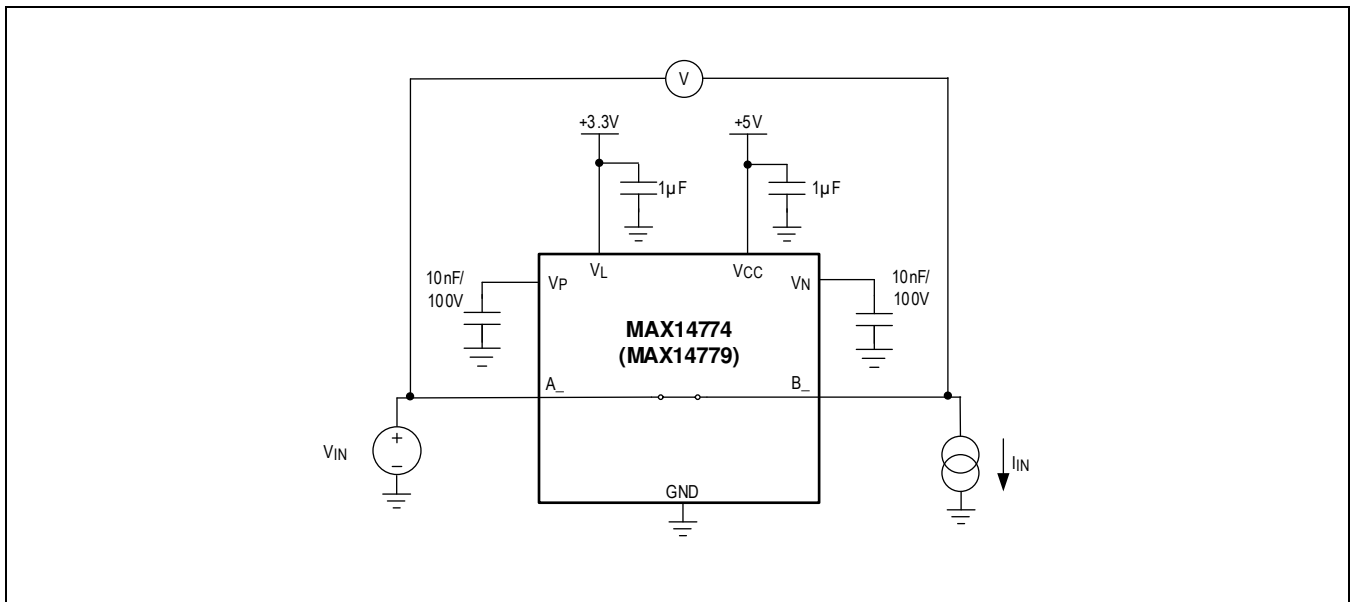


Figure 1. On-Resistance Measurement

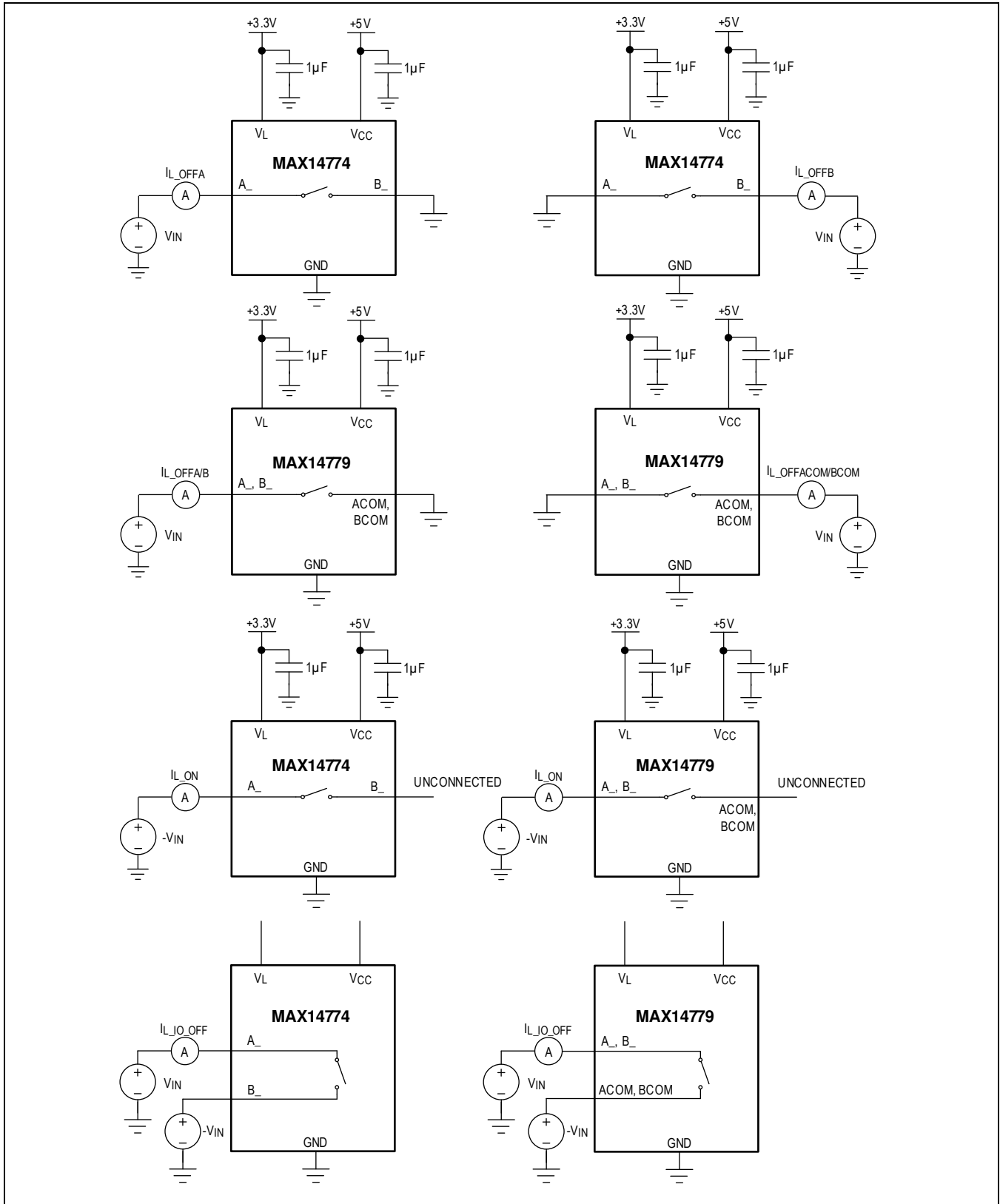


Figure 2. Leakage Current Measurements

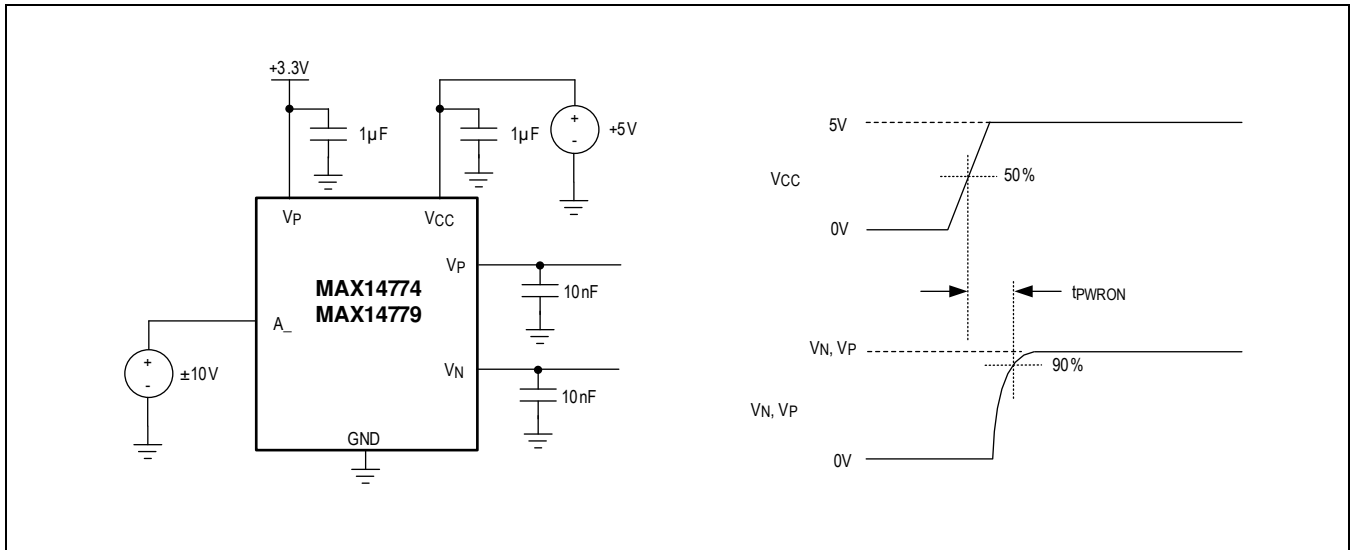


Figure 3. Power-Up Time Measurement

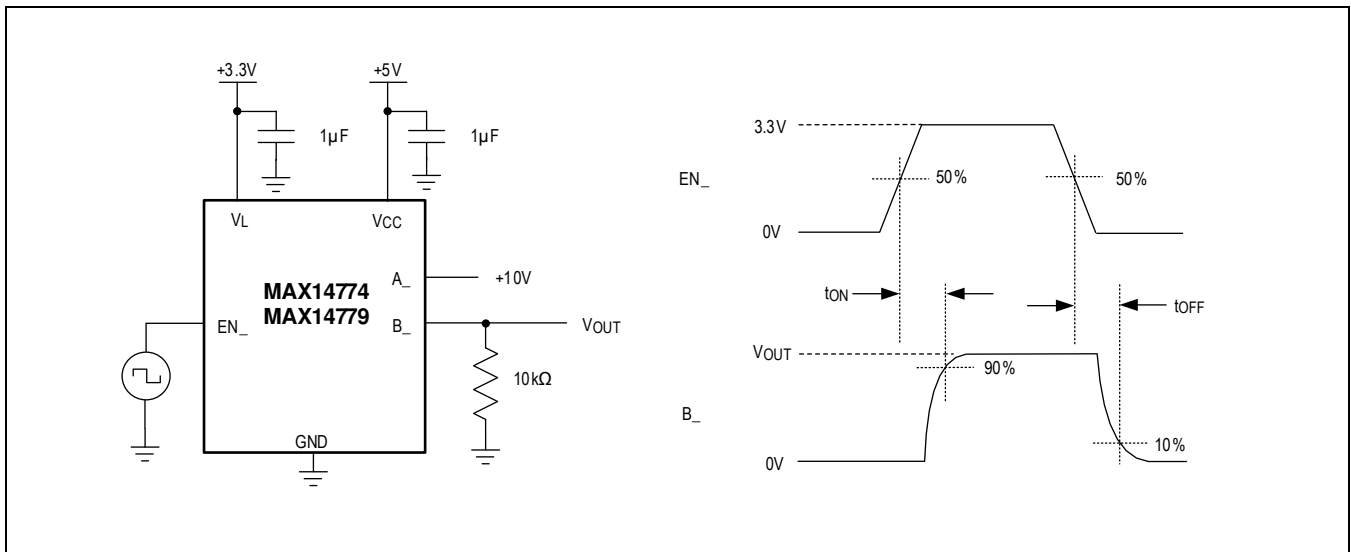


Figure 4. Turn-On and Turn-Off Time Measurement

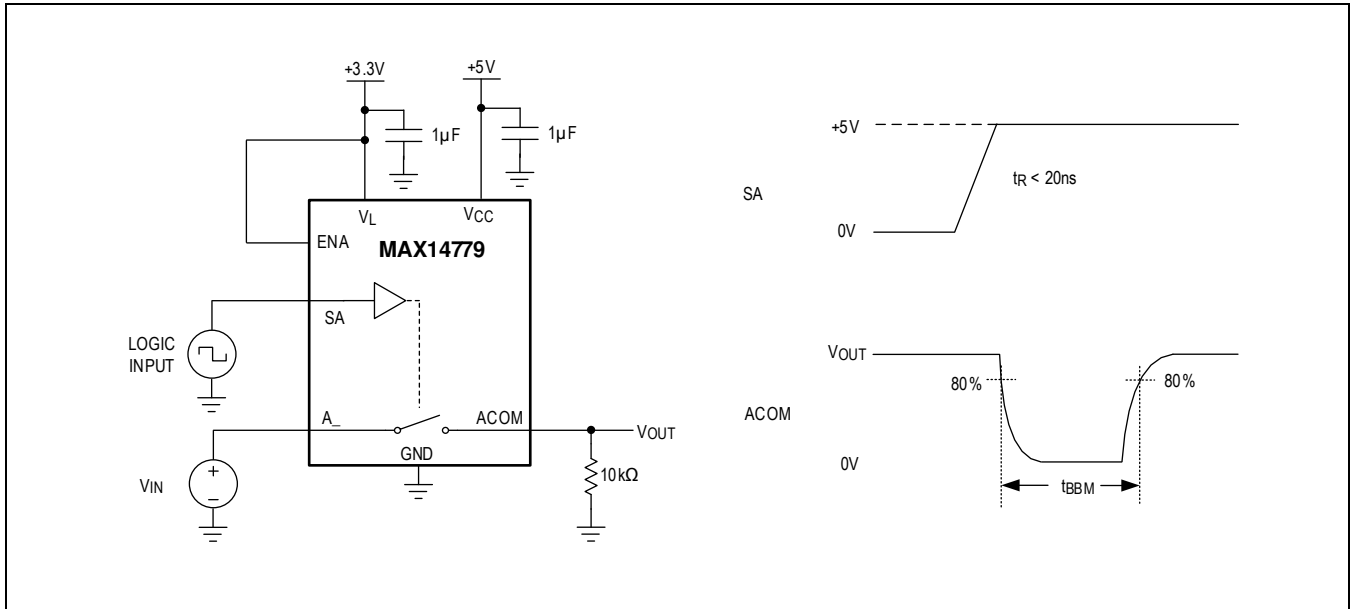


Figure 5. Break Before Make Time Measurement

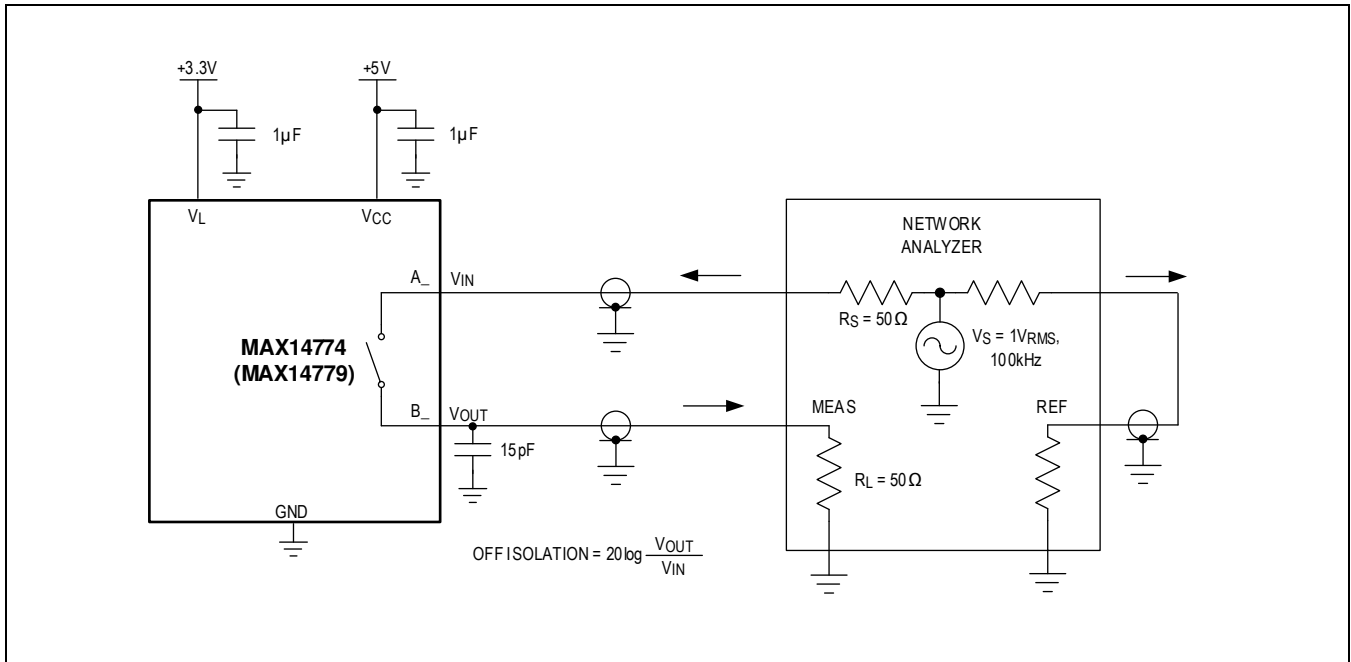


Figure 6. Off Isolation Measurement

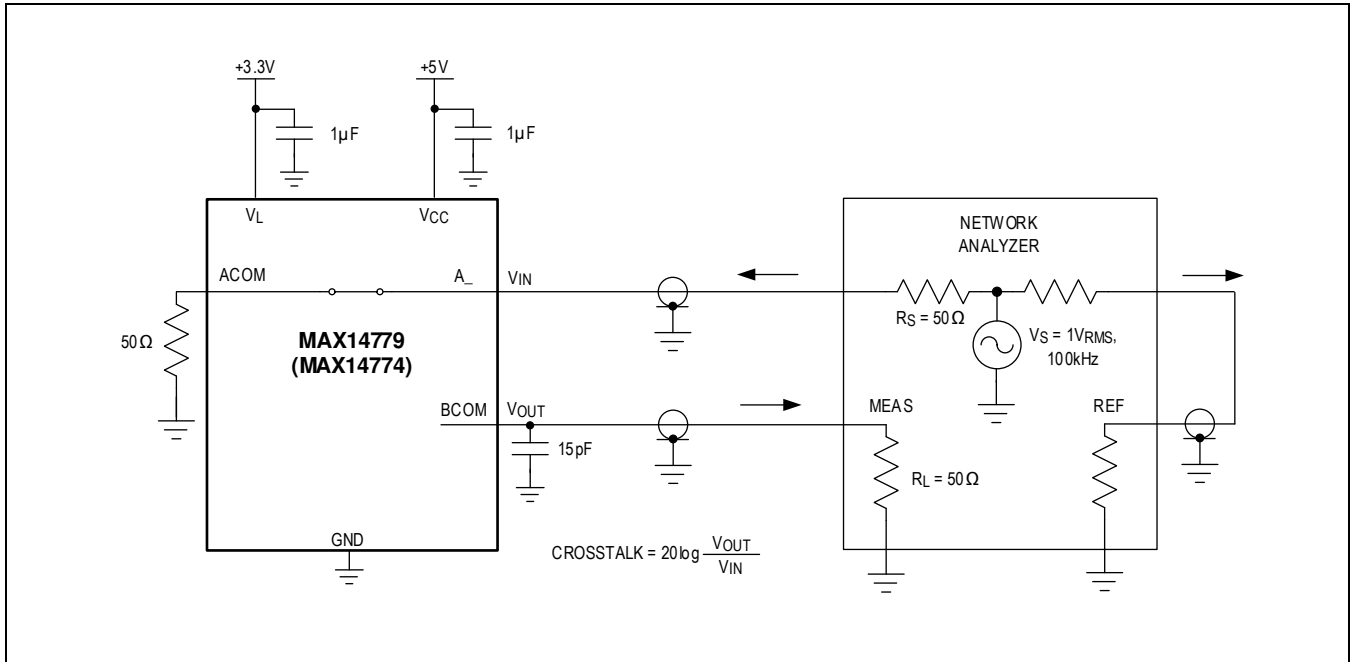


Figure 7. Crosstalk Measurement

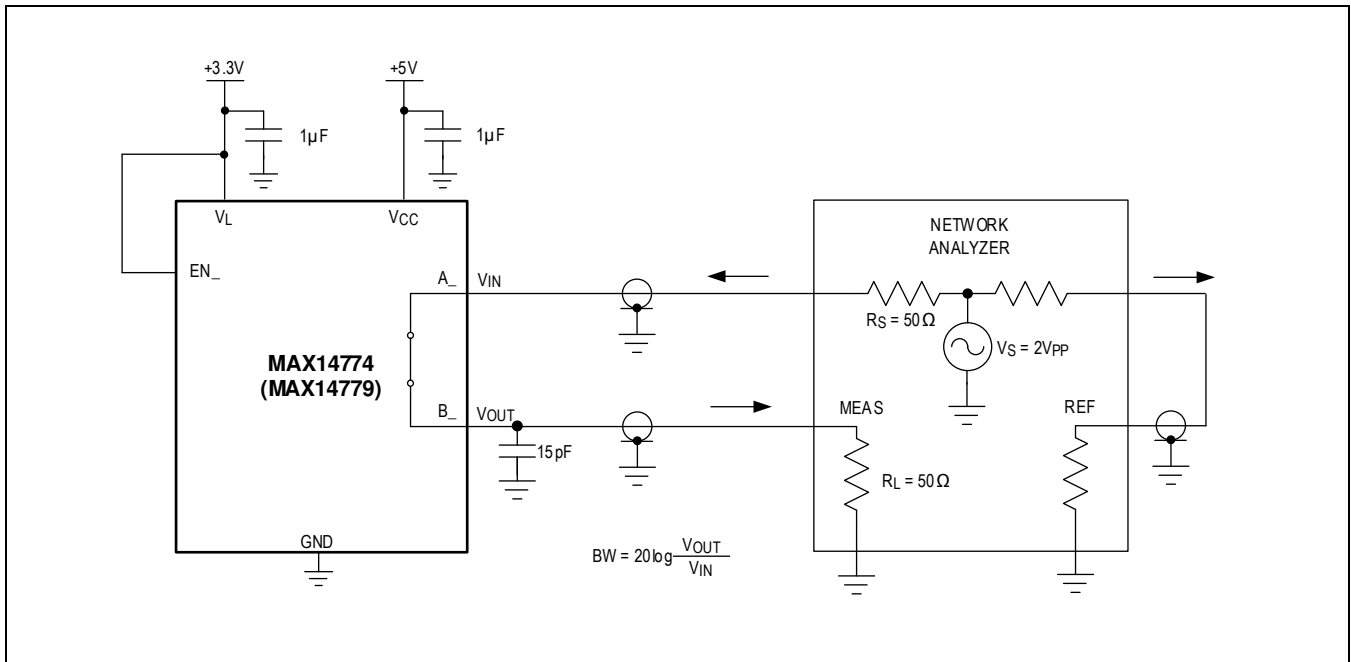


Figure 8. Frequency Response Measurement

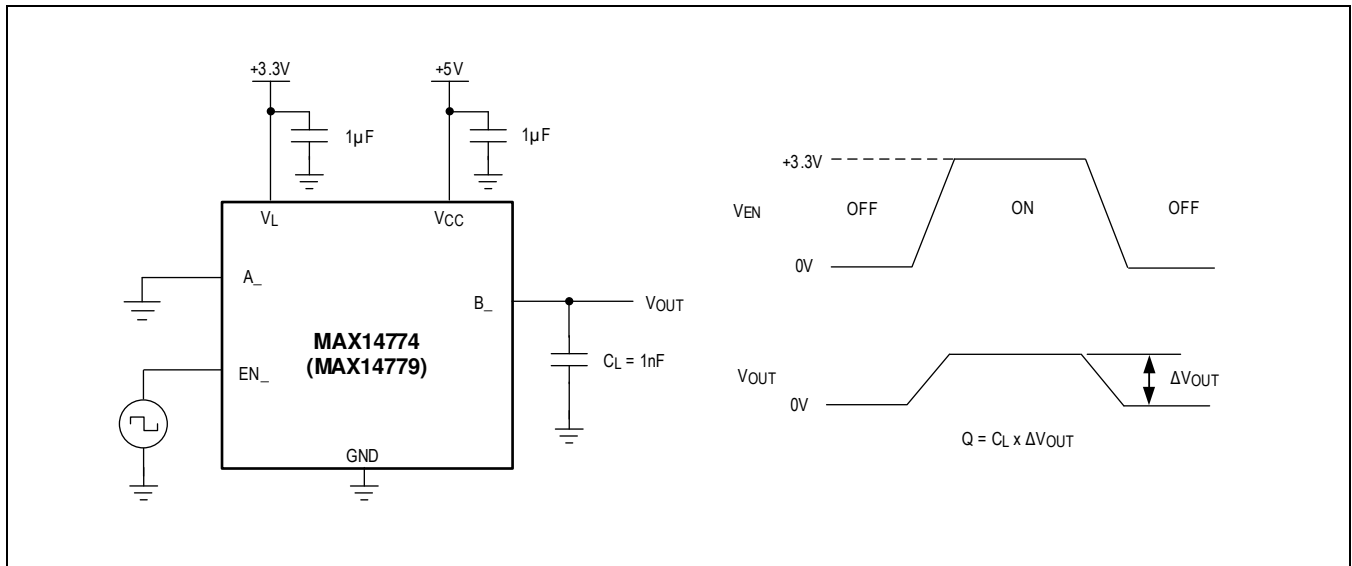
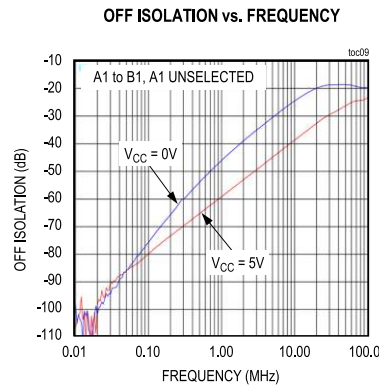
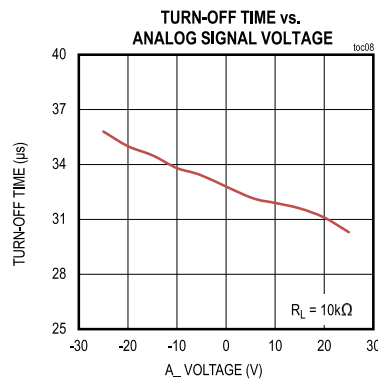
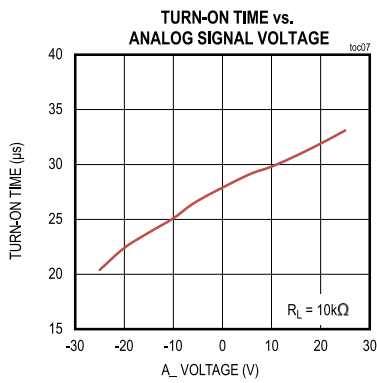
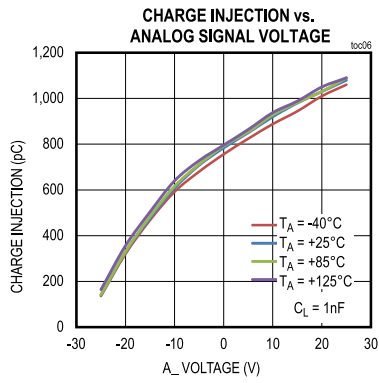
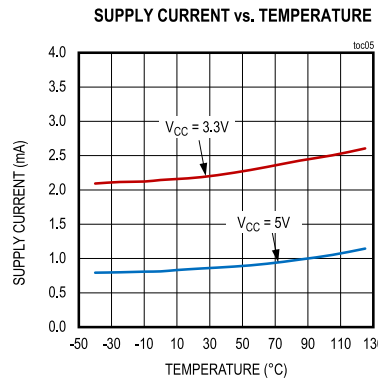
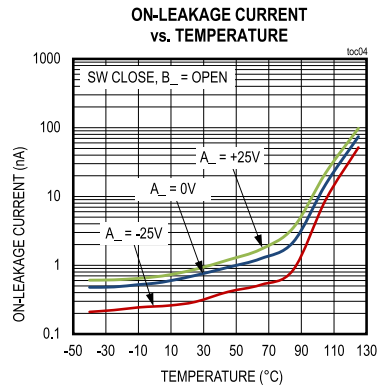
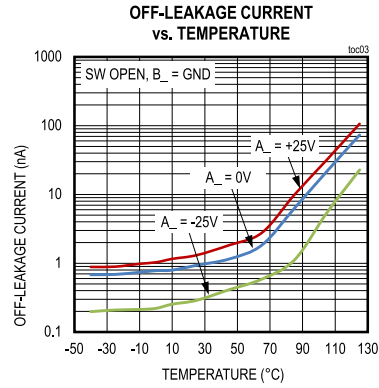
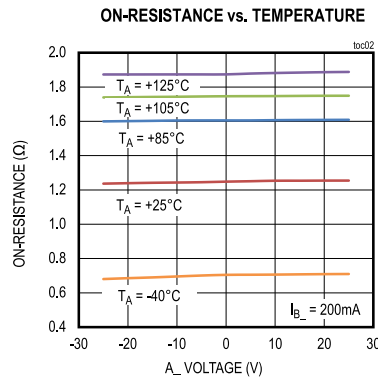
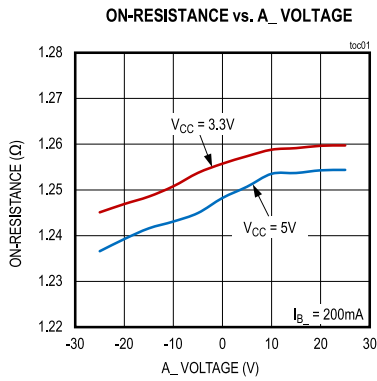


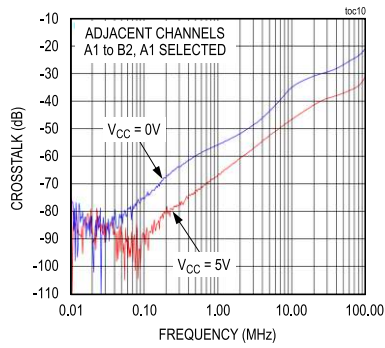
Figure 9. Charge Injection Measurement

Typical Operating Characteristics – MAX14774

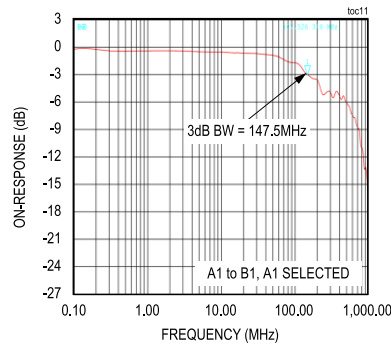
V_{CC} = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.



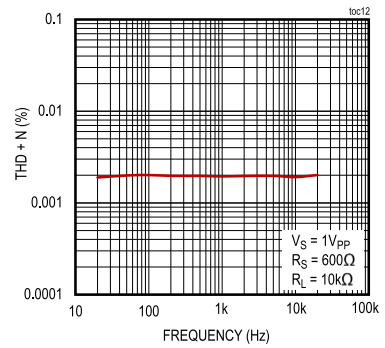
CROSSTALK vs. FREQUENCY



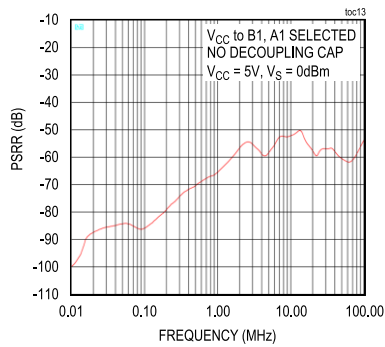
FREQUENCY RESPONSE



THD + N vs. FREQUENCY

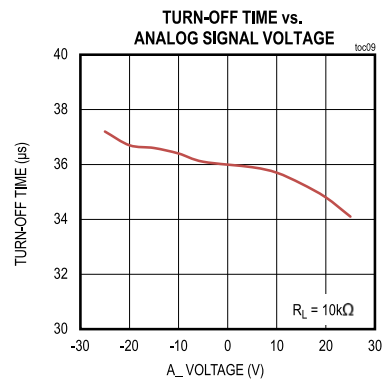
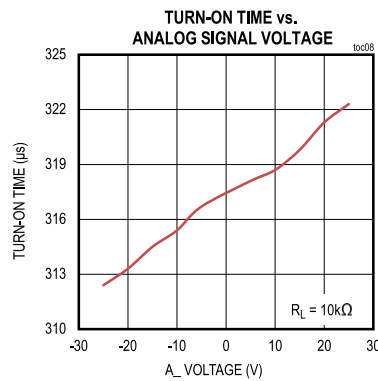
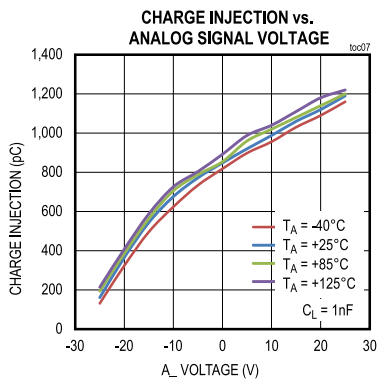
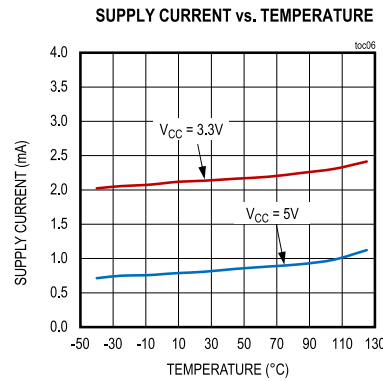
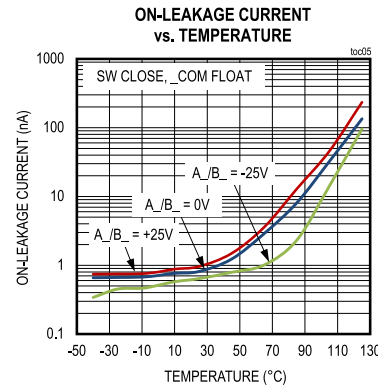
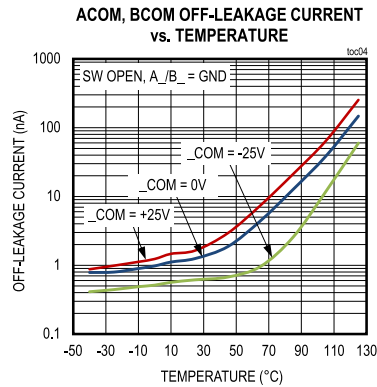
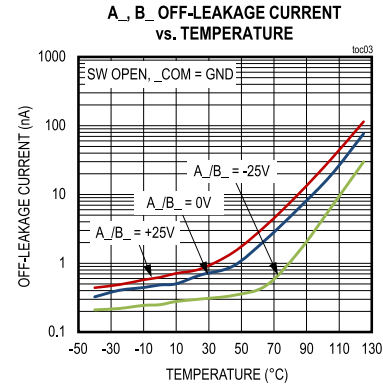
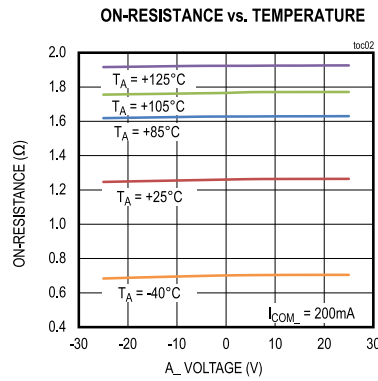
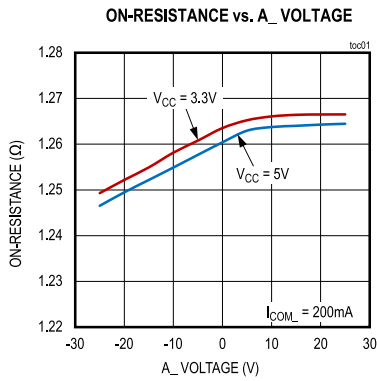


PSRR vs. FREQUENCY

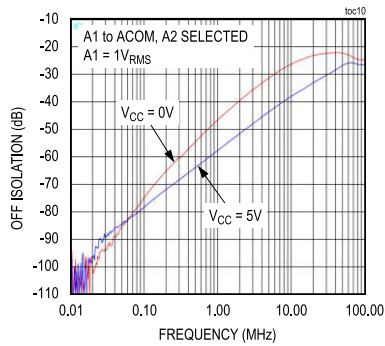


Typical Operating Characteristics – MAX14779

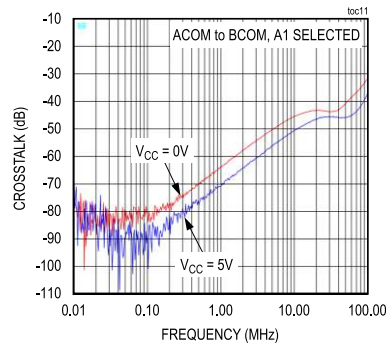
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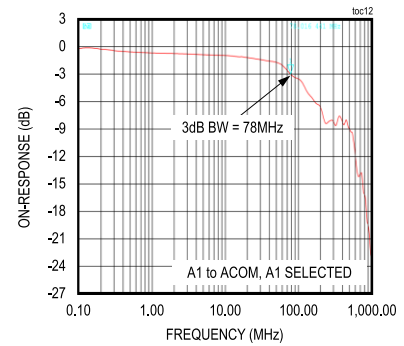
OFF ISOLATION vs. FREQUENCY



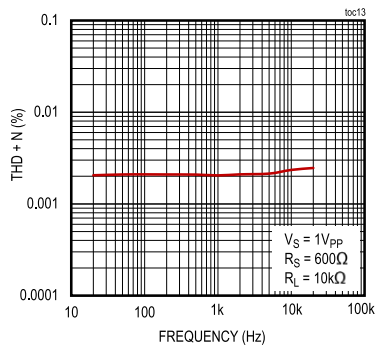
CROSSTALK vs. FREQUENCY



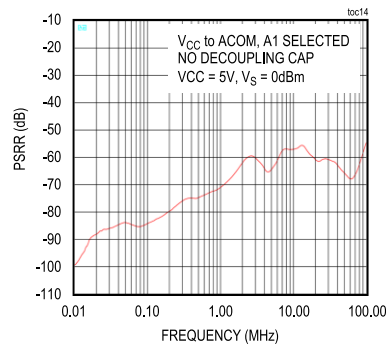
FREQUENCY RESPONSE



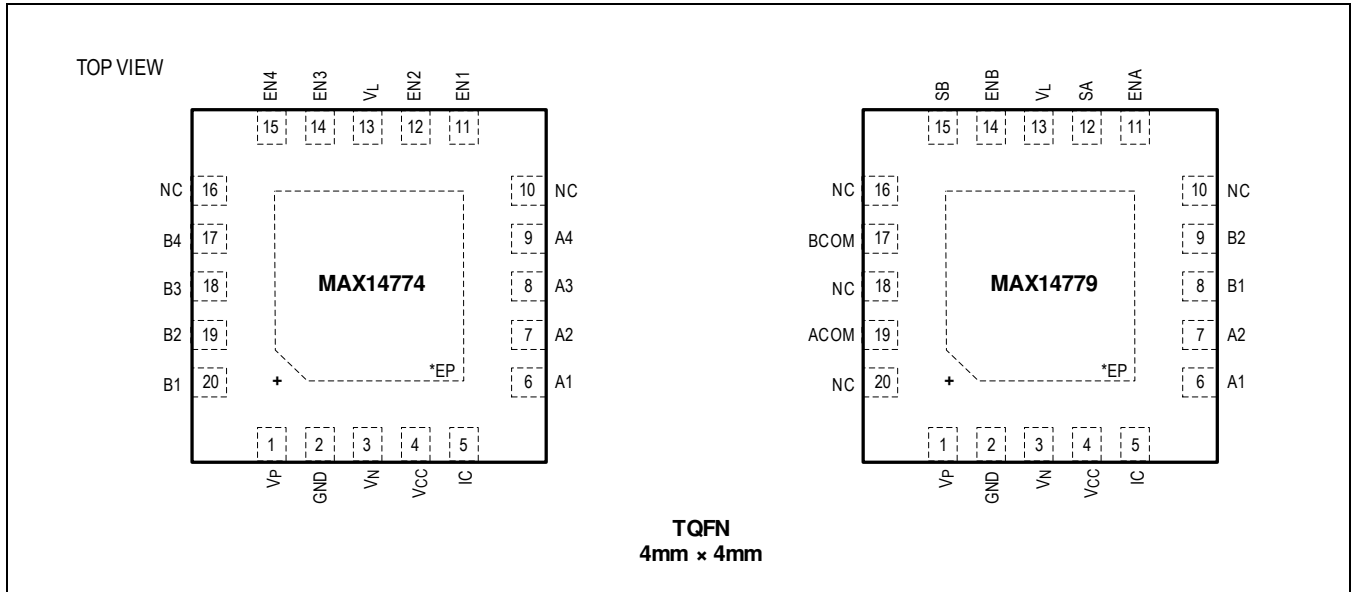
THD + N vs. FREQUENCY



PSRR vs. FREQUENCY



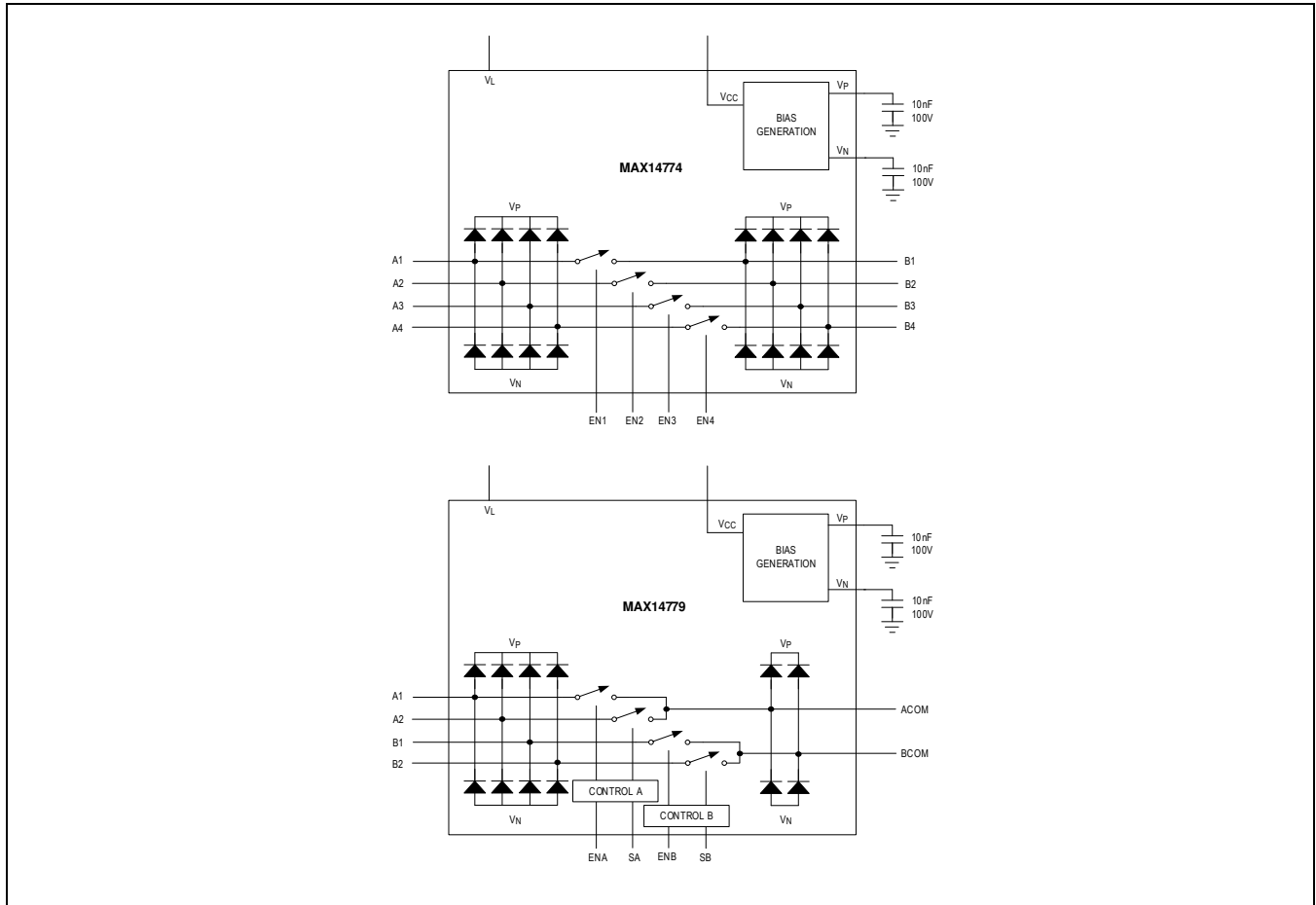
Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
MAX14774	MAX14779		
1	1	V _P	Positive Charge-Pump Output. Bypass V _P to GND with a 10nF/100V ceramic capacitor placed as close as possible to the device.
2	2	GND	Ground.
3	3	V _N	Negative Charge-Pump Output. Bypass V _N to GND with a 10nF/100V ceramic capacitor placed as close as possible to the device.
4	4	V _{CC}	Power Supply Input. Connect to a supply voltage between 3.0V to 5.5V. Bypass V _{CC} to GND with a 1μF ceramic capacitor placed as close as possible to the device.
5	5	I.C.	Internally Connected. Connect to GND.
13	13	V _L	Logic Supply Input. Connect to a supply voltage between 1.62V to 5.5V. Bypass V _L to GND with a 1μF ceramic capacitor placed as close as possible to the device.
EP	EP	EP	Exposed Pad. Connect to V _N .
10, 16	10, 16, 18, 20	N.C.	Not Connected.
ANALOG I/O			
6	6	A1	Analog Switch Terminal A1.
7	7	A2	Analog Switch Terminal A2.
8	-	A3	Analog Switch Terminal A3.
9	-	A4	Analog Switch Terminal A4.
-	19	ACOM	Analog Switch Terminal ACOM.
17	-	B4	Analog Switch Terminal B4.
18	-	B3	Analog Switch Terminal B3.
19	9	B2	Analog Switch Terminal B2.
20	8	B1	Analog Switch Terminal B1.
-	17	BCOM	Analog Switch Terminal BCOM.
CONTROL INPUTS			
11	-	EN1	Switch 1 Control Input. Drive EN1 high to close switch 1. Drive EN1 low to open switch 1.
12	-	EN2	Switch 2 Control Input. Drive EN2 high to close switch 2. Drive EN2 low to open switch 2.
14	-	EN3	Switch 3 Control Input. Drive EN3 high to close switch 3. Drive EN3 low to open switch 3.
15	-	EN4	Switch 4 Control Input. Drive EN4 high to close switch 4. Drive EN4 low to open switch 4.
-	11	ENA	Switch A Enable Input. Drive ENA low to open A1 and A2 switches, independent of the SA input logic. Drive ENA high to enable SA control.
-	12	SA	Switch A Control Input. Drive SA high to close switch A2. Drive SA low to close switch A1. SA operation is conditional on ENA being high.
-	14	ENB	Switch B Enable Input. Drive ENB low to open B1 and B2 switches, independent of the SB input logic. Drive ENB high to enable SB control.
-	15	SB	Switch B Control Input. Drive SB high to close switch B2. Drive SB low to close switch B1. SB operation is conditional on ENB being high.

Functional Diagrams



Detailed Description

The MAX14774 quad SPST and the MAX14779 dual SPDT Beyond-The-Rails switches support switching analog signals of up to $\pm 25\text{V}$ using a single 3.0V to 5.5V supply. The MAX14774 is a quad SPST switch configuration with four EN_ control inputs, and the MAX14779 is a dual SPDT switch configuration with two EN_ and two S_ control inputs. Both the MAX14774 and MAX14779 have a flexible 1.62V to 5.5V CMOS logic interface.

The switches feature 2.5Ω (max) on-resistance and $18\text{m}\Omega$ (typ) flatness at 85°C . The MAX14774 has a low on-leakage current of $\pm 100\text{nA}$ (max) while the MAX14779 has $\pm 200\text{nA}$ (max) at 85°C . The switches maintain the performance over the entire common-mode voltage range to maximum signal integrity. Each device can carry up to 200mA (max) of continuous current in either direction while operating from -40°C to $+125^\circ\text{C}$.

Integrated Bias Generation

The MAX14774/MAX14779 contain a total of three charge pumps to generate bias voltages for the internal switches: a 5V regulated charge pump, a positive high-voltage charge pump (V_P), and a negative high-voltage charge pump (V_N). When the V_{CC} is above 4.75V (typ), the 5V charge pump is bypassed and V_{CC} provides the input for the high-voltage charge pumps, reducing overall supply current. The voltage at V_N is -27V (typ), the voltage at V_P is $+33\text{V}$ (typ), and the analog signal range is $\pm 25\text{V}$.

An external $10\text{nF}/100\text{V}$ (min) capacitor is required for each high-voltage charge pump between V_P/V_N and GND.

Logic Interface Supply

The MAX14774/MAX14779 feature a separate supply control input V_L that sets the high and low thresholds for all logic inputs EN_ and S_. It allows flexible interfacing to controllers with a different logic level other than V_{CC} . Drive V_L with a voltage between 1.62V and 5.5V.

Control Logic

The MAX14774 is a quad SPST analog switch with four enable inputs EN1, EN2, EN3, and EN4. See [Table 1](#) for the switching logic.

Table 1. MAX14774 Control Logic

ENABLE PIN	POSITION	FUNCTION
EN1	0	B1 Open
	1	B1 connected to A1
EN2	0	B2 Open
	1	B2 connected to A2
EN3	0	B3 Open
	1	B3 connected to A3
EN4	0	B4 Open
	1	B4 connected to A4

The MAX14779 is a dual SPDT analog switch with two enable inputs ENA and ENB, and two digital select inputs SA and SB. See [Table 2](#) for the switching logic.

Table 2. MAX14779 Control Logic

ENA POSITION	SA POSITION	ACOM CONNECTED TO
0	X	Open
1	0	A1
1	1	A2
ENB POSITION	SB POSITION	BCOM CONNECTED TO
0	X	Open
1	0	B1
1	1	B2

X is Don't Care.

Applications Information

Non-Powered Condition

To understand the behavior of the MAX14774/MAX14779 when not powered (i.e., $V_{CC} = 0V$), the transient and DC signal conditions should be considered separately.

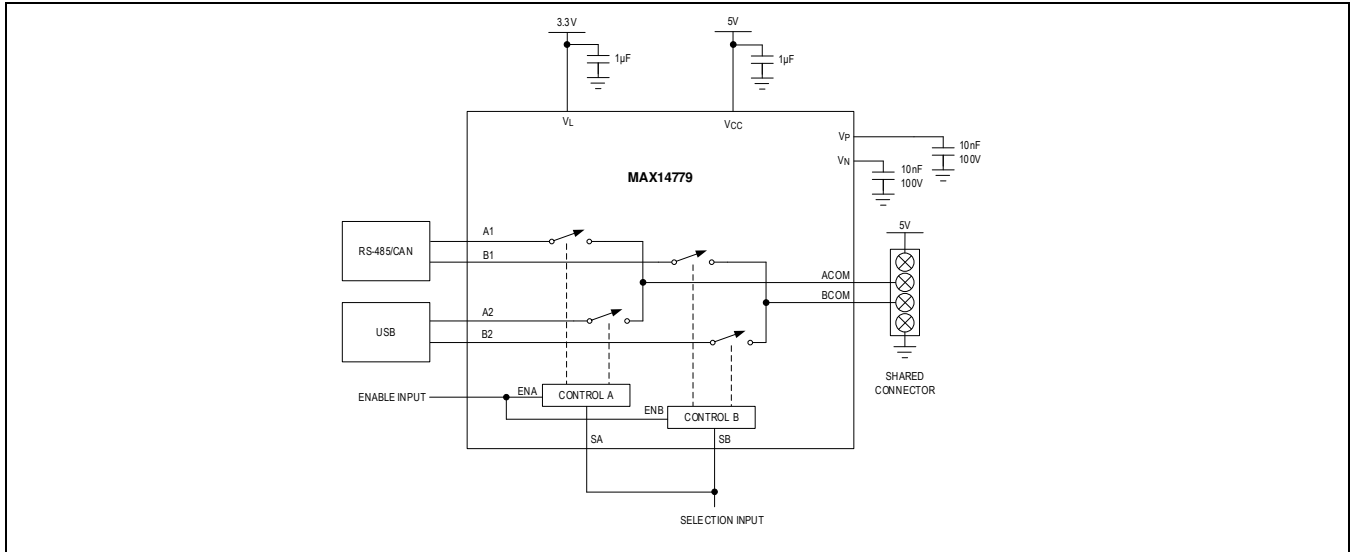
Every A_ and B_ pin has internal diodes connected to V_P and V_N . Applying a positive voltage on A_ or B_ charges the capacitor on V_P through the diode to V_P . Applying a negative voltage on A_ or B_ charges the capacitor on V_N through the diode to V_N . Switch terminals A_ and B_ support voltages ranging from -25V to +25V when the devices are unpowered.

Under transient conditions, the voltages applied to the A_ or B_ pins charge the capacitors on V_P and V_N and at the same time the internal off-leakage current ($I_{L_IO_OFF}$) discharges these capacitors. Thus, the input impedance into the A_ or B_ pin is determined by the capacitors on V_P/V_N and their charge states.

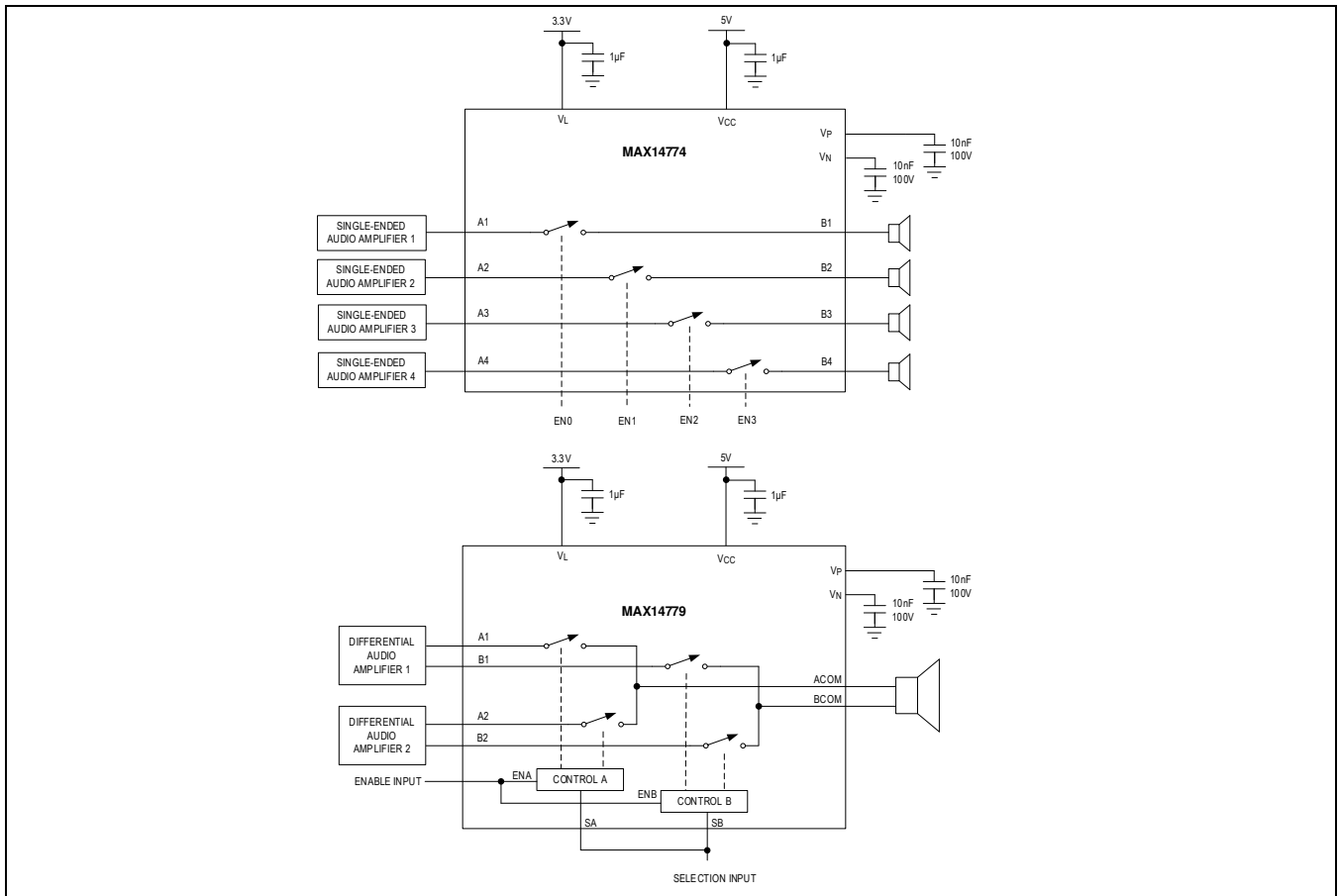
Under DC conditions, when a voltage is applied to an A_ or B_ pin with V_{CC} unpowered, the switch is open when the voltage difference between the A_ and B_ pin is larger than 3V. Under these conditions, the DC leakage current flows into the pin. When $|V_{A_} - V_{B_}| < 3V$, the switch is not fully open, and currents up to a few mA can flow between the A_ and B_ pins.

Typical Application Circuits

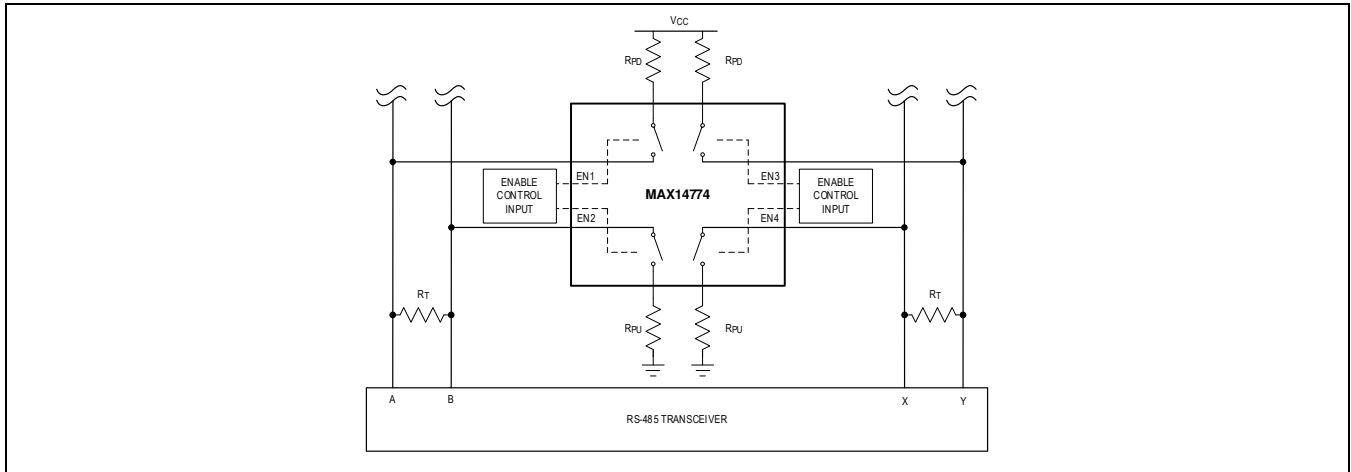
Switching between RS-485/CAN and USB Transceivers



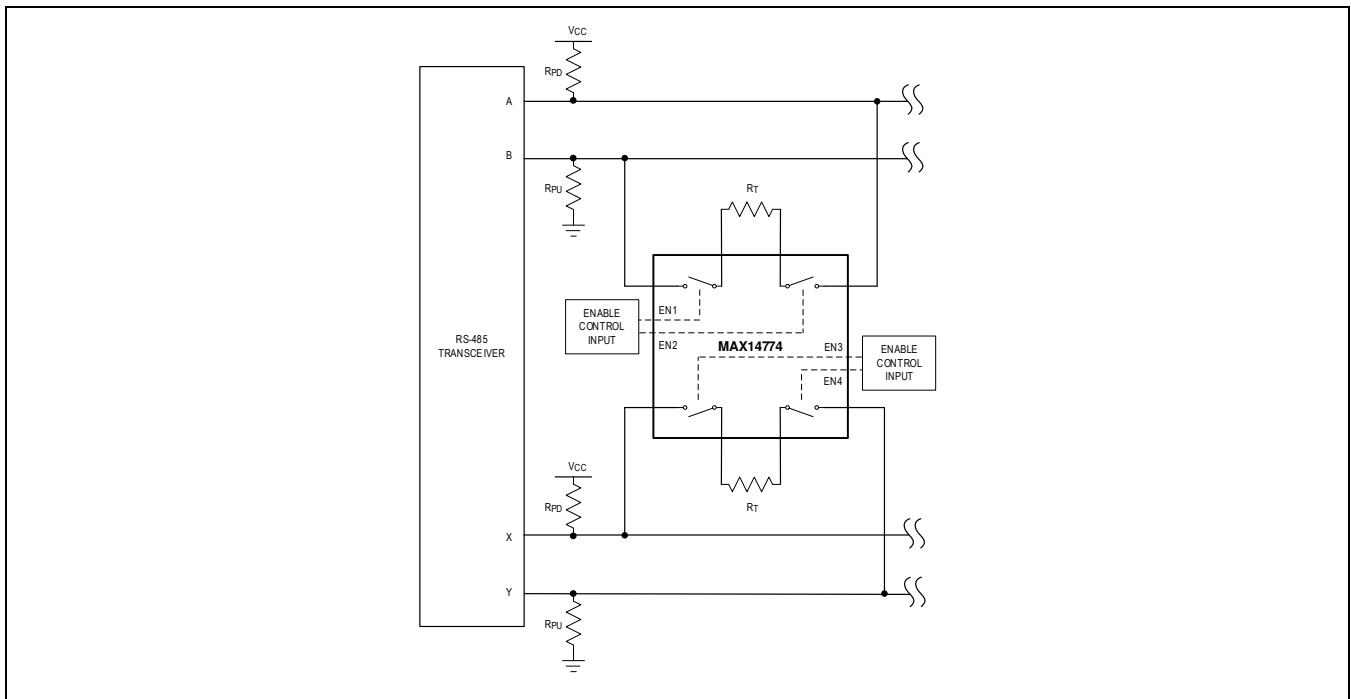
Switching Audio Amplifiers



RS-485 Fail-Safe Biasing Switch



RS-485 Termination Resistor Switch



Ordering Information

PART NUMBER	CONFIGURATION	TEMPERATURE RANGE	PIN-PACKAGE
MAX14774ATP+	Quad SPST	-40°C to +125°C	20 TQFN
MAX14779ATP+	Dual SPDT	-40°C to +125°C	20 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/22	Release for Market Intro	—

