



SY58605U

3.2Gbps Precision, LVDS Buffer with Internal Termination and Fail Safe Input

General Description

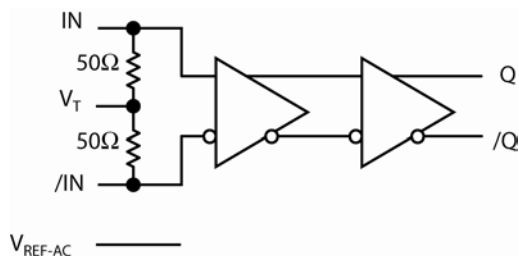
The SY58605U is a 2.5V, high-speed, fully differential LVDS buffer optimized to provide less than 10ps_{pp} total jitter. The SY58605U can process clock signals as fast as 2GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV (200mV_{pp}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference (V_{REF-AC}) is provided to bias the V_T pin. The output is 325mV LVDS, with rise/fall times guaranteed to be less than 100ps.

The SY58605U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require CML or LVPECL outputs, consider Micrel's SY58603U and SY58604U, buffers with 400mV and 800mV output swings respectively. The SY58605U is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge[®]

Features

- Precision 325mV LVDS buffer
- Guaranteed AC performance over temperature and voltage:
 - DC-to > 3.2Gbps throughput
 - <300ps typical propagation delay (IN-to-Q)
 - <100ps rise/fall times
- Fail Safe Input
 - Prevents output from oscillating when input is invalid
- Ultra-low jitter design
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{pp} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{pp} deterministic jitter
- High-speed LVDS output
- 2.5V ±5% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 8-pin (2mm x 2mm) DFN package

Applications

- All SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution
- Backplane distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

United States Patent No. RE44,134

Precision Edge is a registered trademark of Micrel, Inc.

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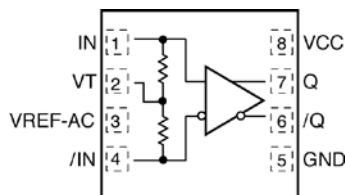
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|-------------------------------------|-------------------|
| SY58605UMG | DFN-8 | Industrial | 605 with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY58605UMGTR ⁽²⁾ | DFN-8 | Industrial | 605 with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

- Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
- Tape and Reel.

Pin Configuration



8-Pin DFN

Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|---------------------|--|
| 1, 4 | IN, /IN | Differential Input: This input pair is the differential signal input to the device. Input accepts DC-coupled differential signals as small as 100mV (200mV _{PP}). Each pin of this pair internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typically 30mV), then the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See "Input Interface Applications" subsection for more details. |
| 2 | VT | Input Termination Center-Tap: Each input terminates to this pin. The V _T pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection for more details. |
| 3 | VREF-AC | Reference Voltage: This output biases to V _{CC} -1.2V. It is used for AC-coupling input IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01μF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. See "Input Interface Applications" subsection for more details. |
| 5 | GND, Exposed pad | Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pin. |
| 6, 7 | /Q, Q | LVDS Differential Output Pair: The output swing is typically 325mV. Normally terminated with 100Ω across the pair (Q, /Q). See "LVDS Output Termination" subsection for more details. |
| 8 | VCC | Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the V _{CC} pin as possible. |

Absolute Maximum Ratings⁽¹⁾

| | | |
|---|-------|--------------------------|
| Supply Voltage (V_{CC}) | | -0.5V to +4.0V |
| Input Voltage (V_{IN}) | | -0.5V to $V_{CC} + 0.3V$ |
| LVDS Output Current (I_{OUT}) | | $\pm 10mA$ |
| Input Current | | |
| Source or Sink Current on (IN, /IN) | | $\pm 50mA$ |
| Current (V_{REF}) | | |
| Source or sink current on V_{REF-AC} ⁽⁴⁾ | | $\pm 1.5mA$ |
| Maximum operating Junction Temperature | | 125°C |
| Lead Temperature (soldering, 20sec.) | | 260°C |
| Storage Temperature (T_s) | | -65°C to +150°C |

Operating Ratings⁽²⁾

| | | |
|---|-------|--------------------|
| Supply Voltage (V_{IN}) | | +2.375V to +2.625V |
| Ambient Temperature (T_A) | | -40°C to +85°C |
| Package Thermal Resistance ⁽³⁾ | | |
| DFN | | |
| Still-air (θ_{JA}) | | 93°C/W |
| Junction-to-board (ψ_{JB}) | | 56°C/W |

DC Electrical Characteristics⁽⁵⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|------------------------|--------------|--------------|--------------|----------|
| V_{CC} | Power Supply Voltage Range | | 2.375 | 2.5 | 2.625 | V |
| I_{CC} | Power Supply Current | No load, max. V_{CC} | | 35 | 50 | mA |
| R_{DIFF_IN} | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (IN, /IN) | IN, /IN | 1.2 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, /IN) | IN, /IN | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, /IN) | see Figure 3a, Note 6 | 0.1 | | 1.7 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing (IN - /IN) | see Figure 3b | 0.2 | | | V |
| V_{IN_FSI} | Input Voltage Threshold that Triggers FSI | | | 30 | 100 | mV |
| V_{REF-AC} | Output Reference Voltage | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |
| V_{T_IN} | Voltage from Input to V_T | | | | 1.28 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max) is specified when V_T is floating.

LVDS Output DC Electrical Characteristics⁽⁷⁾

$V_{CC} = +2.5V \pm 5\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|-----------------------------------|---------------|-------|------|-------|-------|
| V_{OUT} | Output Voltage Swing | See Figure 3a | 250 | 325 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing | See Figure 3b | 500 | 650 | | mV |
| V_{OCM} | Output Common Mode Voltage | | 1.125 | 1.20 | 1.275 | V |
| ΔV_{OCM} | Change in Common Mode Voltage | | -50 | | 50 | mV |

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

$V_{CC} = +2.5V \pm 5\%$, $R_L = 100\Omega$ across the outputs, Input $t_r/t_f: \leq 300ps$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|-------------------------------------|-------------------------|-----|-----|-----|---------------|
| f_{MAX} | Maximum Frequency | NRZ Data | 3.2 | | | Gbps |
| | | $V_{OUT} > 200mV$ Clock | 2.0 | 3 | | GHz |
| t_{PD} | Propagation Delay IN-to-Q | $V_{IN}: 100mV-200mV$ | 170 | 280 | 420 | ps |
| | | 200mV-800mV | 130 | 200 | 300 | ps |
| t_{Skew} | Part-to-Part Skew | Note 8 | | | 135 | ps |
| t_{Jitter} | Data Random Jitter | Note 9 | | | 1 | μs_{RMS} |
| | Deterministic Jitter | Note 10 | | | 10 | μs_{PP} |
| | Clock Cycle-to-Cycle Jitter | Note 11 | | | 1 | μs_{RMS} |
| | Total Jitter | Note 12 | | | 10 | μs_{PP} |
| t_r, t_f | Output Rise/Fall Times (20% to 80%) | At full output swing. | 35 | 60 | 100 | ps |
| | Duty Cycle | Differential I/O | 47 | | 53 | % |

Notes:

- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
- Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
- Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
- Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100mV_{PK} (200mV_{PP}), typically 30mV_{PK} . Maximum frequency of SY58605U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will then eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Characteristics" for detailed information.

Timing Diagrams

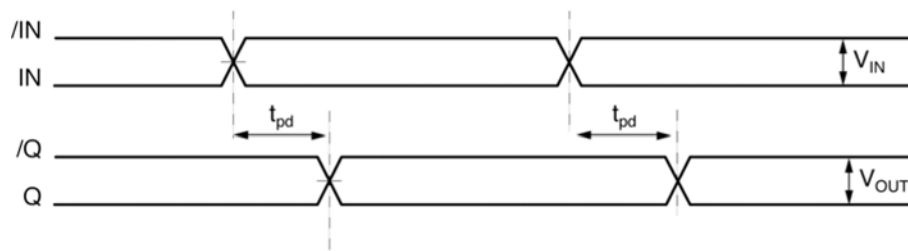


Figure 1a. Propagation Delay

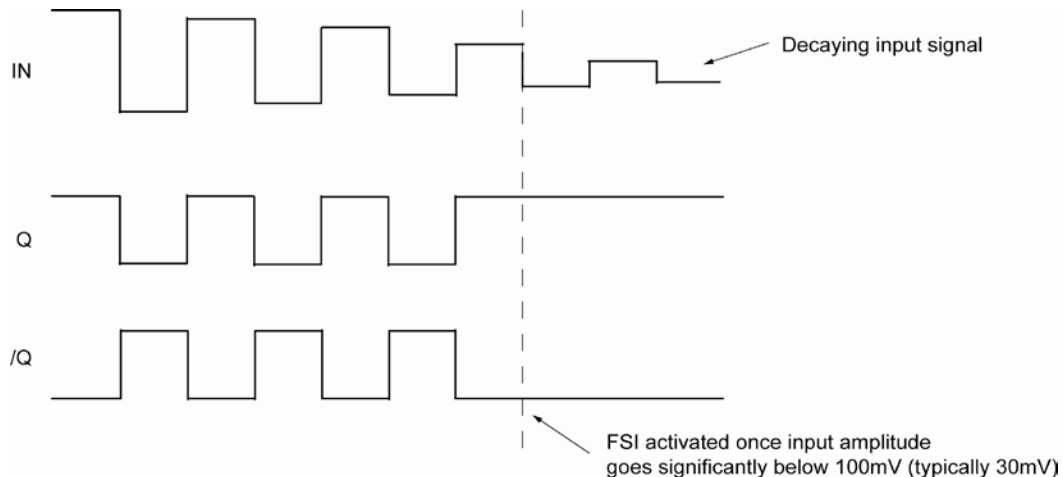
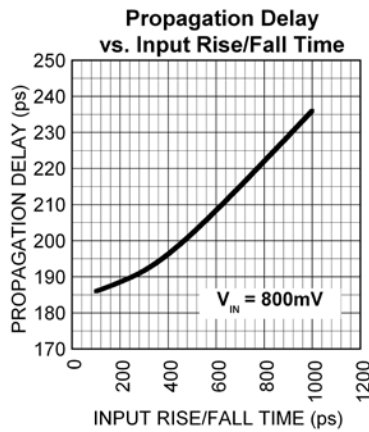
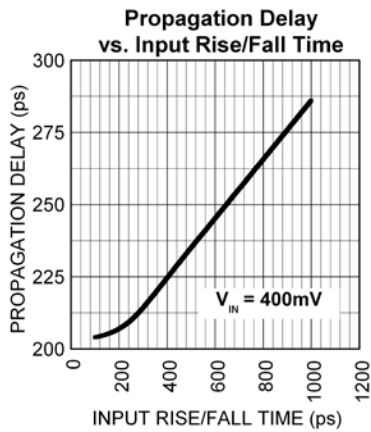
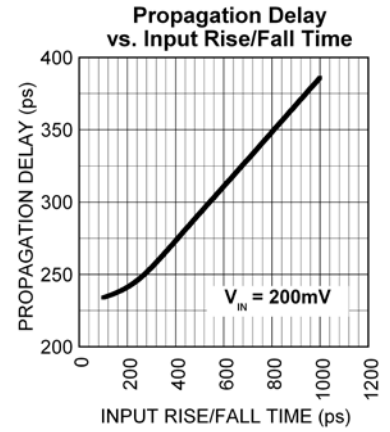
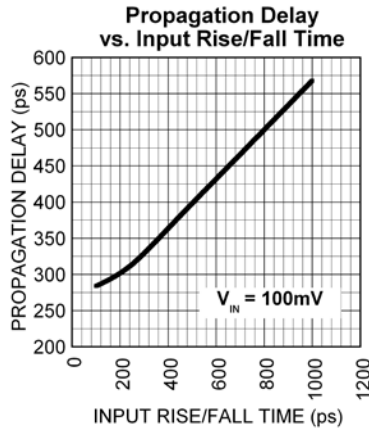
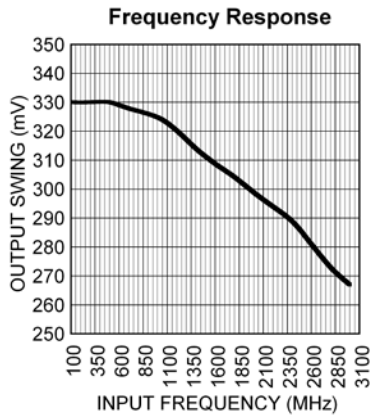


Figure 1b. Fail Safe Feature

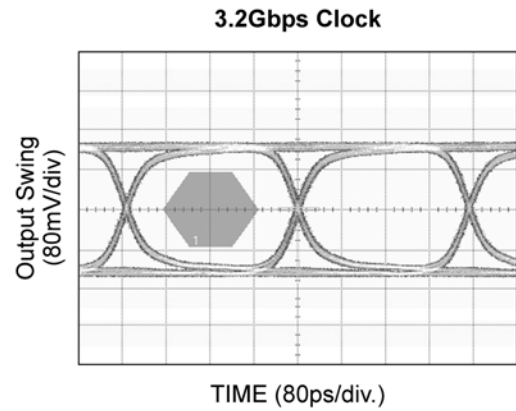
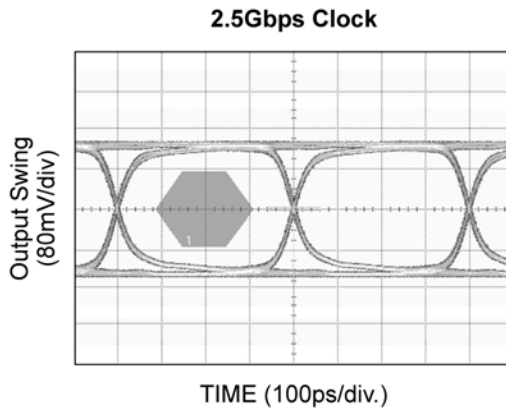
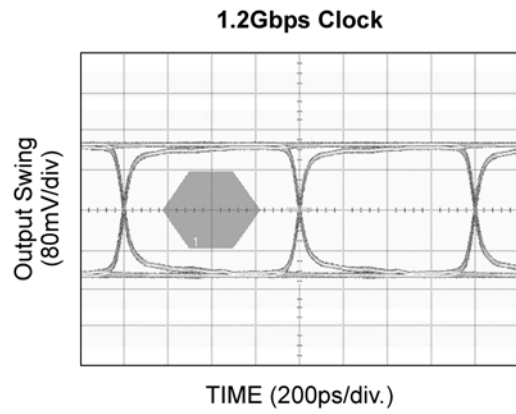
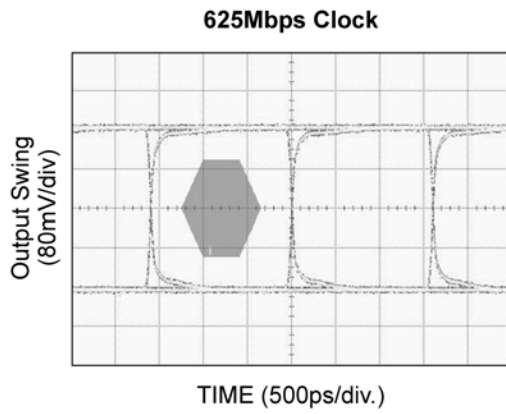
Typical Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



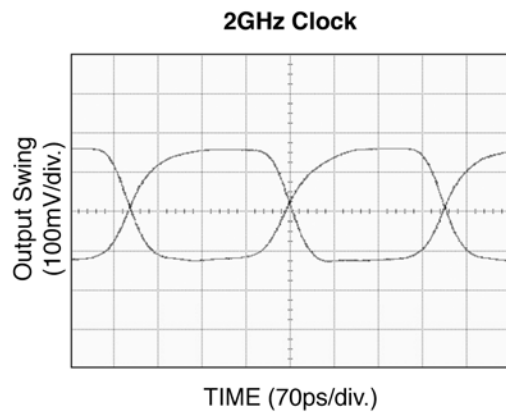
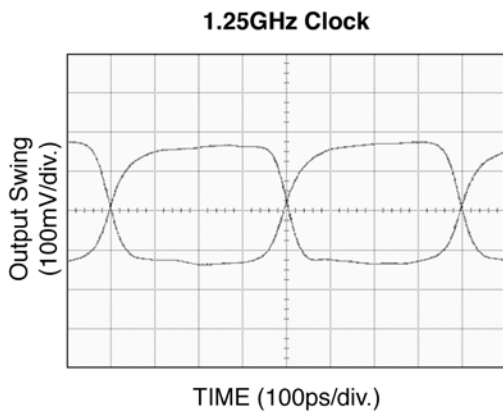
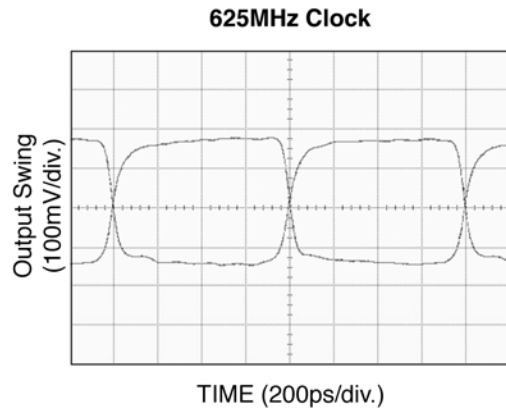
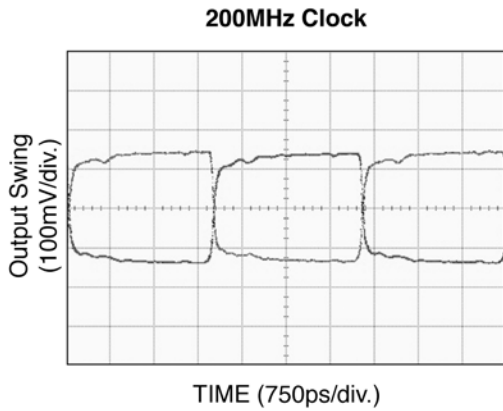
Functional Characteristics

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 250mV$, Data Pattern: $2^{23}-1$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics (continued)

$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Input Stage

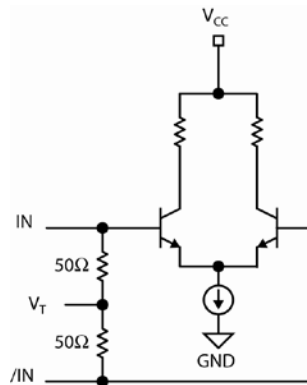


Figure 2. Simplified Differential Input Buffer

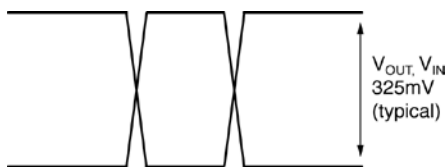


Figure 3a. Single-Ended Swing

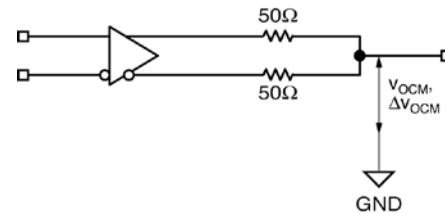


Figure 3c. LVDS Common Mode Measurement

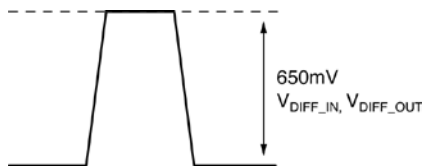


Figure 3b. Differential Swing

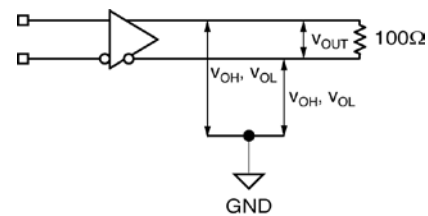


Figure 3d. LVDS Differential Measurement

Input Interface Applications

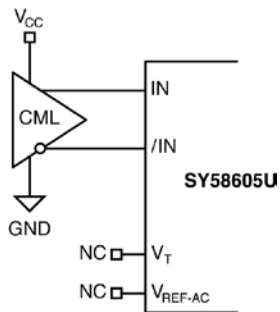


Figure 4a. CML Interface (DC-Coupled)

Option: May connect VT to VCC

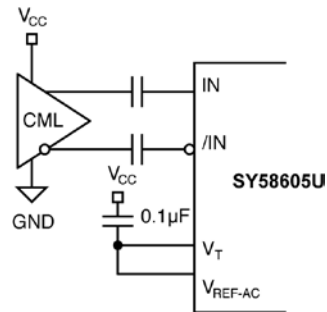


Figure 4b. CML Interface (AC-Coupled)

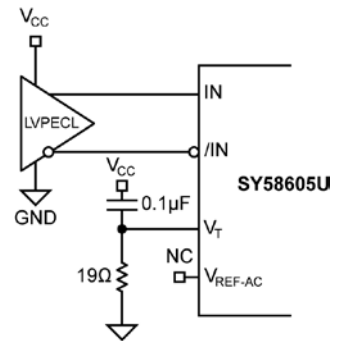


Figure 4c. LVPECL Interface (DC-Coupled)

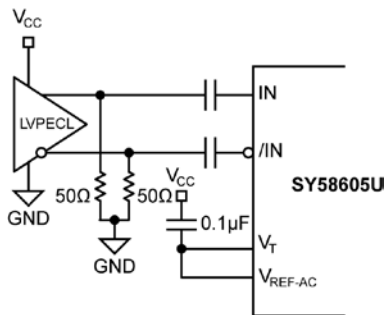


Figure 4d. LVPECL Interface (AC-Coupled)

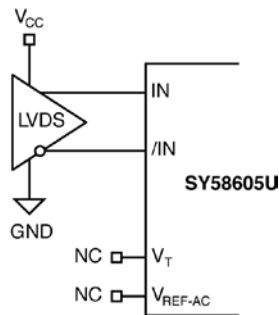
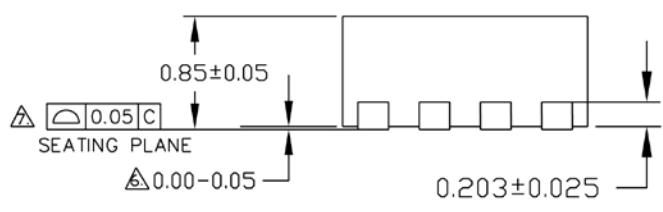
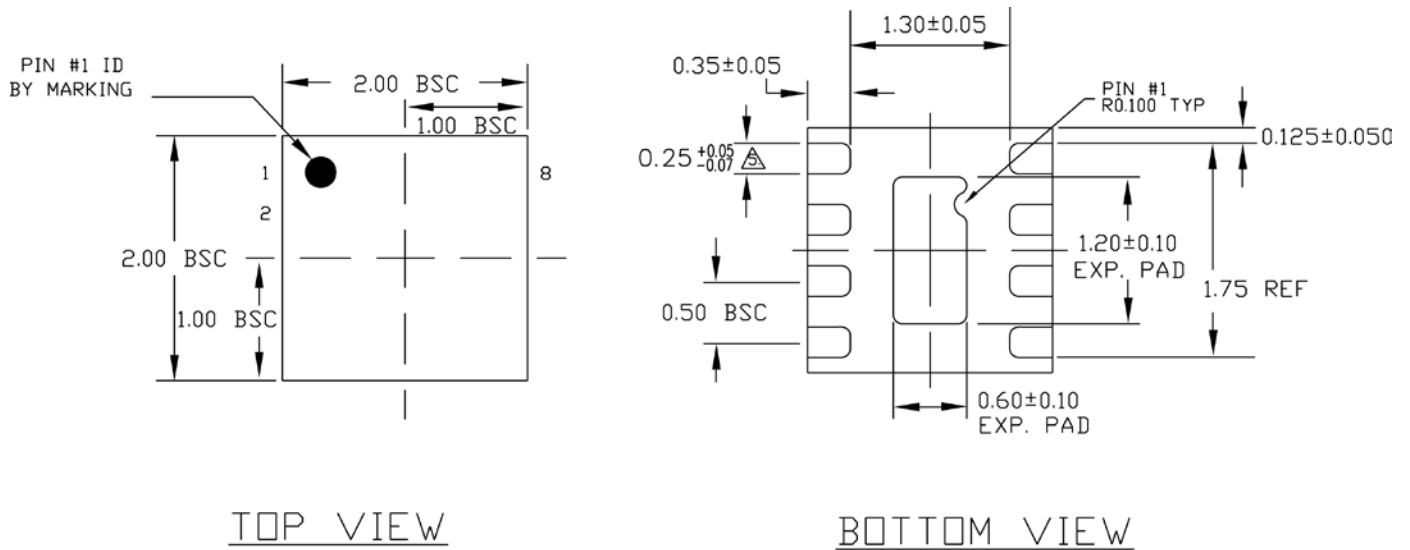


Figure 4e. LVDS Interface

Related Product and Support Documents

| Part Number | Function | Data Sheet Link |
|---------------|---|---|
| SY58603U | 4.25Gbps Precision CML Buffer with Internal Termination and Fail Safe Input | http://www.micrel.com/page.do?page=/product-info/products/sy58603u.shtml |
| SY58604U | 3.2Gbps Precision LVPECL Buffer with Internal Termination and Fail Safe Input | http://www.micrel.com/page.do?page=/product-info/products/sy58604u.shtml |
| HBW Solutions | New Products and Termination Application Notes | http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml |

Package Information



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

SIDE VIEW

8-Pin (2mm x 2mm) DFN

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