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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2709AGR

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2709AGR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

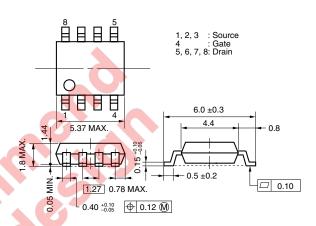
FEATURES

- Low on-state resistance
 - $R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, I}_D = 7.0 \text{ A)}$

 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX.} (V_{GS} = 4.5 \text{ V}, I_{D} = 7.0 \text{ A})$

- · Low gate to drain charge
 - $Q_{GD} = 3.3 \text{ nC TYP.} (V_{DD} = 15 \text{ V}, I_{D} = 13 \text{ A})$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

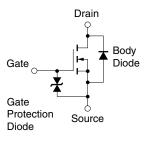
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	ID(DC)	±13	Α
Drain Current (pulse) Note1	ID(pulse)	±52	Α
Total Power Dissipation Note2	P _{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	P _{T2}	2.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	13	Α
Single Avalanche Energy Note3	Eas	17	mJ

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
 - 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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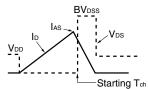


ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

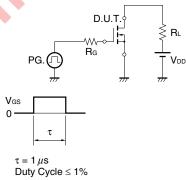
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 7.0 A	7			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 7.0 A		8.3	10.5	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 7.0 A		10.6	15	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1270		pF
Output Capacitance	Coss	V _{GS} = 0 V		320		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		110		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 7.0 A		10		ns
Rise Time	tr	V _{GS} = 10 V		5.3		ns
Turn-off Delay Time	t d(off)	R _G = 10 Ω		40		ns
Fall Time	tf			7.8		ns
Total Gate Charge	QG	V _{DD} = 15 V		11		nC
Gate to Source Charge	Qgs	V _{GS} = 5 V		3.8		nC
Gate to Drain Charge	Q _{GD}	ID = 13 A		3.3		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.8		٧
Reverse Recovery Time	trr	I _F = 13 A, V _{GS} = 0 V		25		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		22		nC
Gate Resistance	Rg	f = 1 MHz		1.2		Ω

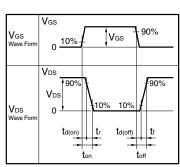
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

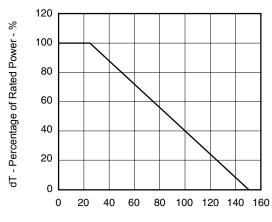




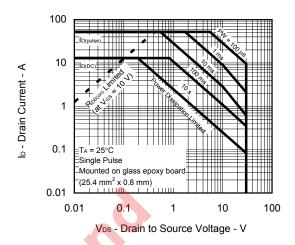
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

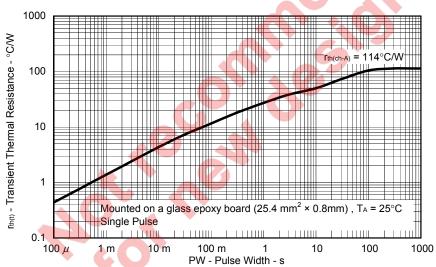


FORWARD BIAS SAFE OPERATING AREA

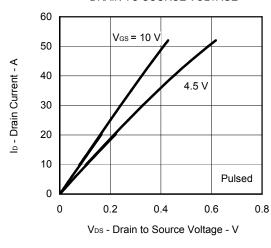


T_A - Ambient Temperature - °C

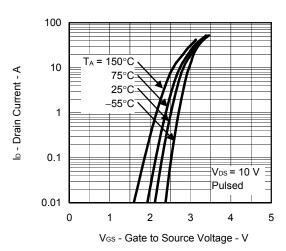
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



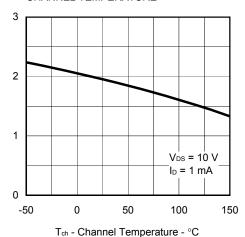
FORWARD TRANSFER CHARACTERISTICS



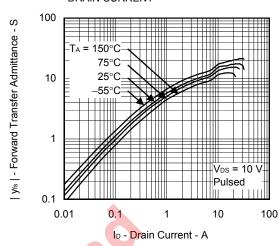
Ves(off) - Gate to Source Cut-off Voltage - V

R_{DS(o1)} - Drain to Source On-state Resistance - mΩ

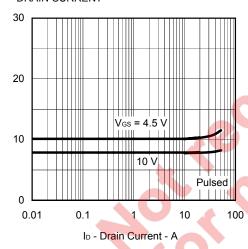
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



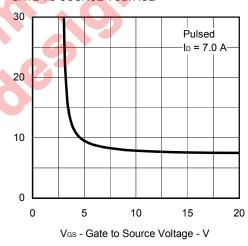
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



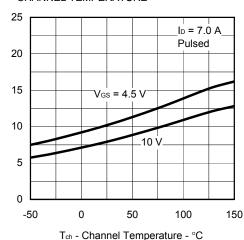
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



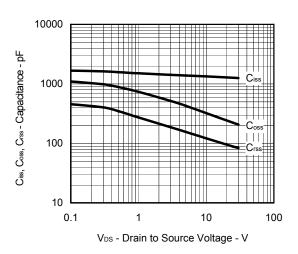
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

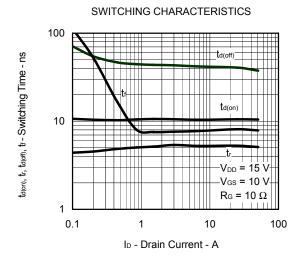


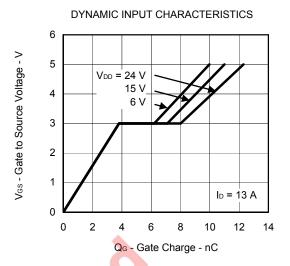
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



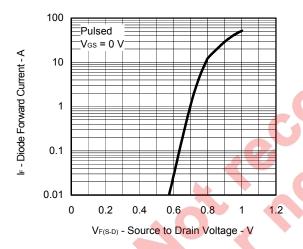
 $\mathsf{R}_{\mathsf{DS}(\varpi)}$ - Drain to Source On-state Resistance - $m\Omega$

RDS(on) - Drain to Source On-state Resistance - mΩ

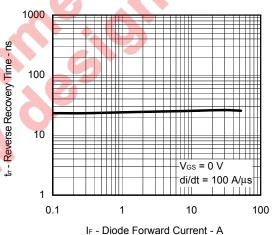












ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
μPA2709AGR-E1-AT Note	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8	
μ PA2709AGR-E2-AT Note			0.08 g TYP.	

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

 μ PA2709AGR

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