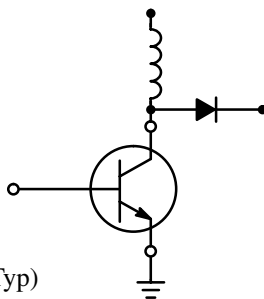


# SWITCHMODE™ II Series NPN Silicon Power Transistors

The BUV48/BUV48A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated SWITCHMODE applications such as:

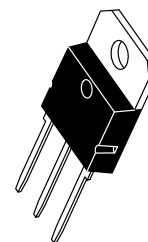
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
  - 60 ns Inductive Fall Time — 25°C (Typ)
  - 120 ns Inductive Crossover Time — 25°C (Typ)
- Operating Temperature Range –65 to +175°C
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltage
  - Leakage Currents (125°C)



## BUV48 BUV48A

**15 AMPERES  
NPN SILICON  
POWER TRANSISTORS  
400 AND 450 VOLTS**

**$V_{(BR)CEO}$   
850–1000 VOLTS  
 $V_{(BR)CEX}$   
150 WATTS**



**CASE 340D-02  
TO-218 TYPE**

## MAXIMUM RATINGS

| Rating                                             | Symbol         | BUV48       | BUV48A | Unit  |
|----------------------------------------------------|----------------|-------------|--------|-------|
| Collector–Emitter Voltage                          | $V_{CEO(sus)}$ | 400         | 450    | Vdc   |
| Collector–Emitter Voltage ( $V_{BE} = -1.5$ V)     | $V_{CEX}$      | 850         | 1000   | Vdc   |
| Emitter Base Voltage                               | $V_{EB}$       | 7           |        | Vdc   |
| Collector Current — Continuous                     | $I_C$          | 15          |        | Adc   |
| — Peak (1)                                         | $I_{CM}$       | 30          |        |       |
| — Overload                                         | $I_{OI}$       | 60          |        |       |
| Base Current — Continuous                          | $I_B$          | 5           |        | Adc   |
| — Peak (1)                                         | $I_{BM}$       | 20          |        |       |
| Total Power Dissipation — $T_C = 25^\circ\text{C}$ | $P_D$          | 150         |        | Watts |
| — $T_C = 100^\circ\text{C}$                        |                | 75          |        |       |
| Derate above 25°C                                  |                | 1           |        | W/°C  |
| Operating and Storage Junction Temperature Range   | $T_J, T_{stg}$ | –65 to +175 |        | °C    |

## THERMAL CHARACTERISTICS

| Characteristic                                                                   | Symbol          | Max | Unit |
|----------------------------------------------------------------------------------|-----------------|-----|------|
| Thermal Resistance, Junction to Case                                             | $R_{\theta JC}$ | 1   | °C/W |
| Maximum Lead Temperature for Soldering Purposes:<br>1/8" from Case for 5 Seconds | $T_L$           | 275 | °C   |

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

# BUV48 BUV48A

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

### OFF CHARACTERISTICS (1)

|                                                                                                                                                                                                    |                                                       |                |            |        |          |      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|----------------|------------|--------|----------|------|
| Collector–Emitter Sustaining Voltage (Table 1)<br>( $I_C = 200\text{ mA}$ , $I_B = 0$ ) $L = 25\text{ mH}$                                                                                         | BUV48<br>BUV48A                                       | $V_{CEO(sus)}$ | 400<br>450 | —<br>— | —<br>—   | Vdc  |
| Collector Cutoff Current<br>( $V_{CEX} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )<br>( $V_{CEX} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) |                                                       | $I_{CEX}$      | —<br>—     | —<br>— | 0.2<br>2 | mAdc |
| Collector Cutoff Current<br>( $V_{CE} = \text{Rated } V_{CEX}$ , $R_{BE} = 10\ \Omega$ )                                                                                                           | $T_C = 25^\circ\text{C}$<br>$T_C = 125^\circ\text{C}$ | $I_{CER}$      | —<br>—     | —<br>— | 0.5<br>3 | mAdc |
| Emitter Cutoff Current<br>( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )                                                                                                                                  |                                                       | $I_{EBO}$      | —          | —      | 0.1      | mAdc |
| Emitter–Base Breakdown Voltage<br>( $I_E = 50\text{ mA}$ – $I_C = 0$ )                                                                                                                             |                                                       | $V_{(BR)EBO}$  | 7          | —      | —        | Vdc  |

### SECOND BREAKDOWN

|                                                             |           |               |  |
|-------------------------------------------------------------|-----------|---------------|--|
| Second Breakdown Collector Current with Base Forward Biased | $I_{S/b}$ | See Figure 12 |  |
| Clamped Inductive SOA with Base Reverse Biased              | RBSOA     | See Figure 13 |  |

### ON CHARACTERISTICS (1)

|                                                                                                                                                                                                                                                                                                                                                                                                                          |                             |               |                            |                            |                                |     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------------|----------------------------|----------------------------|--------------------------------|-----|
| DC Current Gain<br>( $I_C = 10\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )<br>( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )                                                                                                                                                                                                                                                                                             | BUV48<br>BUV48A             | $h_{FE}$      | 8<br>8                     | —<br>—                     | —<br>—                         |     |
| Collector–Emitter Saturation Voltage<br>( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ )<br>( $I_C = 15\text{ Adc}$ , $I_B = 3\text{ Adc}$ )<br>( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )<br>( $I_C = 8\text{ Adc}$ , $I_B = 1.6\text{ Adc}$ )<br>( $I_C = 12\text{ Adc}$ , $I_B = 2.4\text{ Adc}$ )<br>( $I_C = 8\text{ Adc}$ , $I_B = 1.6\text{ Adc}$ , $T_C = 100^\circ\text{C}$ ) | BUV48<br><br><br><br>BUV48A | $V_{CE(sat)}$ | —<br>—<br>—<br>—<br>—<br>— | —<br>—<br>—<br>—<br>—<br>— | 1.5<br>5<br>2<br>1.5<br>5<br>2 | Vdc |
| Base–Emitter Saturation Voltage<br>( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ )<br>( $I_C = 10\text{ Adc}$ , $I_B = 2\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )<br>( $I_C = 8\text{ Adc}$ , $I_B = 1.6\text{ Adc}$ )<br>( $I_C = 8\text{ Adc}$ , $I_B = 1.6\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )                                                                                                                | BUV48<br><br>BUV48A         | $V_{BE(sat)}$ | —<br>—<br>—<br>—           | —<br>—<br>—<br>—           | 1.6<br>1.6<br>1.6<br>1.6       | Vdc |

### DYNAMIC CHARACTERISTICS

|                                                                                            |          |   |   |     |    |
|--------------------------------------------------------------------------------------------|----------|---|---|-----|----|
| Output Capacitance<br>( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ ) | $C_{ob}$ | — | — | 350 | pF |
|--------------------------------------------------------------------------------------------|----------|---|---|-----|----|

### SWITCHING CHARACTERISTICS

#### Resistive Load (Table 1)

|              |                                                                                                                                                                                                  |                 |       |   |     |     |               |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|---|-----|-----|---------------|
| Delay Time   | $I_C = 10\text{ A}$ , $I_B = 2\text{ A}$<br>$I_C = 8\text{ A}$ , $I_B = 1.6\text{ A}$<br>Duty Cycle $\leq 2\%$ , $V_{BE(off)} = 5\text{ V}$<br>$T_p = 30\ \mu\text{s}$ , $V_{CC} = 300\text{ V}$ | BUV48<br>BUV48A | $t_d$ | — | 0.1 | 0.2 | $\mu\text{s}$ |
| Rise Time    |                                                                                                                                                                                                  |                 | $t_r$ | — | 0.4 | 0.7 |               |
| Storage Time |                                                                                                                                                                                                  |                 | $t_s$ | — | 1.3 | 2   |               |
| Fall Time    |                                                                                                                                                                                                  |                 | $t_f$ | — | 0.2 | 0.4 |               |

#### Inductive Load, Clamped (Table 1)

|                |                                               |        |                             |          |   |      |      |               |
|----------------|-----------------------------------------------|--------|-----------------------------|----------|---|------|------|---------------|
| Storage Time   | $I_C = 10\text{ A}$<br>$I_{B1} = 2\text{ A}$  | BUV48  | $(T_C = 25^\circ\text{C})$  | $t_{sv}$ | — | 1.3  | —    | $\mu\text{s}$ |
| Fall Time      |                                               |        |                             | $t_{fi}$ | — | 0.06 | —    |               |
| Storage Time   | $I_C = 8\text{ A}$<br>$I_{B1} = 1.6\text{ A}$ | BUV48A | $(T_C = 100^\circ\text{C})$ | $t_{sv}$ | — | 1.5  | 2.5  |               |
| Crossover Time |                                               |        |                             | $t_c$    | — | 0.3  | 0.6  |               |
| Fall Time      |                                               |        |                             | $t_{fi}$ | — | 0.17 | 0.35 |               |

(1) Pulse Test: Pulse Width =  $300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .  
 $V_{cl} = 300\text{ V}$ ,  $V_{BE(off)} = 5\text{ V}$ ,  $L_c = 180\ \mu\text{H}$

# BUV48 BUV48A

## DC CHARACTERISTICS

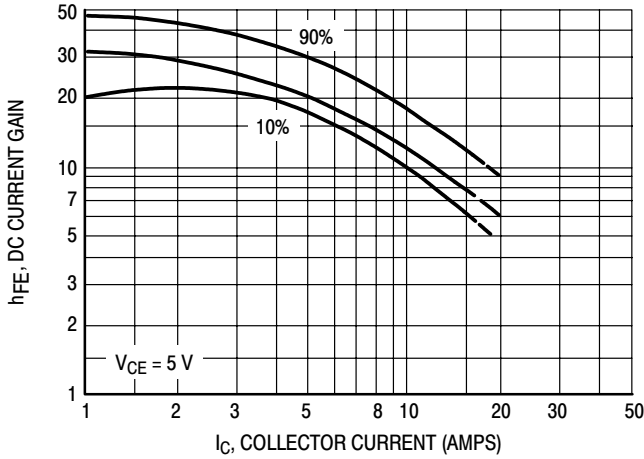


Figure 1. DC Current Gain

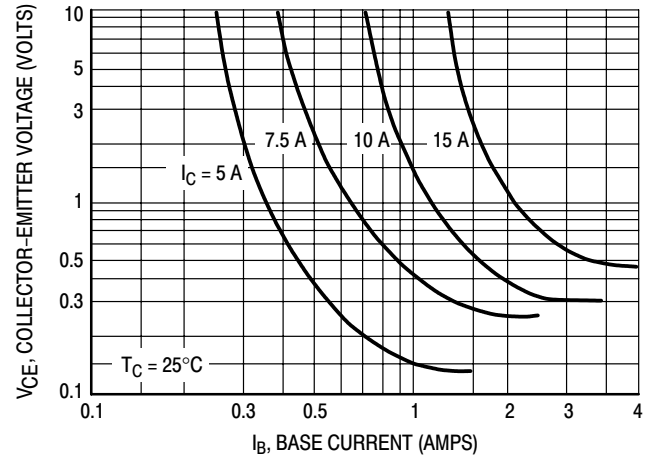


Figure 2. Collector Saturation Region

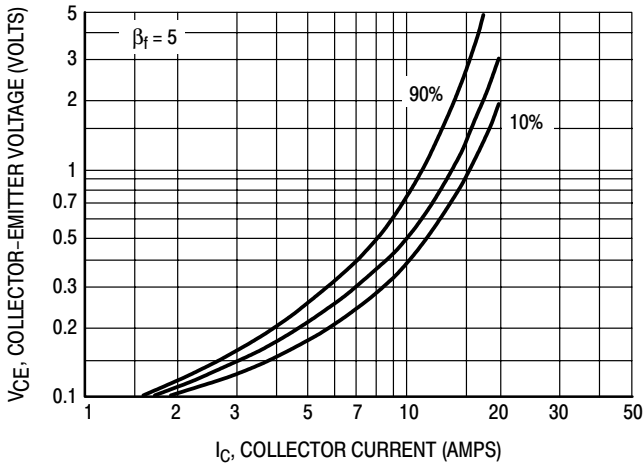


Figure 3. Collector-Emitter Saturation Voltage

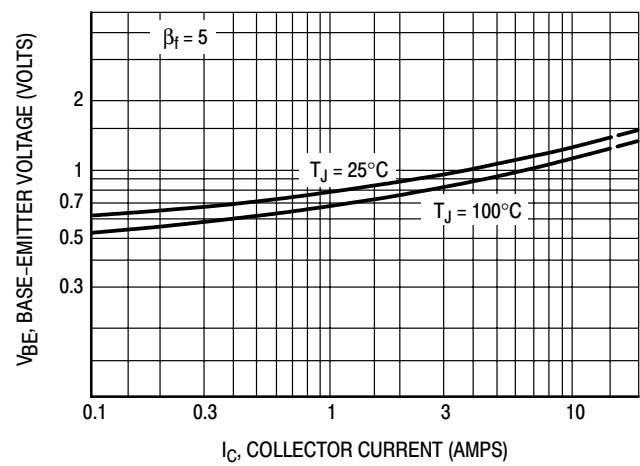


Figure 4. Base-Emitter Voltage

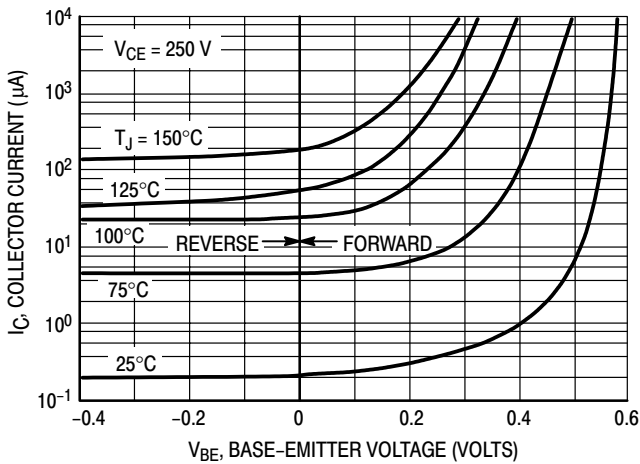


Figure 5. Collector Cutoff Region

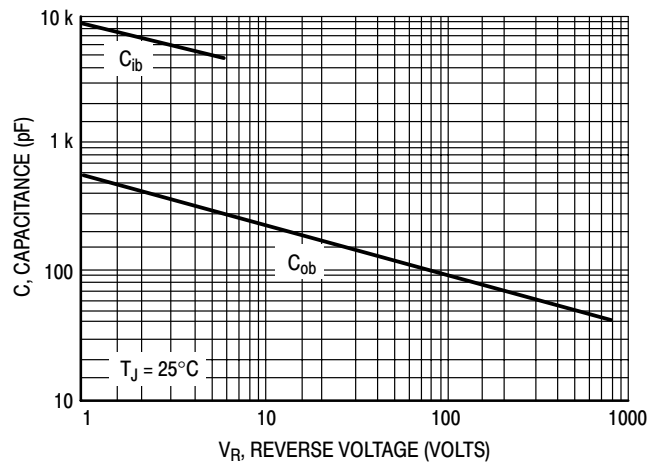
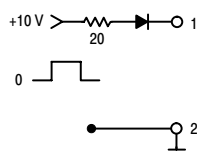
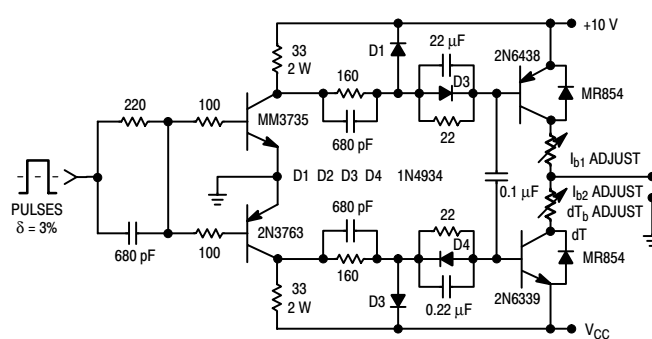
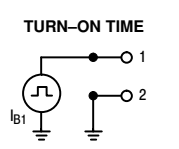
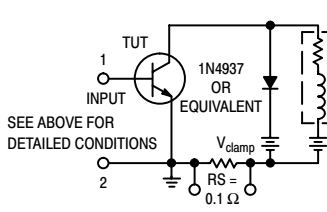
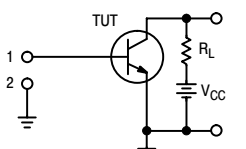


Figure 6. Capacitance

BUV48 BUV48A

Table 1. Test Conditions for Dynamic Performance

|                  | $V_{CE(sus)}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | RBSOA AND INDUCTIVE SWITCHING                                                                                                                                   | RESISTIVE SWITCHING                                                                                                                                                                                                                                                                                               |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INPUT CONDITIONS |  <p>PW Varied to Attain<br/><math>I_C = 200 \text{ mA}</math></p>                                                                                                                                                                                                                                                                                                                                                        |                                                                               |  <p><b>TURN-ON TIME</b></p> <p><math>I_{B1}</math> adjusted to obtain the forced <math>h_{FE}</math> desired</p> <p><b>TURN-OFF TIME</b></p> <p>Use inductive switching driver as the input to the resistive test circuit.</p> |
| CIRCUIT VALUES   | $L_{coil} = 25 \text{ mH}$ , $V_{CC} = 10 \text{ V}$<br>$R_{coil} = 0.7 \Omega$                                                                                                                                                                                                                                                                                                                                                                                                                           | $L_{coil} = 180 \mu\text{H}$<br>$R_{coil} = 0.05 \Omega$<br>$V_{CC} = 20 \text{ V}$<br>$V_{clamp} = 300 \text{ V}$<br>$R_B$ ADJUSTED TO ATTAIN DESIRED $I_{B1}$ | $V_{CC} = 300 \text{ V}$<br>$R_L = 83 \Omega$<br>Pulse Width = $10 \mu\text{s}$                                                                                                                                                                                                                                   |
| TEST CIRCUITS    |  <p><b>INDUCTIVE TEST CIRCUIT</b></p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p> <p><math>R_S = 0.1 \Omega</math></p> <p><b>OUTPUT WAVEFORMS</b></p> <p><math>t_1</math> Adjusted to Obtain <math>I_C</math></p> <p><math>t_1 \approx \frac{L_{coil} (I_{C(pk)})}{V_{CC}}</math></p> <p><math>t_2 \approx \frac{L_{coil} (I_{C(pk)})}{V_{Clamp}}</math></p> <p>Test Equipment<br/>Scope — Tektronix 475 or Equivalent</p> |  <p><b>RESISTIVE TEST CIRCUIT</b></p>                                        |                                                                                                                                                                                                                                                                                                                   |

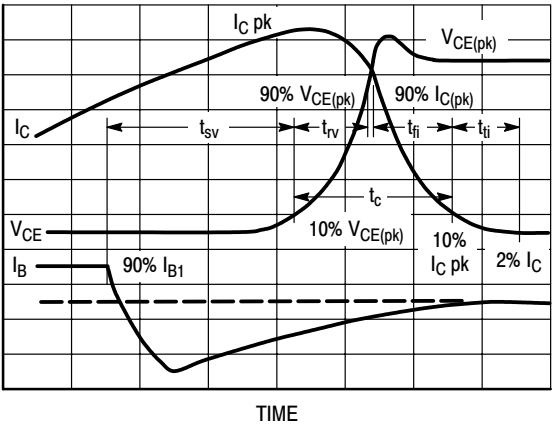


Figure 7. Inductive Switching Measurements

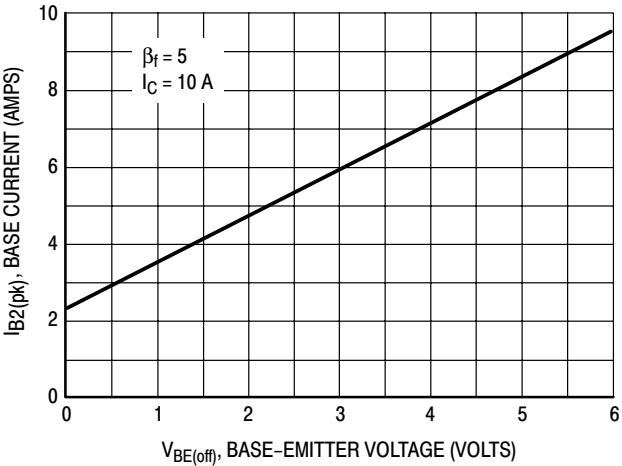


Figure 8. Peak-Reverse Current

# SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- $t_{sv}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{clamp}$
- $t_{rv}$  = Voltage Rise Time, 10–90%  $V_{clamp}$
- $t_{fi}$  = Current Fall Time, 90–10%  $I_C$
- $t_{ti}$  = Current Tail, 10–2%  $I_C$
- $t_c$  = Crossover Time, 10%  $V_{clamp}$  to 10%  $I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general,  $t_{rv} + t_{fi} \approx t_c$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds ( $t_c$  and  $t_{sv}$ ) which are guaranteed at 100°C.

## INDUCTIVE SWITCHING

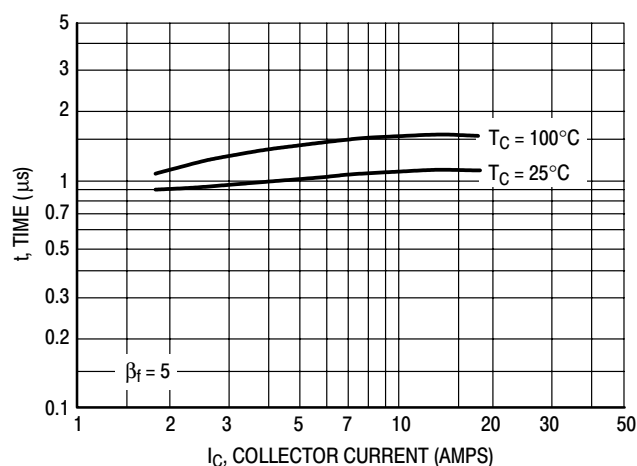


Figure 9. Storage Time,  $t_{sv}$

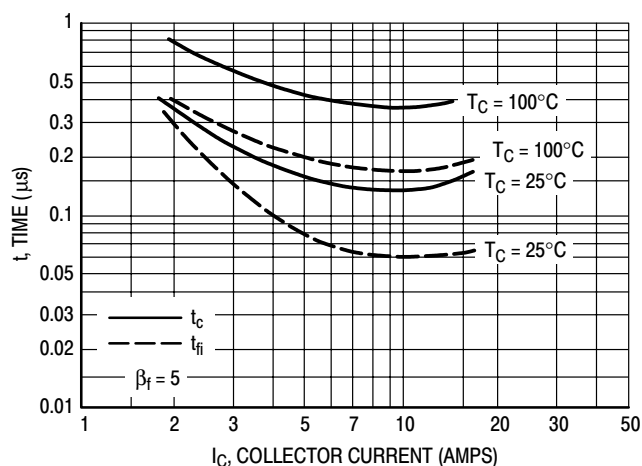


Figure 10. Crossover and Fall Times

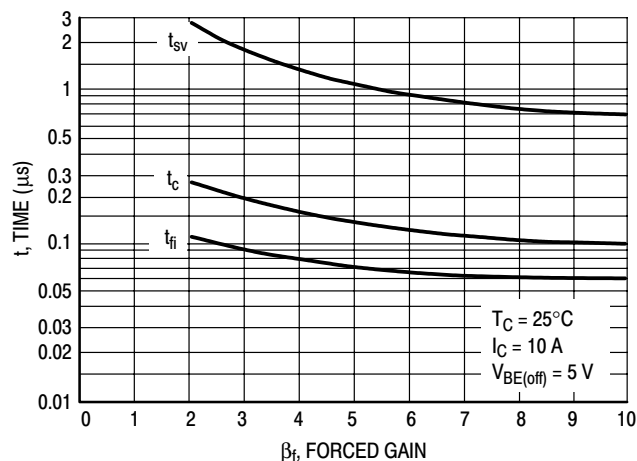


Figure 11. Turn-Off Times versus Forced Gain

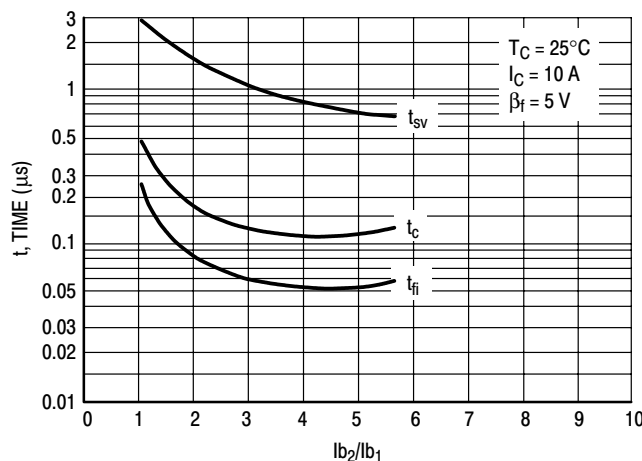


Figure 12. Turn-Off Times versus  $I_{b2}/I_{b1}$

# BUV48 BUV48A

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

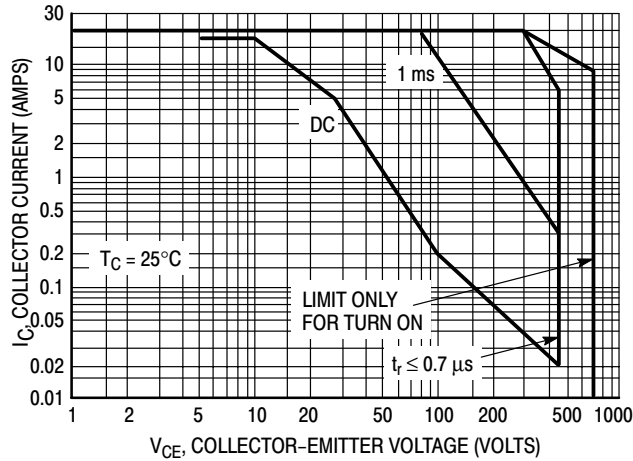


Figure 13. Forward Bias Safe Operating Area

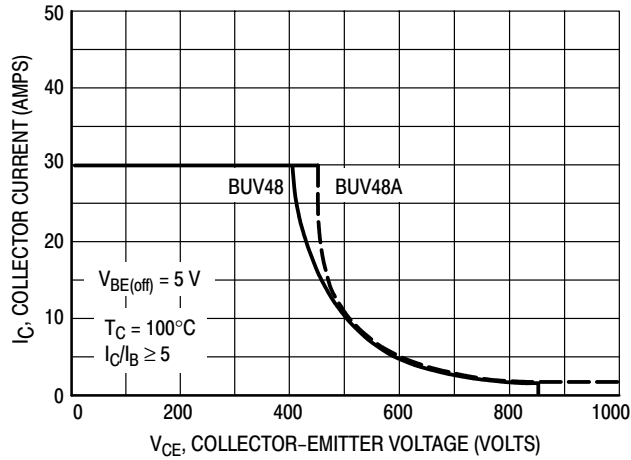


Figure 14. Reverse Bias Safe Operating Area

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \leq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.

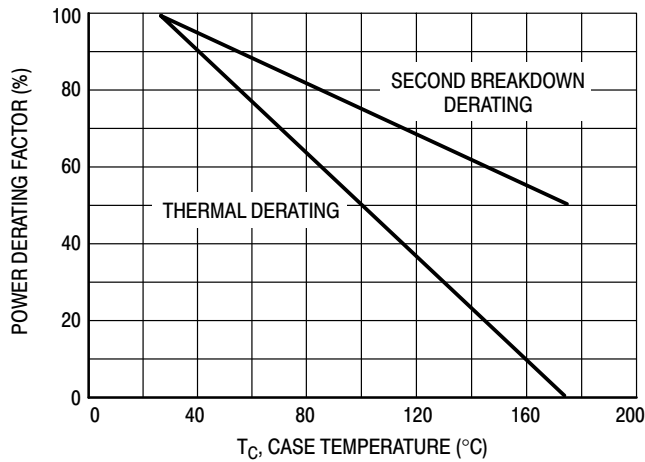


Figure 15. Power Derating

## BUV48 BUV48A

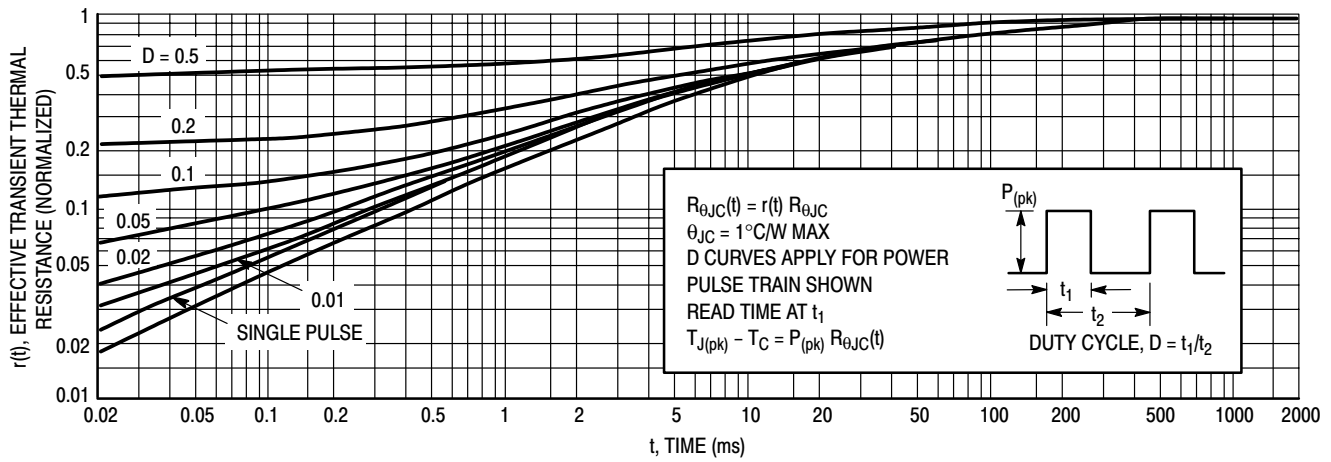


Figure 16. Thermal Response

## OVERLOAD CHARACTERISTICS

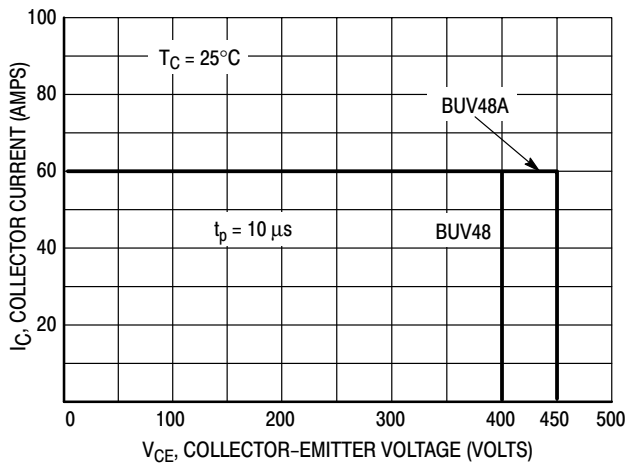


Figure 17. Rated Overload Safe Operating Area (OLSOA)

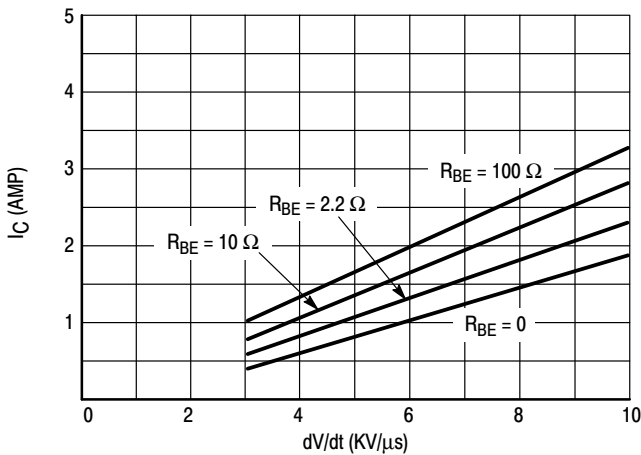


Figure 18.  $I_C = f(dV/dt)$

## OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 17 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 19) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

### Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired  $I_C$ ,  $t_p$

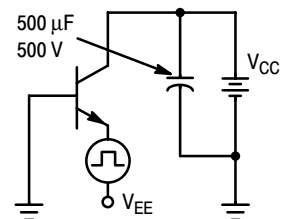
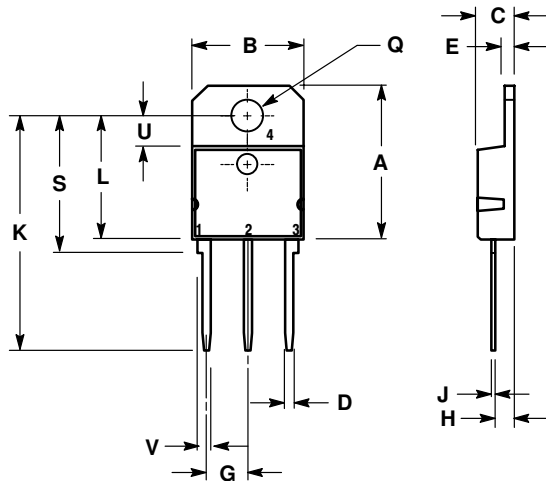


Figure 19. Overload SOA Test Circuit

# BUV48 BUV48A

## PACKAGE DIMENSIONS

### SOT-93 (TO-218) CASE 340D-02 ISSUE B



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| A   | ---         | 20.35 | ---    | 0.801 |
| B   | 14.70       | 15.20 | 0.579  | 0.598 |
| C   | 4.70        | 4.90  | 0.185  | 0.193 |
| D   | 1.10        | 1.30  | 0.043  | 0.051 |
| E   | 1.17        | 1.37  | 0.046  | 0.054 |
| G   | 5.40        | 5.55  | 0.213  | 0.219 |
| H   | 2.00        | 3.00  | 0.079  | 0.118 |
| J   | 0.50        | 0.78  | 0.020  | 0.031 |
| K   | 31.00       | REF   | 1.220  | REF   |
| L   | ---         | 16.20 | ---    | 0.638 |
| Q   | 4.00        | 4.10  | 0.158  | 0.161 |
| S   | 17.80       | 18.20 | 0.701  | 0.717 |
| U   | 4.00        | REF   | 0.157  | REF   |
| V   | 1.75        | REF   | 0.069  | REF   |

SWITCHMODE is a registered trademark of Semiconductor Components Industries, LLC (SCILLC)

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
Email: ONlit-german@hibbertco.com  
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
Email: ONlit-french@hibbertco.com  
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781

\*Available from Germany, France, Italy, UK, Ireland

### CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
Email: ONlit-spanish@hibbertco.com  
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –  
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 1-303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
001-800-4422-3781  
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
Phone: 81-3-5740-2700  
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.