TEXAS INSTRUMENTS
TPS51216-EP
SLUSCA7A – NOVEMBER 2015 – REVISED JULY 2022

TPS51216-EP Complete DDR2, DDR3 and DDR3L Memory Power Solution Synchronous Buck Controller, 2-A LDO, Buffered Reference

1 Features

- Synchronous buck controller (VDDQ)
  - Conversion voltage range: 3 to 28 V
  - Output voltage range: 0.7 to 1.8 V
  - 0.8% V_{REF} accuracy
  - D-CAP™ mode for fast transient response
  - Selectable 300-kHz/400-kHz switching frequencies
  - Optimized efficiency at light and heavy loads with auto-skip function
  - Supports soft-off in S4/S5 states
  - OCL/OVP/UVP/UVLO protections
  - Powergood output
- 2-A LDO (VTT), buffered reference (VTTREF)
  - 2-A (peak) sink and source current
  - Requires only 10-µF of ceramic output capacitance
  - Buffered, low noise, 10-mA VTTREF output
  - 0.8% VTTREF, 20-mV VTT accuracy
  - Support high-z in S3 and soft-off in S4/S5
- Thermal shutdown
- 20-Pin, 3 mm × 3 mm, WQFN Package
- **Supports Defense, Aerospace, and Medical Applications**
  - Controlled baseline
  - One assembly/test site
  - One fabrication site
  - Available in military (–55°C to 125°C) temperature range [1]
  - Extended product life cycle
  - Extended product-change notification
  - Product traceability

2 Applications

- DDR2/DDR3/DDR3L memory power supplies
- SSTL_18, SSTL_15, SSTL_135, and HSTL termination

3 Description

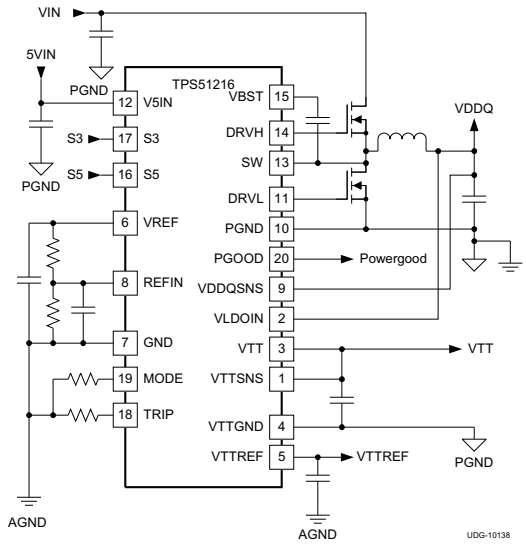
The TPS51216-EP provides a complete power supply for DDR2, DDR3 and DDR3L memory systems in the lowest total cost and minimum space. It integrates a synchronous buck regulator controller (VDDQ) with a 2-A sink/source tracking LDO (VTT) and buffered low noise reference (VTTREF). The TPS51216-EP employs D-CAP™ mode coupled with 300 kHz/400 kHz frequencies for ease-of-use and fast transient response. The VTTREF tracks VDDQ/2 within excellent 0.8% accuracy. The VTT, which provides 2-A sink/source peak current capabilities, requires only 10-µF of ceramic capacitance. In addition, a dedicated LDO supply input is available.

The TPS51216-EP provides rich useful functions as well as excellent power supply performance. It supports flexible power state control, placing VTT at high-Z in S3 and discharging VDDQ, VTT, and VTTREF (soft-off) in S4/S5 state.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS51216-EP	WQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram

[1] Additional temperature ranges available - contact factory

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4 Revision History

Changes from Revision * (November 2015) to Revision A (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated resistor numbers in Equation 7 to match description	23

5 Description (continued)

Programmable OCL with low-side MOSFET $R_{DS(on)}$ sensing, OVP/UVP/UVLO and thermal shutdown protections are also available.

The TPS51216-EP is available in a 20-pin, 3 mm × 3 mm, WQFN package and is specified for junction temperature from –55°C to 125°C.

6 Pin Configuration and Functions

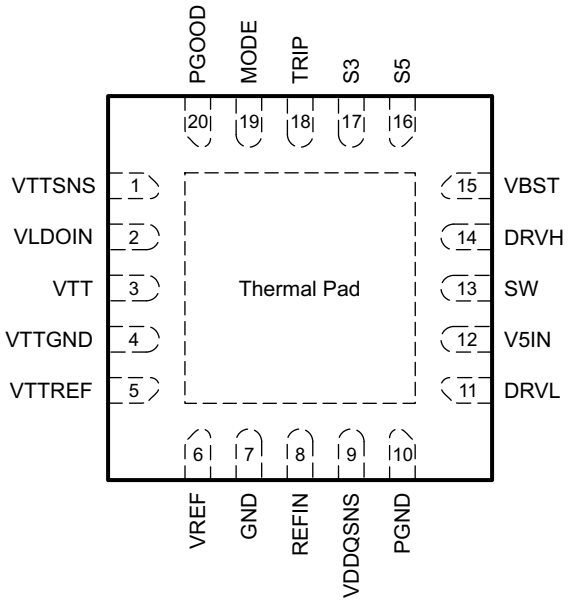


Figure 6-1. RUK Package 20-Pin WQFN Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH	14	O	High-side MOSFET gate driver output.
DRVL	11	O	Low-side MOSFET gate driver output.
GND	7	—	Signal ground.
MODE	19	I	Connect resistor to GND to configure switching frequency and discharge mode. (See Table 8-2.)
PGND	10	—	Gate driver power ground. $R_{DS(on)}$ current sensing input (+).
PGOOD	20	O	Powergood signal open drain output. PGOOD goes high when VDDQ output voltage is within the target range.
REFIN	8	I	Reference input for VDDQ. Connect to the midpoint of a resistor divider from VREF to GND. Add a capacitor for stable operation.
SW	13	I/O	High-side MOSFET gate driver return. $R_{DS(on)}$ current sensing input (–).
S3	17	I	S3 signal input. (See Table 8-1.)
S5	16	I	S5 signal input. (See Table 8-1.)
TRIP	18	I	Connect resistor to GND to set OCL at V_{TRIP} / 8. Output 10-µA current at room temperature, T_C = 4700 ppm/°C.
VBST	15	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from the VBST pin to the SW pin.
VDDQSNS	9	I	VDDQ output voltage feedback. Reference input for VTTREF. Also serves as power supply for VTTREF.
VLDOIN	2	I	Power supply input for VTT LDO. Connect VDDQ in typical application.
VREF	6	O	1.8-V reference output.
VTT	3	O	VTT 2-A LDO output. Need to connect 10 µF or larger capacitance for stability.
VTTGND	4	—	Power ground for VTT LDO.
VTTREF	5	O	Buffered VTT reference output. Need to connect 0.22 µF or larger capacitance for stability.
VTTSNS	1	I	VTT output voltage feedback.
V5IN	12	I	5-V power supply input for internal circuits and MOSFET gate drivers.
Thermal pad	—	—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	VBST	–0.3	36	V
	VBST(3)	–0.3	6	
	SW	–5	30	
	VLDOIN, VDDQSNS, REFIN	–0.3	3.6	
	VTTSNS	–0.3	3.6	
	PGND, VTTGND	–0.3	0.3	
	V5IN, S3, S5, TRIP, MODE	–0.3	6	
Output voltage(2)	DRVH	–5	36	V
	DRVH(3)	–0.3	6	
	DRVH(3) (duty cycle < 1%)	–2.5	6	
	VTTREF, VREF	–0.3	3.6	
	VTT	–0.3	3.6	
	DRVL	–0.3	6	
	DRVL (duty cycle < 1%)	–2.5	6	
	PGOOD	–0.3	6	
Junction temperature, T_J		–55	135	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V5IN	4.5		5.5	V
Input voltage range	VBST	–0.1		33.5	V
	VBST(2)	–0.1		5.5	
	SW	-3		28	
	SW(1)	–4.5		28	
	VLDOIN, VDDQSNS, REFIN	–0.1		3.5	
	VTTSNS	–0.1		3.5	
	PGND, VTTGND	–0.1		0.1	
	S3, S5, TRIP, MODE	–0.1		5.5	
Output voltage range	DRVH	–3		33.5	V
	DRVH(2)	–0.1		5.5	
	DRVH(1)	–4.5		33.5	
	VTTREF, VREF	–0.1		3.5	
	VTT	–0.1		3.5	
	DRVL	–0.1		5.5	
	PGOOD	–0.1		5.5	
T_J	Operating junction temperature	–55		125	°C

(1) This voltage should be applied for less than 30% of the repetitive period.
(2) Voltage values are with respect to the SW terminal.

7.4 Thermal Information

THERMAL METRIC(1)		TPS51216-EP RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –55°C to 125°C, VV5IN = 5 V, VLDOIN is connected to VDDQ output, V_{MODE} = 0 V, V_{S3} = V_{S5} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{V5IN(S0)}$	V5IN supply current, in S0	T_J = 25°C, No load, V_{S3} = V_{S5} = 5 V		590		µA
$I_{V5IN(S3)}$	V5IN supply current, in S3	T_J = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V		500		µA
$I_{V5INSDN}$	V5IN shutdown current	T_J = 25°C, No load, V_{S3} = V_{S5} = 0 V			1	µA
$I_{VLDOIN(S0)}$	VLDOIN supply current, in S0	T_J = 25°C, No load, V_{S3} = V_{S5} = 5 V			5	µA
$I_{VLDOIN(S3)}$	VLDOIN supply current, in S3	T_J = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V			5	µA
$I_{VLDOINSDN}$	VLDOIN shutdown current	T_J = 25°C, No load, V_{S3} = V_{S5} = 0 V			5	µA
VREF OUTPUT						
V_{VREF}	Output voltage	I_{VREF} = 30 µA, T_J = 25°C		1.8000		V
		0 µA ≤ I_{VREF} <300 µA, T_J = –55°C to 125°C	1.7820		1.8180	
$I_{VREFOCL}$	Current limit	V_{VREF} = 1.7 V	0.4	0.8		mA
VTTREF OUTPUT						
V_{VTTREF}	Output voltage			$V_{VDDQSNS}$/2		V
V_{VTTREF}	Output voltage tolerance to V_{VDDQ}	$\|I_{VTTREF}\|$ <100 µA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49.2%		50.8%	
		$\|I_{VTTREF}\|$ <10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49%		51%	
$I_{VTTREFOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF}= 0 V	10	18		mA
$I_{VTTREFOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF} = 1.8 V	10	17		mA
$I_{VTTREFDIS}$	VTTREF discharge current	T_J = 25°C, V_{S3} = V_{S5} = 0 V, V_{VTTREF} = 0.5 V	0.8	1.3		mA
VTT OUTPUT						
V_{VTT}	Output voltage			V_{VTTREF}		V
V_{VTTTOL}	Output voltage tolerance to VTTREF	$\|I_{VTT}\|$ ≤ 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF} = 0 A	–20		20	mV
		$\|I_{VTT}\|$ ≤ 1 A, 1.2 ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF} = 0 A	–30		30	
		$\|I_{VTT}\|$ ≤ 2 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF} = 0 A	–40		40	
		$\|I_{VTT}\|$ ≤ 1.5 A, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V, I_{VTTREF} = 0 A	–40		40	
$I_{VTTOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 0.7 V, I_{VTTREF} = 0 A	2	3		A
$I_{VTTOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8V, V_{VTT} = V_{VTTSNS} = 1.1 V, I_{VTTREF} = 0 A	2	3		
I_{VTTLK}	Leakage current	T_J = 25°C , V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = V_{VTTREF}			5	µA
$I_{VTTSNSBIAS}$	VTTSNS input bias current	V_{S3} = 5 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.5	0.0	0.5	
$I_{VTTSNSLK}$	VTTSNS leakage current	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–1	0	1	
I_{VTTDIS}	VTT Discharge current	T_J = 25°C, V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 1.8 V, V_{VTT} = 0.5 V, I_{VTTREF} = 0 A		7.8		mA
VDDQ OUTPUT						
$V_{VDDQSNS}$	VDDQ sense voltage			V_{REFIN}		
$V_{VDDQSNSTOL}$	VDDQSNS regulation voltage tolerance to REFIN	T_J = 25°C	–3		3	mV
$I_{VDDQSNS}$	VDDQSNS input current	$V_{VDDQSNS}$ = 1.8 V		39		µA
I_{REFIN}	REFIN input current	V_{REFIN} = 1.8 V	–0.1	0.0	0.1	µA
$I_{VDDQDIS}$	VDDQ discharge current	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, MODE pin pulled down to GND through 47 kΩ (Non-tracking)		12		mA
$I_{VLDOINDIS}$	VLDOIN discharge current	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, MODE pin pulled down to GND through 100 kΩ (Non-tracking)		1.2		A
SWITCH MODE POWER SUPPLY (SMPS) FREQUENCY						
f_{SW}	VDDQ switching frequency	V_{IN} = 5 V, $V_{VDDQSNS}$ = 1.8 V, R_{MODE} = 100 kΩ		300		kHz
		V_{IN} = 5 V, $V_{VDDQSNS}$ = 1.8 V, R_{MODE} = 200 kΩ		400		
$t_{ON(min)}$	Minimum on time	DRVH rising to falling1		60		ns
$t_{OFF(min)}$	Minimum off time	DRVH falling to rising	200	320	450	

7.5 Electrical Characteristics (continued)

T_J = –55°C to 125°C, VV5IN = 5 V, VLDOIN is connected to VDDQ output, V_{MODE} = 0 V, V_{S3} = V_{S5} = 5 V (unless otherwise noted)

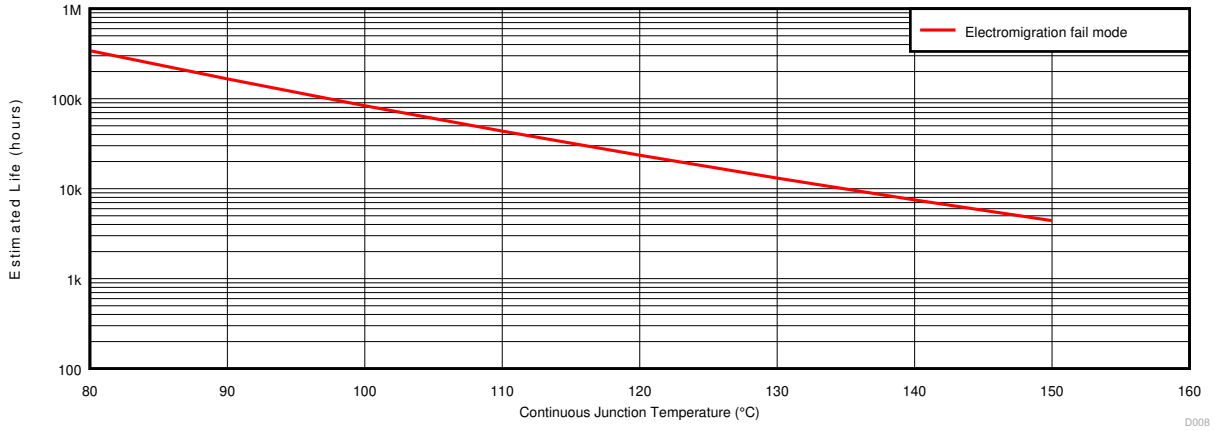
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VDDQ MOSFET DRIVER						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA		1.6	3.0	Ω
		Sink, I_{DRVH} = 50 mA		0.6	1.5	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA		0.9	2.0	
		Sink, I_{DRVL} = 50 mA		0.5	1.2	
t_{DEAD}	Dead time	DRVH-off to DRVL-on		10		ns
		DRVL-off to DRVH-on		20		
INTERNAL BOOT STRAP SW						
V_{FBST}	Forward voltage	$V_{V5IN-VBST}$, T_J = 25°C, I_F = 10 mA		0.1	0.2	V
I_{VBSTLK}	VBST leakage current	T_J = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA
LOGIC THRESHOLD						
I_{MODE}	MODE source current		14	15	16	µA
V_{THMODE}	MODE threshold voltage	MODE 0	580	600	620	mV
		MODE 1	829	854	879	
		MODE 2	1202	1232	1262	
		MODE 3	1760	1800	1840	
V_{IL}	S3/S5 low-level voltage				0.5	V
V_{IH}	S3/S5 high-level voltage		1.8			
V_{IHYST}	S3/S5 hysteresis voltage			0.25		
V_{ILK}	S3/S5 input leak current		–1	0	1	µA
SOFT START						
t_{SS}	VDDQ soft-start time	Internal soft-start time, C_{VREF} = 0.1 µF, S5 rising to $V_{VDDQSNS}$ > 0.99 × V_{REFIN}		1.1		ms
PGOOD COMPARATOR						
V_{THPG}	VDDQ PGOOD threshold	PGOOD in from higher	106%	108%	110%	
		PGOOD in from lower	90%	92%	94%	
		PGOOD out to higher	114%	116%	118%	
		PGOOD out to lower	82%	84%	86%	
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	3	5.9		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD in	0.8	1	1.2	ms
		Delay for PGOOD out, with 100 mV over drive		330		ns
$t_{PGSSDLY}$	PGOOD start-up delay	C_{VREF} = 0.1 µF, S5 rising to PGOOD rising		2.5		ms
PROTECTIONS						
I_{TRIP}	TRIP source current	T_J = 25°C, V_{TRIP} = 0.4 V	9	10	11	µA
TC_{ITRIP}	TRIP source current temperature coefficient1			4700		ppm/°C
V_{TRIP}	V_{TRIP} voltage range		0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3.0 V	360	375	390	mV
		V_{TRIP} = 1.6 V	190	200	210	
		V_{TRIP} = 0.2 V	20	25	30	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V	–390	–375	–360	mV
		V_{TRIP} = 1.6 V	–210	–200	–190	
		V_{TRIP} = 0.2 V	–30	–25	–20	
V_{ZC}	Zero cross detection offset			0		mV
V_{UVLO}	V5IN UVLO threshold voltage	Wake-up	4.2	4.4	4.5	V
		Shutdown	3.7	3.9	4.1	
V_{OVP}	VDDQ OVP threshold voltage	OVP detect voltage	118%	120%	122%	
t_{OVPDLY}	VDDQ OVP propagation delay	With 100 mV over drive		430		ns

7.5 Electrical Characteristics (continued)

T_J = –55°C to 125°C, VV5IN = 5 V, VLDOIN is connected to VDDQ output, V_{MODE} = 0 V, V_{S3} = V_{S5} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{UVP}	VDDQ UVP threshold voltage	UVP detect voltage	66%	68%	70%	
t_{UVPDLY}	VDDQ UVP delay			1		ms
$t_{UVPENDLY}$	VDDQ UVP enable delay			1.2		ms
V_{OOB}	OOB threshold voltage			108%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature1		140		°C
		Hysteresis1		10		

1. Ensured by design. Not production tested.



A. See data sheet for absolute maximum and minimum recommended operating conditions.
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
C. Enhanced plastic product disclaimer applies.

Figure 7-1. TPS51216-EP Derating Chart

7.6 Typical Characteristics

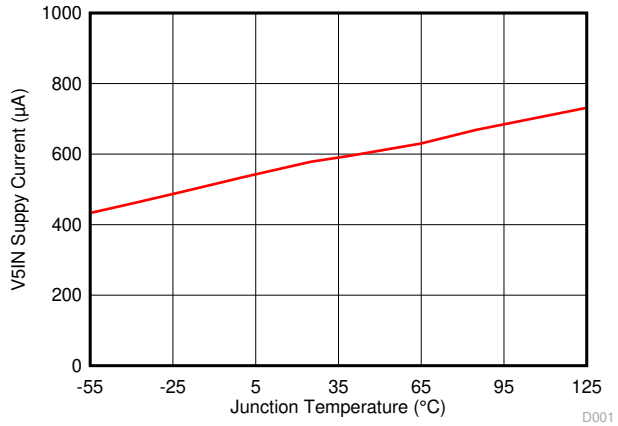


Figure 7-2. V5IN Supply Current vs Junction Temperature

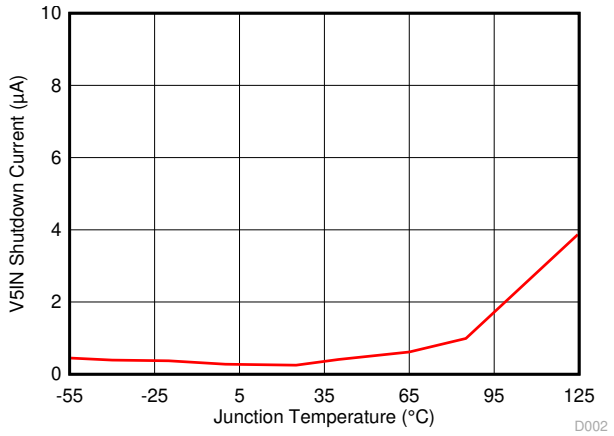


Figure 7-3. V5IN Shutdown Current vs Junction Temperature

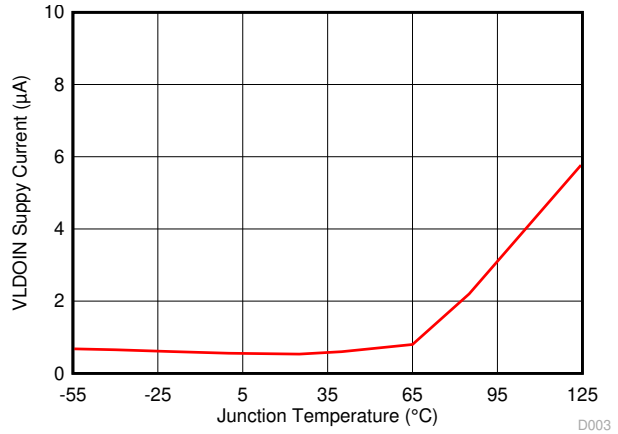


Figure 7-4. VLDOIN Supply Current vs Junction Temperature

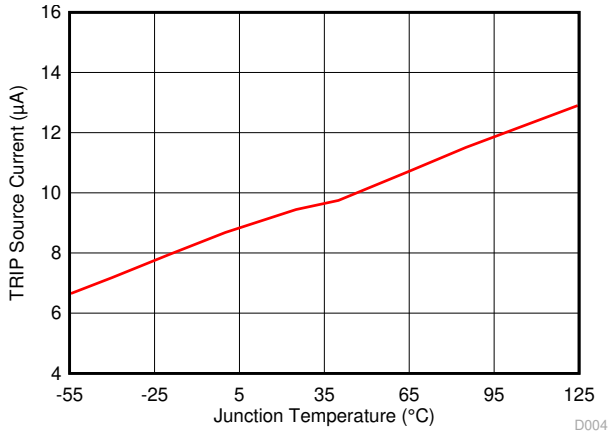


Figure 7-5. Current Sense Current vs Junction Temperature

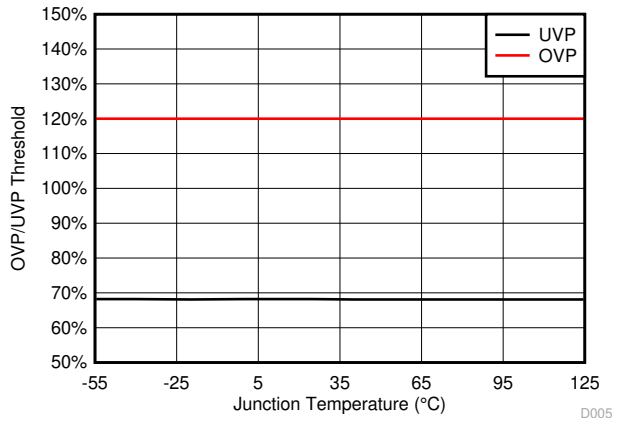


Figure 7-6. OVP/UVP Threshold vs Junction Temperature

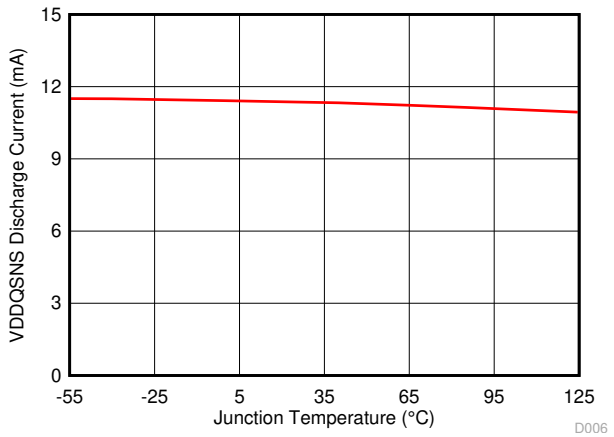


Figure 7-7. VDDQSNS Discharge Current vs Junction Temperature

7.6 Typical Characteristics (continued)

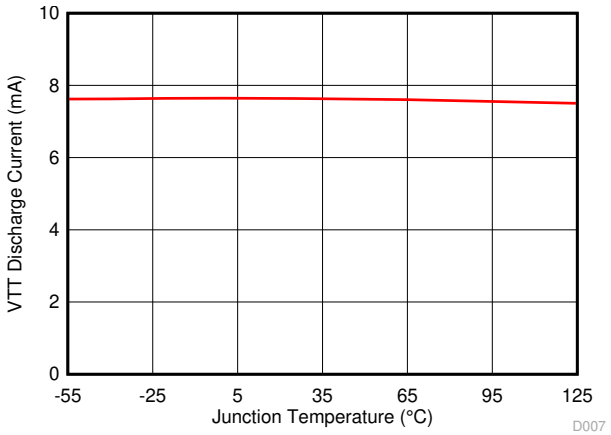


Figure 7-8. VTT Discharge Current vs Junction Temperature

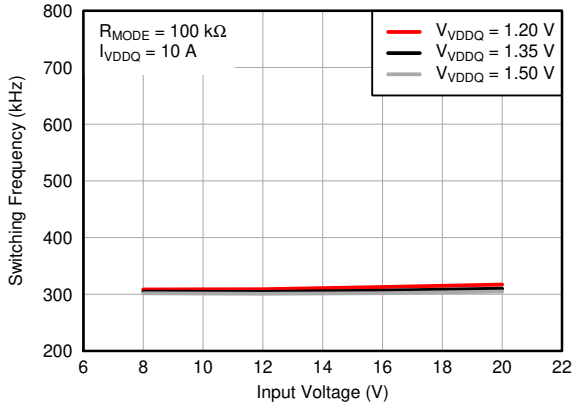


Figure 7-9. Switching Frequency vs Input Voltage

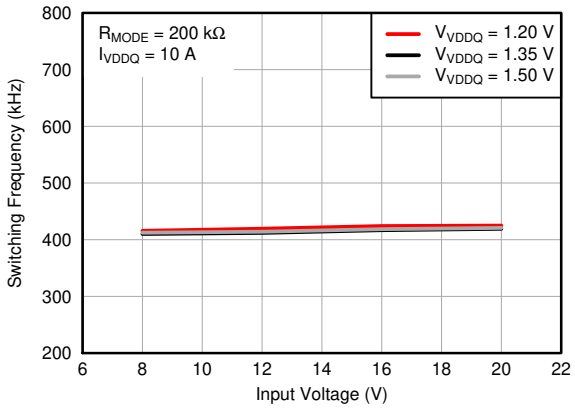


Figure 7-10. Switching Frequency vs Input Voltage

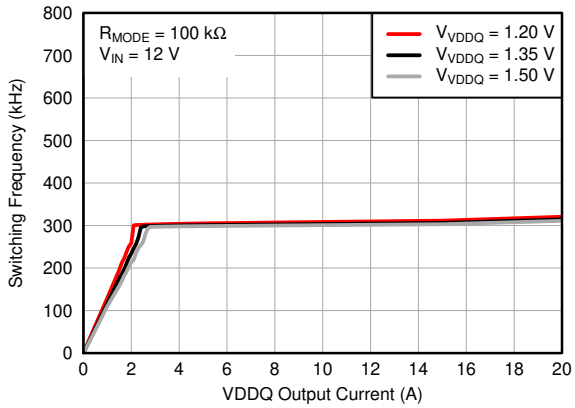


Figure 7-11. Switching Frequency vs Load Current

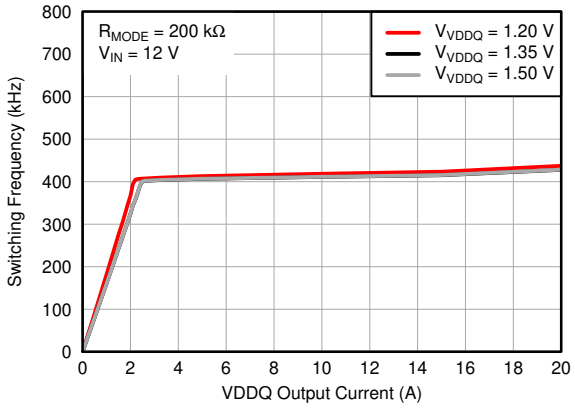


Figure 7-12. Switching Frequency vs Load Current

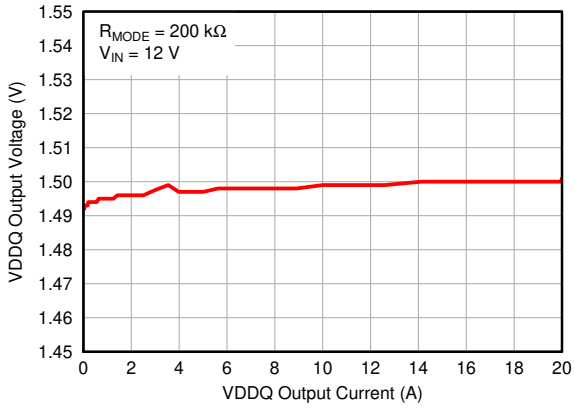


Figure 7-13. Load Regulation

7.6 Typical Characteristics (continued)

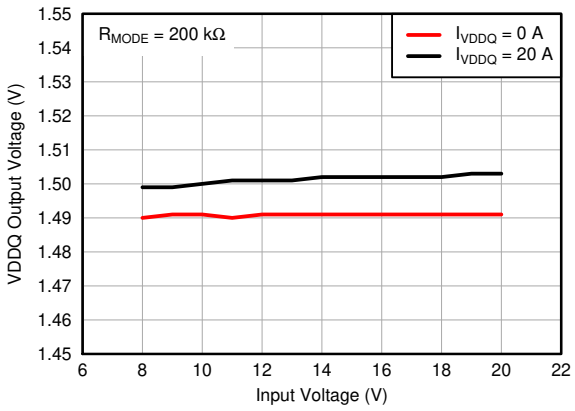


Figure 7-14. Line Regulation

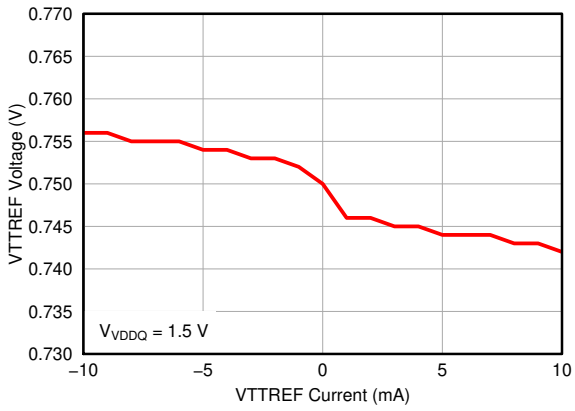


Figure 7-15. VTTREF Load Regulation

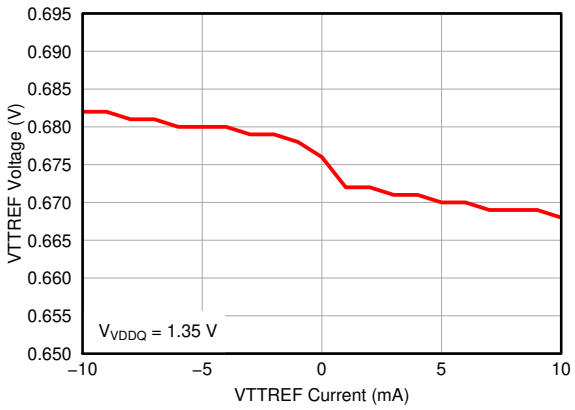


Figure 7-16. VTTREF Load Regulation

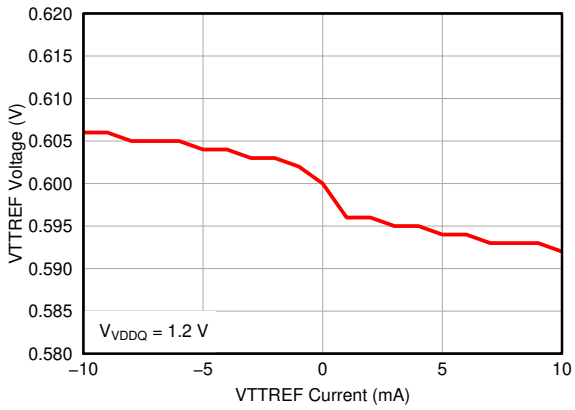


Figure 7-17. VTTREF Load Regulation

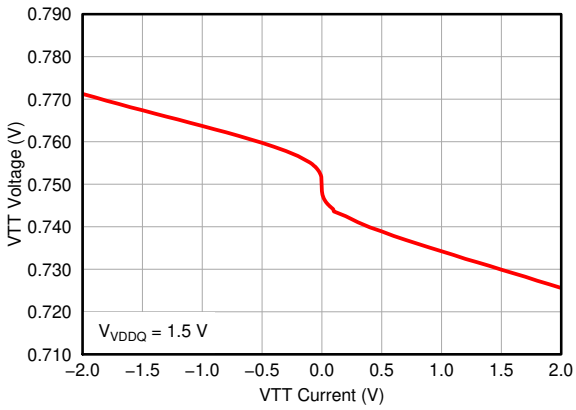


Figure 7-18. VTT Load Regulation

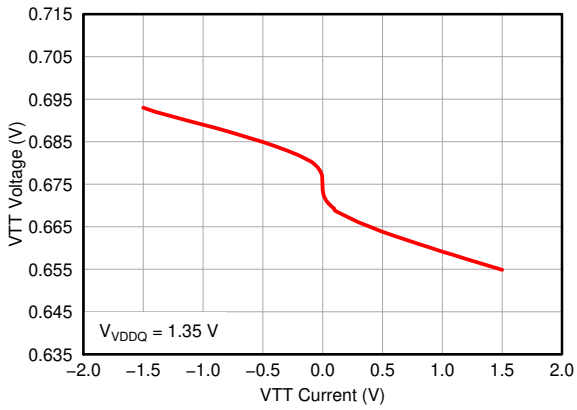


Figure 7-19. VTT Load Regulation

7.6 Typical Characteristics (continued)

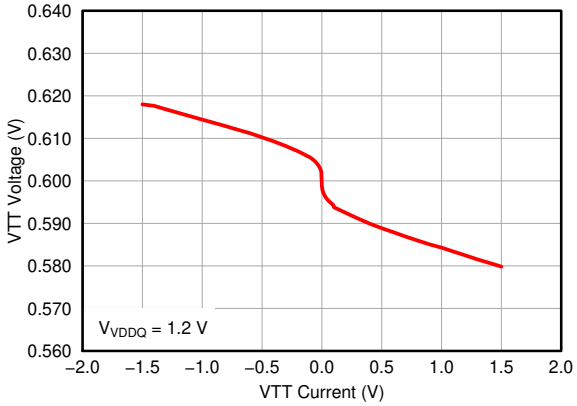


Figure 7-20. VTT Load Regulation

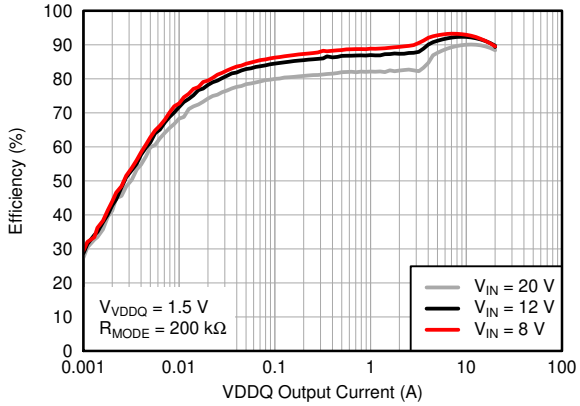


Figure 7-21. Efficiency

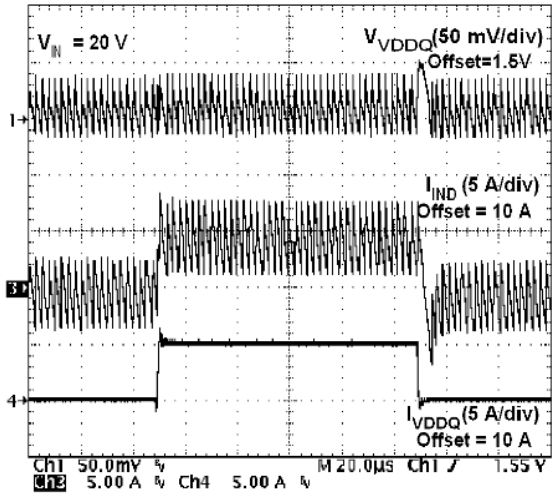


Figure 7-22. 1.5-V Load Transient Response

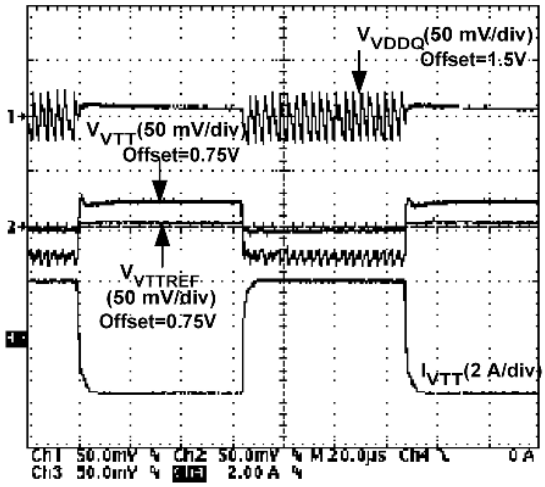


Figure 7-23. VTT Load Transient Response

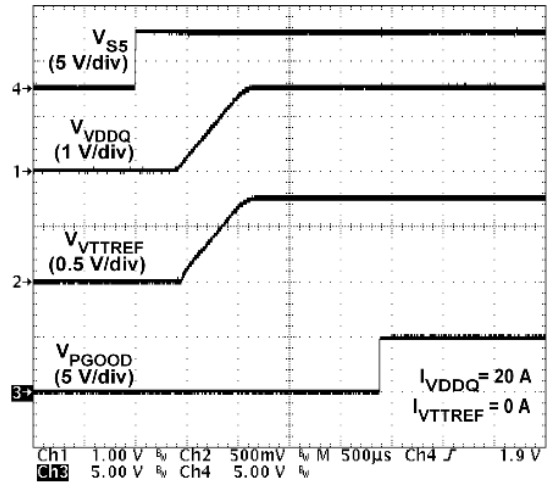


Figure 7-24. 1.5-V Startup Waveforms

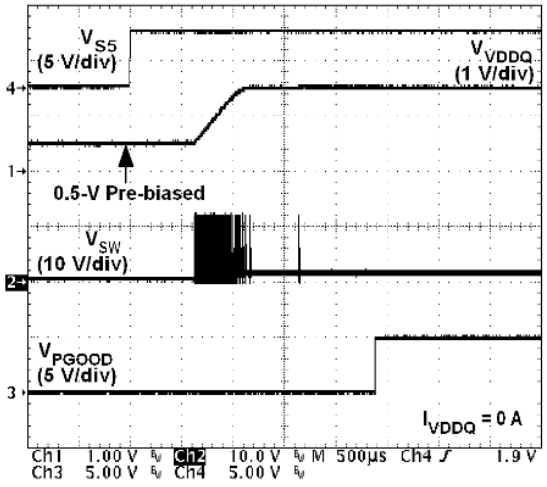


Figure 7-25. 1.5-V Startup Waveforms (0.5-V Pre-Biased)

7.6 Typical Characteristics (continued)

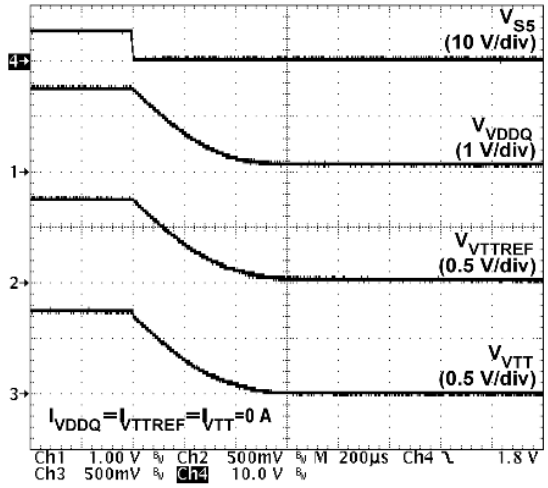


Figure 7-26. 1.5-V Soft-Stop Waveforms (Tracking Discharge)

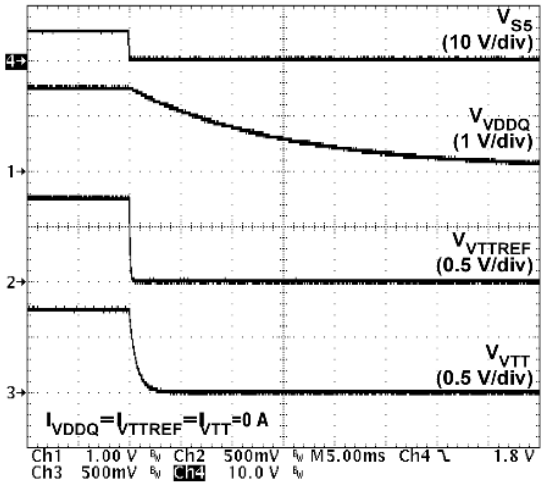


Figure 7-27. 1.5-V Soft-Stop Waveforms (Non-Tracking Discharge)

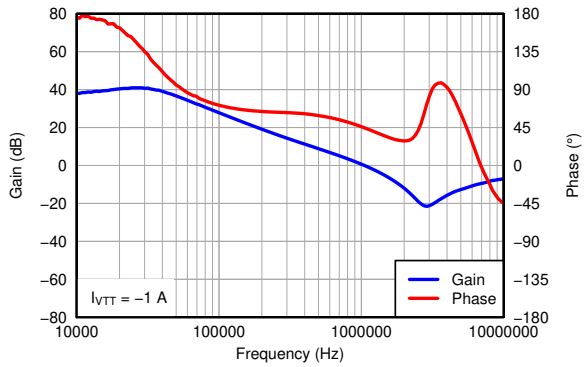


Figure 7-28. VTT Bode Plot (Sink)

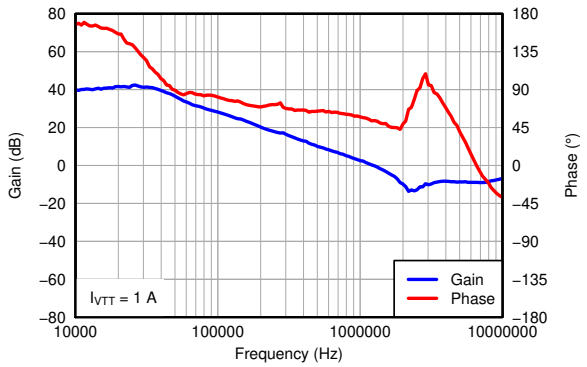


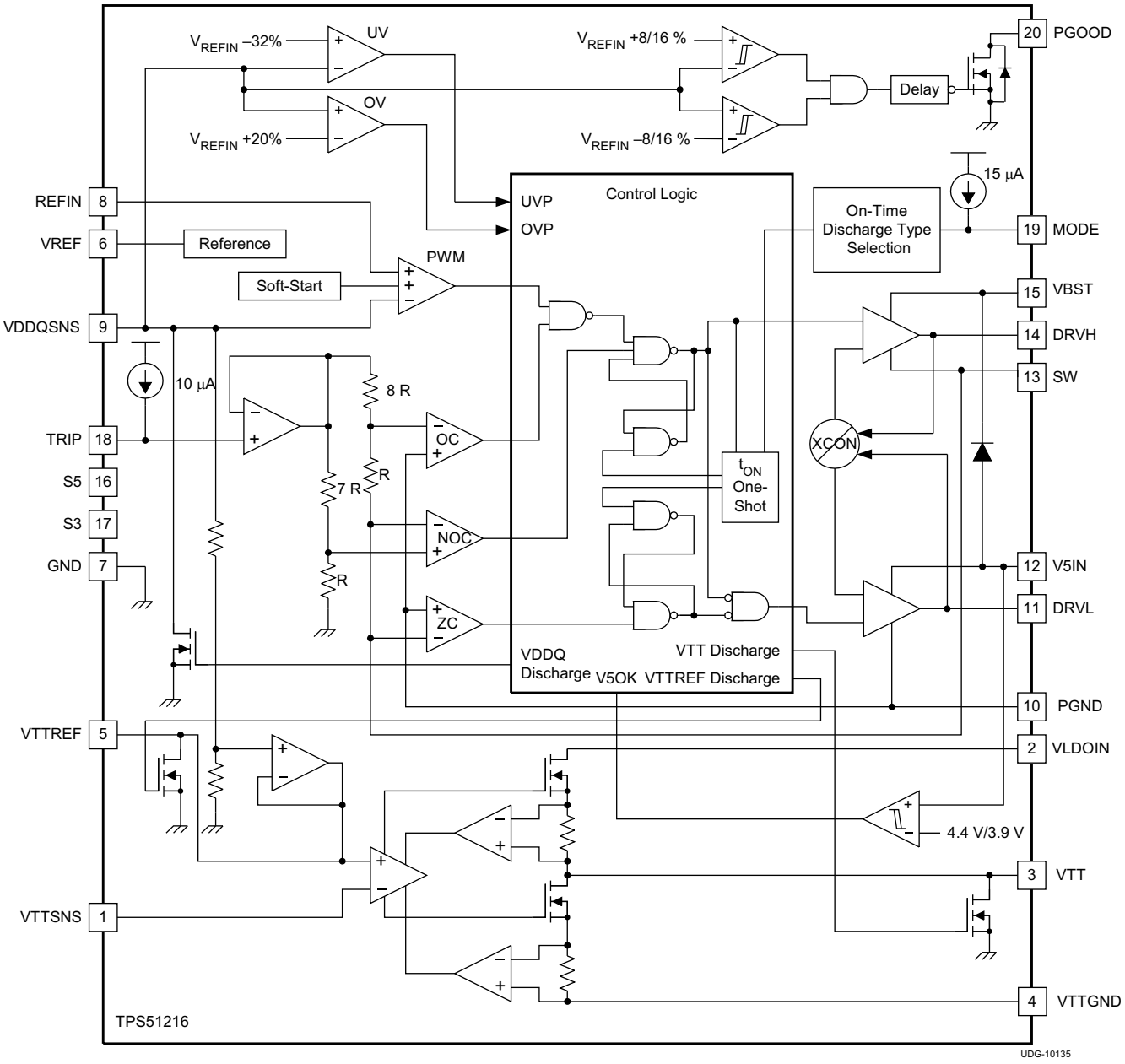
Figure 7-29. VTT Bode Plot (Source)

8 Detailed Description

8.1 Overview

TPS51216-EP provides complete Power Supply Solution for DDR2, DDR3 and DDR3L memory system.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VDDQ Switch Mode Power Supply Control

TPS51216-EP supports D-CAP mode which does not require complex external compensation networks and is suitable for designs with small external components counts. The D-CAP mode provides fast transient response with appropriate amount of equivalent series resistance (ESR) on the output capacitors. An adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51216-EP adjusts the on-time (t_{ON}) to be inversely proportional to the input voltage (V_{IN}) and proportional to the output voltage (V_{DDQ}). This makes a switching frequency fairy constant over the variation of input voltage at the steady state condition.

8.3.2 VREF and REFIN, VDDQ Output Voltage

The part provides a 1.8-V, ±0.8% accurate, voltage reference from VREF. This output has a 300-µA (max) current capability to drive the REFIN input voltage through a voltage divider circuit. A capacitor with a value of 0.1-µF or larger should be attached close to the VREF terminal.

The VDDQ switch-mode power supply (SMPS) output voltage is defined by REFIN voltage, within the range between 0.7 V and 1.8 V, programmed by the resister-divider connected between VREF and GND. (See *Section 9.2.2.2*.) A few nano farads of capacitance from REFIN to GND is recommended for stable operation.

8.3.3 Soft-Start and Powergood

TPS51216-EP provides integrated VDDQ soft-start functions to suppress in-rush current at start-up. The soft-start is achieved by controlling internal reference voltage ramping up. Figure 8-1 shows the start-up waveforms. The switching regulator waits for 400µs after S5 assertion. The MODE pin voltage is read in this period. A typical VDDQ ramp up duration is 700µs.

TPS51216-EP has a powergood open-drain output that indicates the VDDQ voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are ±8% (typ) and 1-ms delay for assertion (low to high), and ±16% (typ) and 330-ns delay for de-assertion (high to low) during running. The PGOOD comparator is enabled 1.1 ms after VREF is raised high and the start-up delay is 2.5 ms. Note that the time constant which is composed of the REFIN capacitor and a resistor divider needs to be short enough to reach the target value before PGOOD comparator enabled.

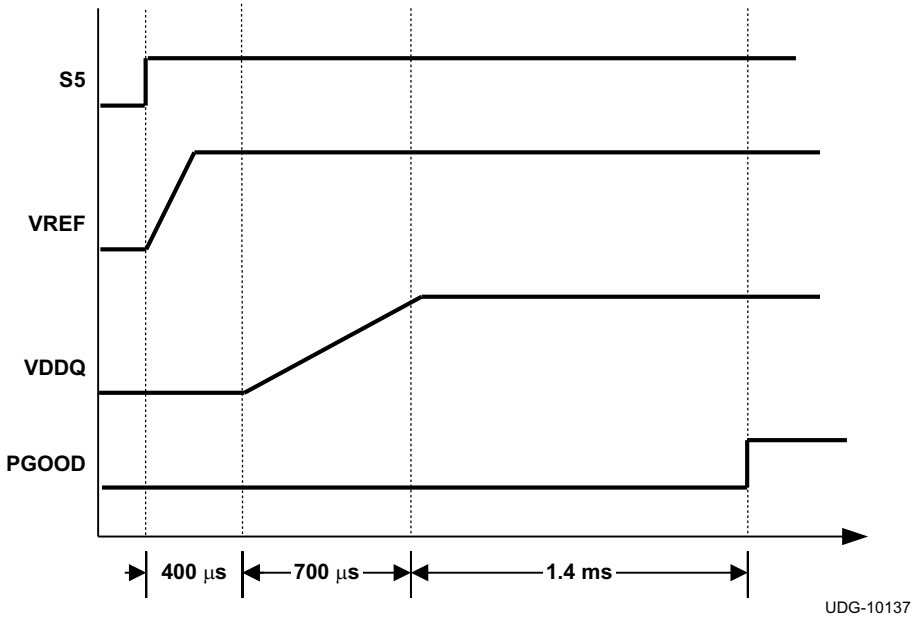


Figure 8-1. Typical Start-up Waveforms

8.3.4 Power State Control

The TPS51216-EP has two input pins, S3 and S5, to provide simple control scheme of power state. All of VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance state (high-Z). The VTT output floats and does not sink or source current in this state. In S4/S5 states (S3=S5=low), all of the three outputs are turned off and discharged to GND according to the discharge mode selected by MODE pin. Each state code represents as follow; S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 8-1)

Table 8-1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (high-Z)
S4/S5	LO	LO	OFF	OFF (discharge)	OFF (discharge)	OFF (discharge)

8.3.5 Discharge Control

In S4/S5 state, VDDQ, VTT, and VTTREF outputs are discharged based on the respective discharge mode selected above. The tracking discharge mode discharges VDDQ output through the internal VTT regulator transistors enabling quick discharge operation. The VTT output maintains tracking of the VTTREF voltage in this mode. (Refer to Figure 7-26.) After 4 ms of tracking discharge operation, the mode changes to non-tracking discharge. The VDDQ output must be connected to the VLDOIN pin in this mode. The non-tracking mode discharges the VDDQ and VTT pins using internal MOSFETs that are connected to corresponding output terminals. The non-tracking discharge is slow compared with the tracking discharge due to the lower current capability of these MOSFETs. (Refer to Figure 7-27.)

8.3.6 VTT Overcurrent Protection

The LDO has an internally fixed constant overcurrent limiting of 3-A (typ) for both sink and source operation.

8.3.7 V5IN Undervoltage Lockout (UVLO) Protection

TPS51216-EP has a 5-V supply UVLO protection threshold. When the V5IN voltage is lower than UVLO threshold voltage, typically 3.93 V, VDDQ, VTT, and VTTREF are shut off. This is a non-latch protection.

8.3.8 Thermal Shutdown

TPS51216-EP includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typical), VDDQ, VTT and VTTREF are shut off. The thermal shutdown state of VDDQ is open, VTT and VTTREF are high impedance (high-Z) respectively, and the discharge functions are disabled. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typical).

8.4 Device Functional Modes

8.4.1 MODE Pin Configuration

The TPS51216-EP reads the MODE pin voltage when the S5 signal is raised high and stores the status in a register. A 15-µA current is sourced from the MODE pin during this time to read the voltage across the resistor connected between the pin and GND. Table 8-2 shows resistor values, corresponding switching frequency, and discharge mode configurations.

Table 8-2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

TPS51216-EP is highly integrated synchronous step-down buck solution. The device is used to convert a higher DC-DC voltage to lower DC output voltage to provide VDDQ and VTT for various DDR memory power solutions.

9.1.1 D-CAP Mode

Figure 9-1 shows a simplified model of D-CAP mode architecture.

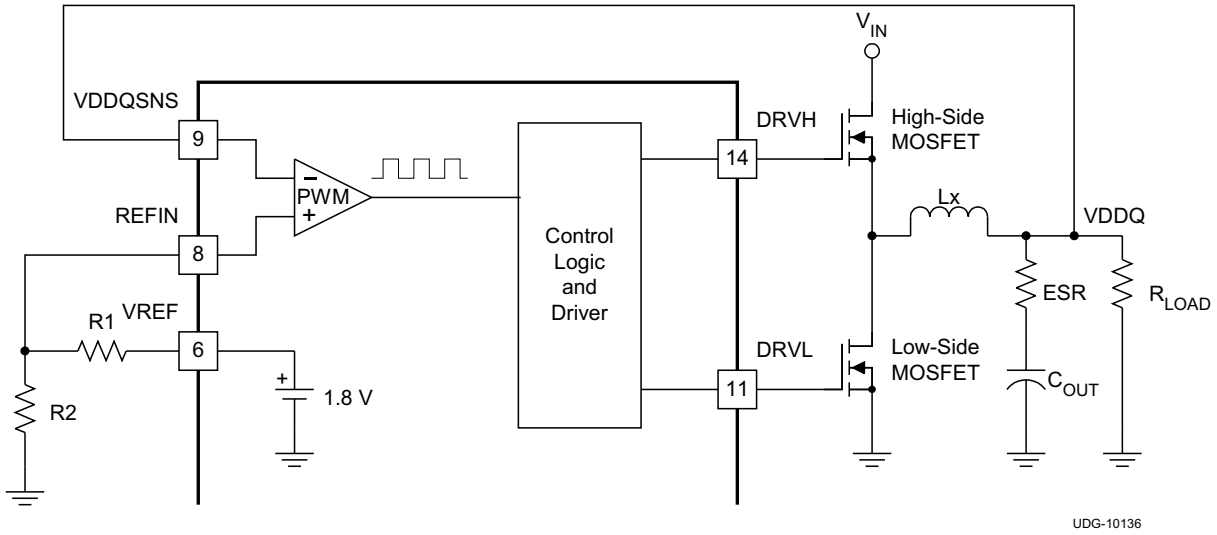


Figure 9-1. Simplified D-CAP Model

The VDDQSNS voltage is compared with REFIN voltage. The PWM comparator creates a set signal to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to maintain the voltage at the beginning of each on-cycle (or the end of each off-cycle) to be substantially constant. The DC output voltage monitored at VDDQ may have line regulation due to ripple amplitude that slightly increases as the input voltage increase. The D-CAP mode offers flexibility on output inductance and capacitance selections and provides ease-of-use with a low external component count. However, it requires a sufficient amount of output ripple voltage for stable operation and good jitter performance.

The requirement for loop stability is simple and is described in Equation 1. The 0-dB frequency, f_0 defined in Equation 1, is recommended to be lower than 1/3 of the switching frequency to secure proper phase margin.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{3} \quad (1)$$

where

- ESR is the effective series resistance of the output capacitor
- C_{OUT} is the capacitance of the output capacitor
- f_{sw} is switching frequency

Jitter is another attribute caused by signal-to-noise ratio of the feedback signal. One of the major factors that determine jitter performance in D-CAP mode is the down-slope angle of the VDDQSNS ripple voltage. Figure 9-2 shows, in the same noise condition, a jitter is improved by making the slope angle larger.

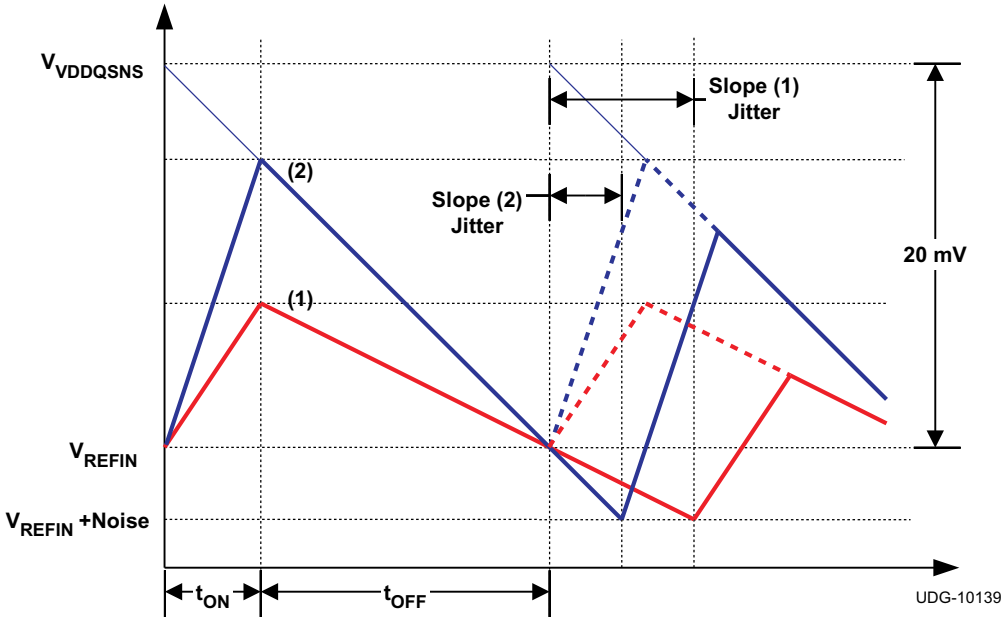


Figure 9-2. Ripple Voltage Slope and Jitter Performance

For a good jitter performance, use the recommended down slope of approximately 20 mV per switching period as shown in Figure 9-2 and Equation 2.

$$\frac{V_{OUT} \times ESR}{f_{SW} \times L_X} \geq 20\,mV \tag{2}$$

where

- V_{OUT} is the VDDQ output voltage
- L_X is the inductance

9.1.2 Light-Load Operation

In auto-skip mode, the TPS51216-EP SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. Equation 3 shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{3}$$

9.1.3 VTT and VTTREF

TPS51216-EP integrates two high performance, low-dropout linear regulators, VTT and VTTREF, to provide complete DDR2/DDR3/DDR3L power solutions. The VTTREF has a 10-mA sink/source current capability, and tracks ½ of VDDQSNS with ±1% accuracy using an on-chip ½ divider. A 0.22-µF (or larger) ceramic capacitor must be connected close to the VTTREF terminal for stable operation. The VTT responds quickly to track VTTREF within ±40 mV at all conditions, and the current capability is 2 A for both sink and source. A 10-µF (or larger) ceramic capacitor must be connected close to the VTT terminal for stable operation. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected

to the positive node of the VTT output capacitors as a separate trace from the high-current line to the VTT pin. (Refer to *Section 11.1* for details.)

When VTT is not required in the design, the following treatments are strongly recommended.

- Connect VLDOIN to VDDQ.
- Tie VTTSNS to VTT, and remove capacitors from VTT to float.
- Connect VTTGND to GND.
- Select MODE 0 or MODE 1 shown in Table 8-2 (select non-tracking discharge mode).
- Maintain a 0.22-µF capacitor connected at VTTREF.
- Pull down S3 to GND with 1-kΩ resistance.

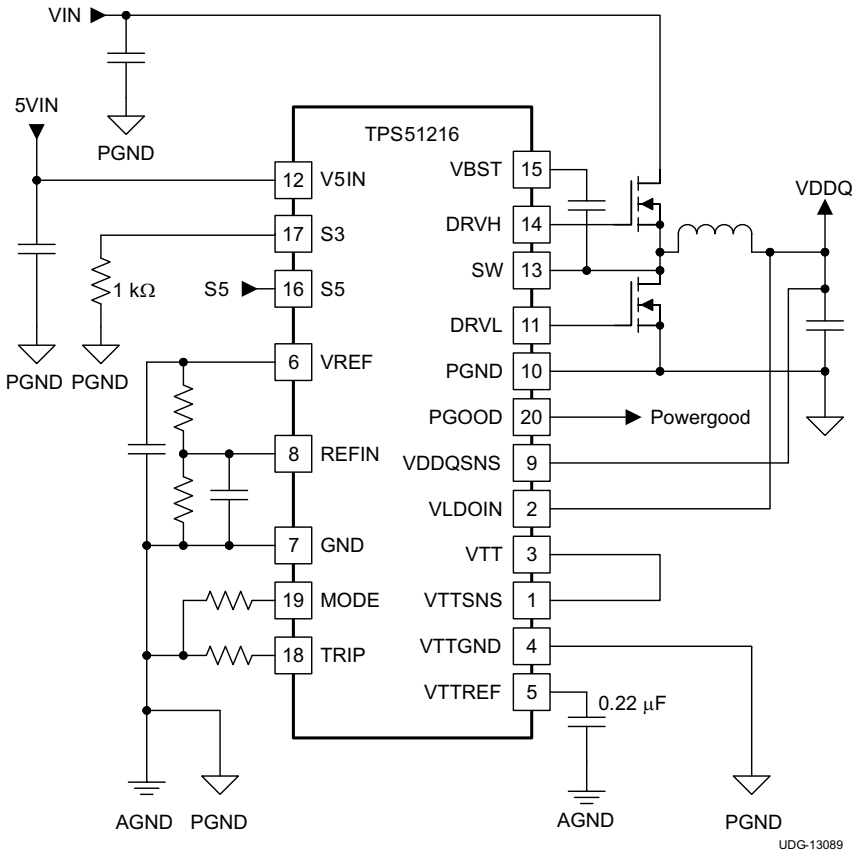


Figure 9-3. Application Circuit When VTT is not Required

9.1.4 VDDQ Overvoltage and Undervoltage Protection

TPS51216-EP sets the overvoltage protection (OVP) when the VDDQSNS voltage reaches a level 20% (typ) higher than the REFIN voltage. When an OV event is detected, the controller latches DRVH low and DRVL high. VTTREF and VTT are turned off and discharged using the non-tracking discharge MOSFETs regardless of the tracking mode.

The undervoltage protection (UVP) latch is set when the VDDQSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the VDDQ, VTT, and VTTREF outputs. UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle S5 or adjust the V5IN voltage down and up beyond the undervoltage lockout threshold.

9.1.5 VDDQ Overcurrent Protection

The VDDQ SMPS has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state using the low-side MOSFET $R_{DS(on)}$ and the controller maintains the off-state while the voltage across the low-side MOSFET is larger than the overcurrent trip level. The current monitor circuit inputs are PGND and SW pins so that those should be properly connected to the source and drain terminals of low-side MOSFET. The overcurrent trip level, V_{TRIP}, is determined by Equation 4.

$$V_{TRIP} = R_{TRIP} \times I_{TRIP} \tag{4}$$

where

- R_{TRIP} is the value of the resistor connected between the TRIP pin and GND
- I_{TRIP} is the current sourced from the TRIP pin. I_{TRIP} is 10 µA typically at room temperature, and has 4700 ppm/°C temperature coefficient to compensate the temperature dependency of the low-side MOSFET $R_{DS(on)}$.

Because the comparison is done during the off-state, V_{TRIP} sets the valley level of the inductor current. The load current OCL level, I_{OCL}, can be calculated by considering the inductor ripple current as shown in Equation 5.

$$I_{OCL} = \left(\frac{V_{TRIP}}{8 \times R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{V_{TRIP}}{8 \times R_{DS(on)}} \right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}} \tag{5}$$

where

- $I_{IND(ripple)}$ is inductor ripple current

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

9.2 Typical Application

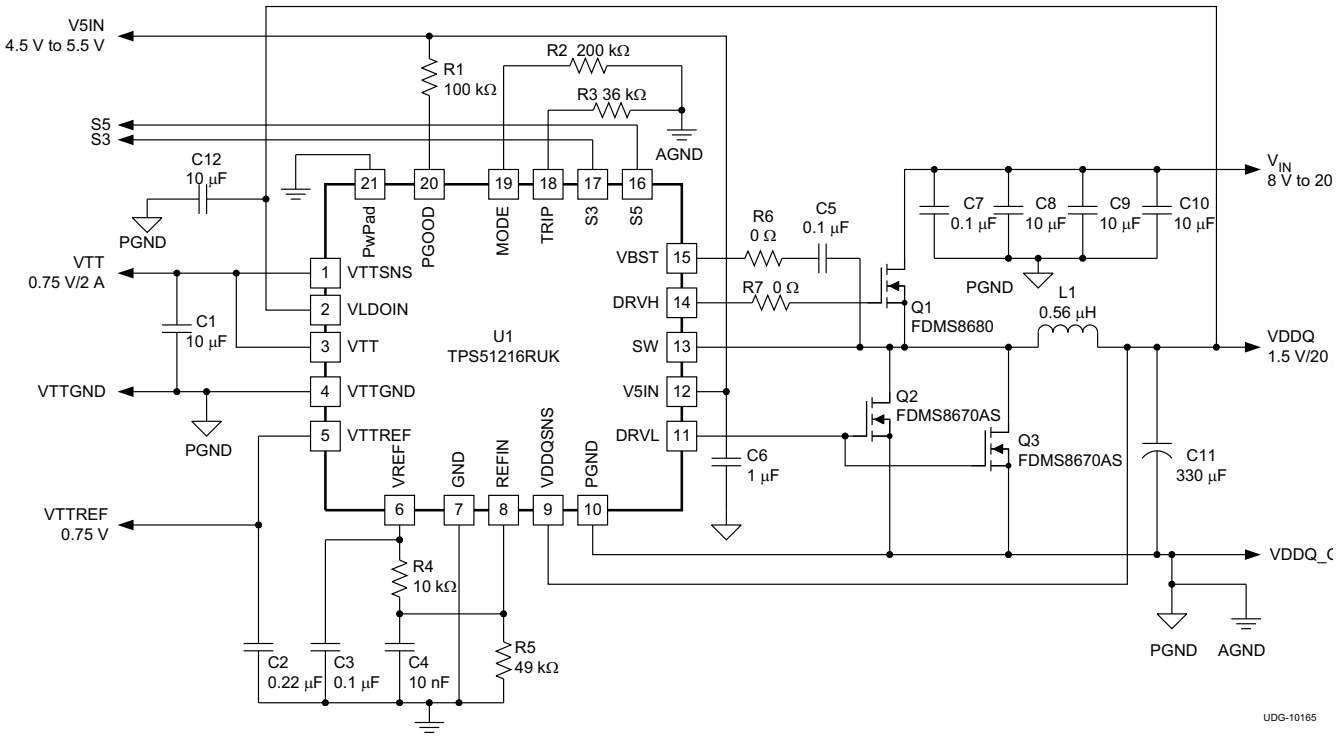


Figure 9-4. DDR3, 400-kHz Application Circuit, Tracking Discharge

9.2.1 Design Requirements

See Table 9-1 for the design parameters.

Table 9-1. Design Parameters

V_{IN}	VDDQ	I_{VDDQ}	VTT	I_{VTT}	F_{SW}
8 to 20 V	1.5 V	20 A	0.75 V	2 A	400 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 List of Materials

Table 9-2. DDR3, 400-kHz Application Circuit, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C8, C9, C10	3	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C11	1	330 µF, 2V, 6 mΩ	Panasonic	EEFSX0D331XE
L1	1	0.56 µH, 21 A, 1.56 mΩ	Panasonic	ETQP4LR56WFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2, Q3	2	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

For this example, the bulk output capacitor ESR requirement for D-CAP mode is described in Equation 6, whichever is greater.

$$ESR \geq \frac{20\,mV \times f_{SW} \times L}{V_{OUT}} \quad \text{or} \quad ESR \geq \frac{3}{2\pi \times f_{SW} \times C_{OUT}} \tag{6}$$

9.2.2.2 External Components Selection

The external components selection is simple in D-CAP mode.

1. **Determine the value of R4 and R5.**

   The output voltage is determined by the value of the voltage-divider resistor, R4 and R5, as shown in Figure 9-4. R4 is connected between VREF and REFIN pins, and R5 is connected between the REFIN pin and GND. Setting R4 as 10-kΩ is a good starting point. Determine R5 using Equation 7.

$$R5 = \frac{R4}{\left(\frac{1.8}{V_{OUT} - \left(\frac{I_{IND(ripple)} \times ESR}{2} \right)} \right) - 1} \tag{7}$$

2. **Choose the inductor.**

   The inductance value should be determined to yield a ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

$$L_X = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{O(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{8}$$

The inductor needs a low direct current resistance (DCR) to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 9.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L_X \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (9)$$

3. **Choose the OCL setting resistance, R_{TRIP}.**

Combining Equation 4 and Equation 5, R_{TRIP} can be obtained using Equation 10.

$$R_{TRIP} = \frac{8 \times \left(I_{OCL} - \left(\frac{\left(V_{IN} - V_{OUT}\right)}{\left(2 \times L_X\right)} \right) \times \frac{V_{OUT}}{\left(f_{SW} \times V_{IN}\right)} \right) \times R_{DS(on)}}{I_{TRIP}} \quad (10)$$

4. **Choose the output capacitors.**

TI recommends organic semiconductor capacitors or specialty polymer capacitors. Determine ESR to meet small signal stability and recommended ripple voltage. A quick reference is shown in Equation 11 and Equation 12.

$$\frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{3} \quad (11)$$

$$\frac{V_{OUT} \times ESR}{f_{SW} \times L_X} \geq 20\,mV \quad (12)$$

9.2.3 Application Curve

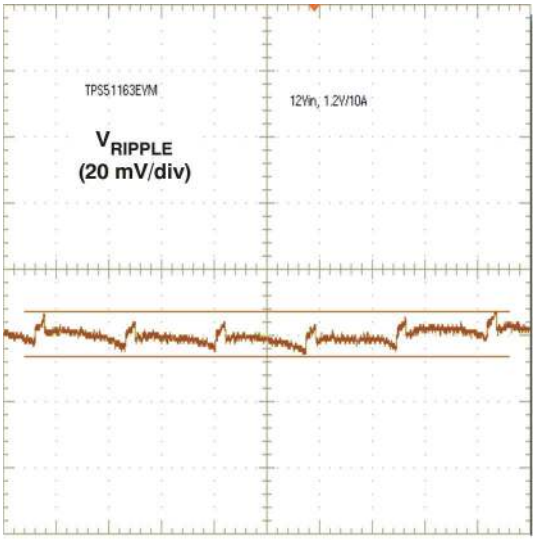


Figure 9-5. Output Ripple

10 Power Supply Recommendations

TPS51216-EP is designed to operate from input voltage supply range of 8 to 20 V. This supply must be well regulated. The power supply must be well bypassed for proper electrical performance. See *Section 11.2* for recommended bypass capacitor placement.

11 Layout

11.1 Layout Guidelines

Certain issues must be considered before designing a layout using the TPS51216-EP.

- VIN capacitors, VOUT capacitors, and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VDDQSNS, VTTSNS, MODE, REFIN, VREF, and TRIP should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH, or VBST to avoid coupling. Use internal layers as ground planes and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the VIN capacitors through the high and low-side MOSFETs, and back to the capacitors through ground. Connect the negative node of the VIN capacitors and the source of the low-side MOSFET at ground as close as possible. (Refer to loop number 1 of Figure 11-1)
  - The second important loop is the path from the low-side MOSFET through inductor and VOUT capacitors, and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of VOUT capacitors at ground as close as possible. (Refer to loop number 2 of Figure 11-1)
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5IN capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND, and back to source of the low-side MOSFET through ground. Connect negative node of V5IN capacitor, source of the low-side MOSFET and PGND at ground as close as possible. (Refer to loop number 3 of Figure 11-1)
- Because the TPS51216-EP controls output voltage referring to voltage across VOUT capacitor, VDDQSNS should be connected to the positive node of VOUT capacitor. In a same manner GND should be connected to the negative node of VOUT capacitor.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency and mode setting resistor from MODE pin to ground, and make the connections as close as possible to the device. The trace from the MODE pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and vias of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- VLDOIN should be connected to VDDQ output with short and wide traces. An input bypass capacitor should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VTT should be placed close to the pin with a short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of the VTT output capacitors as a separate trace from the high-current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage at the point of the load, it is recommended to attach the output capacitors at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitors.
- Consider adding a low pass filter (LPF) at VTTSNS in case the ESR of the VTT output capacitors is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.

- The negative node of the VTT output capacitors and the VTTREF capacitor should be tied together by avoiding common impedance to high-current path of the VTT source/sink current.
- GND pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitors, VTTREF capacitor and VDDQ capacitors with care to avoid additional ESR and/or ESL. GND and PGND should be connected together at a single point.
- In order to effectively remove heat from the package, prepare the thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground planes should be used to help dissipation.

CAUTION

Do **not** connect PGND pin directly to this thermal land underneath the package.

11.2 Layout Example

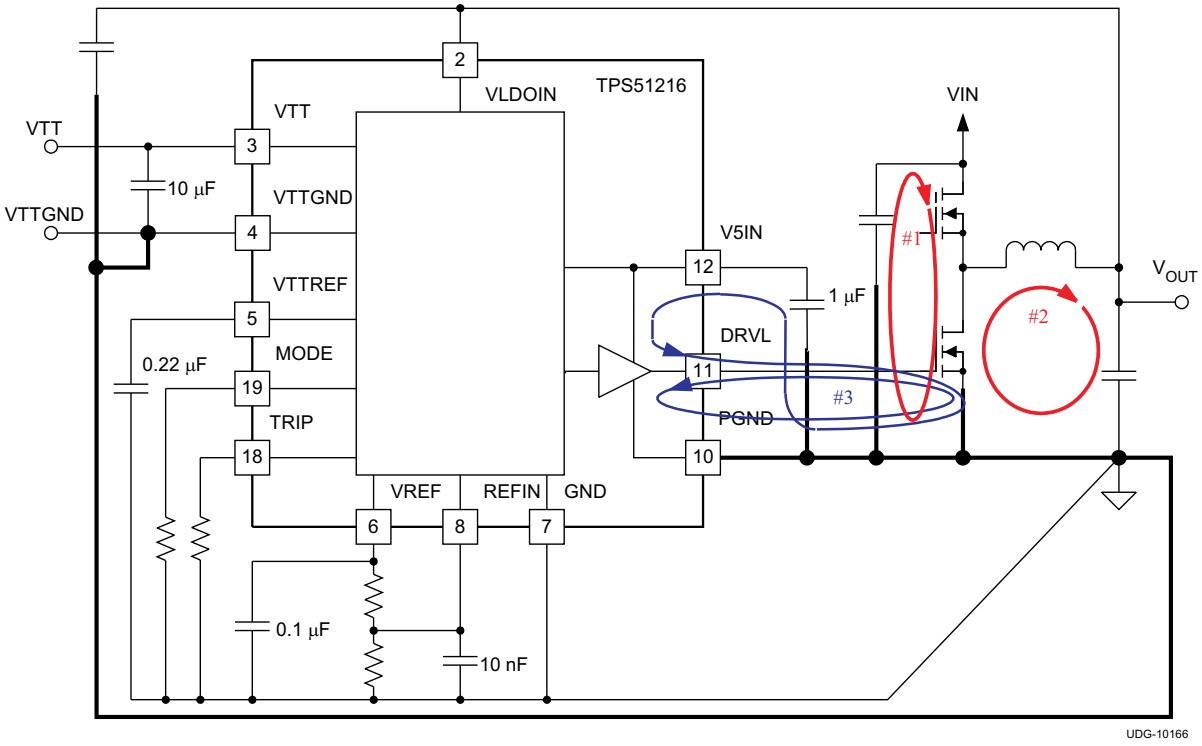


Figure 11-1. DC/DC Converter Ground System

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51216MRUKREP	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	51216M	Samples
V62/16601-01XE	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	51216M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS51216-EP :

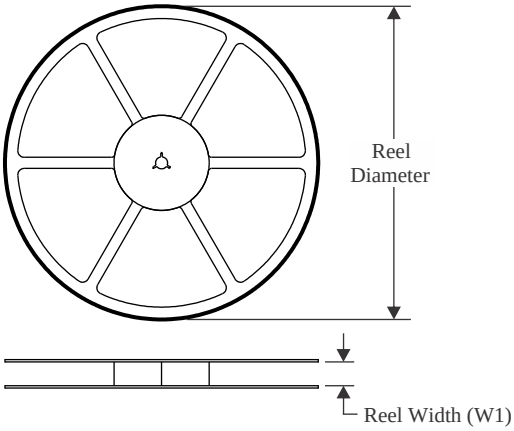
- Catalog : TPS51216

NOTE: Qualified Version Definitions:

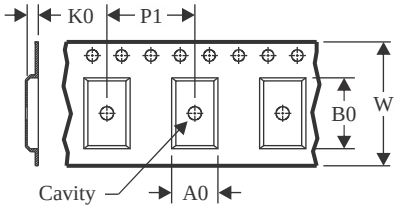
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

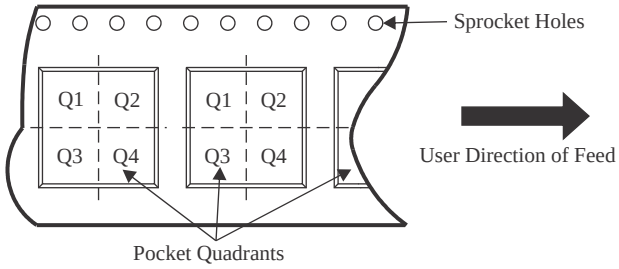


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

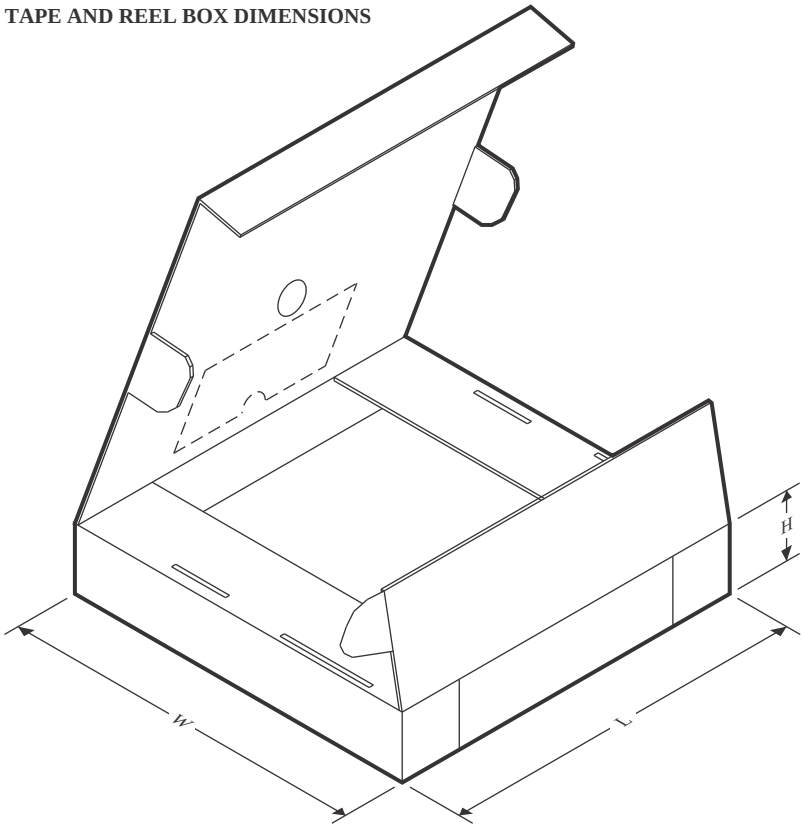
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51216MRUKREP	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

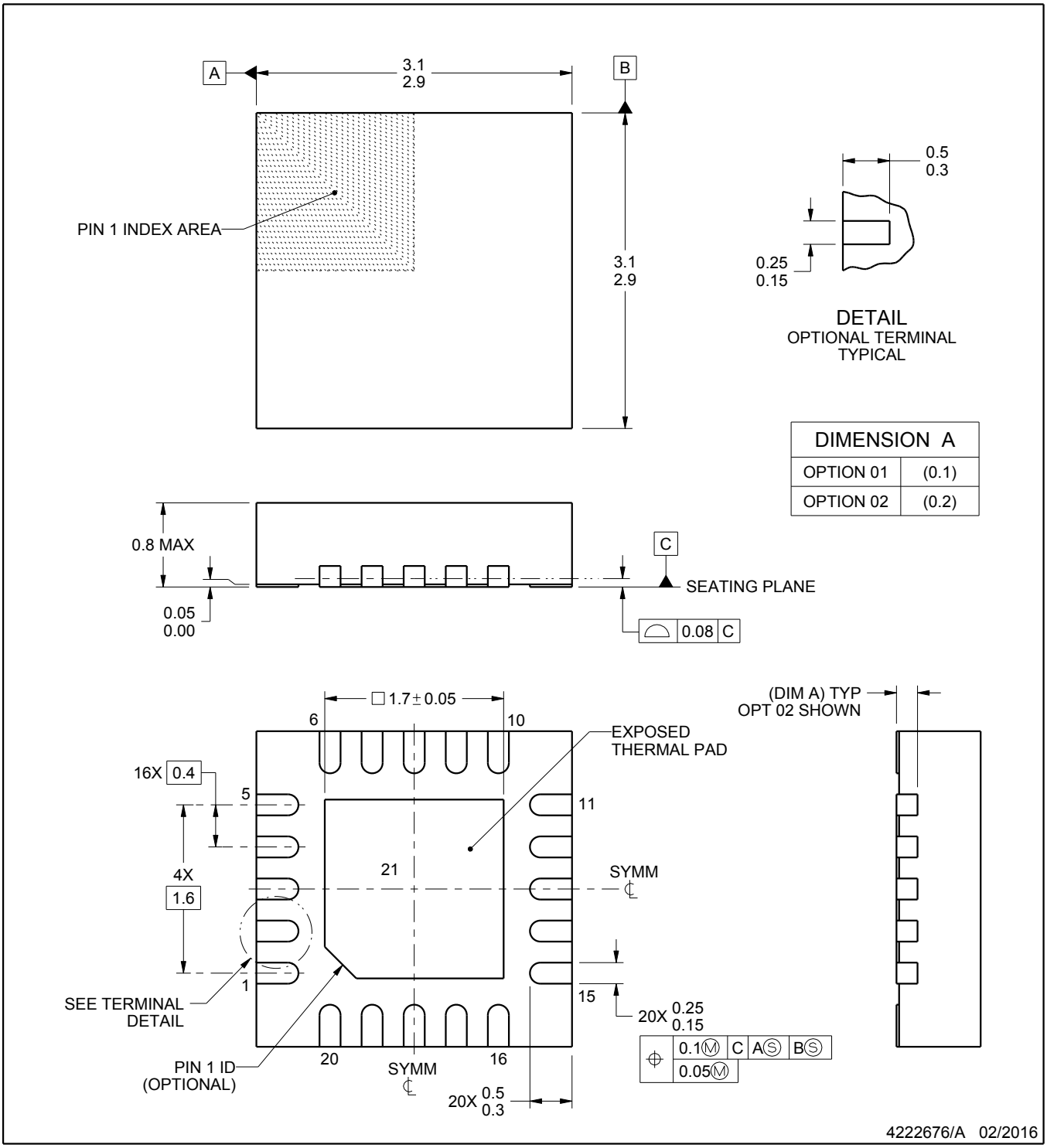
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51216MRUKREP	WQFN	RUK	20	3000	346.0	346.0	33.0

PACKAGE OUTLINE

RUK0020B

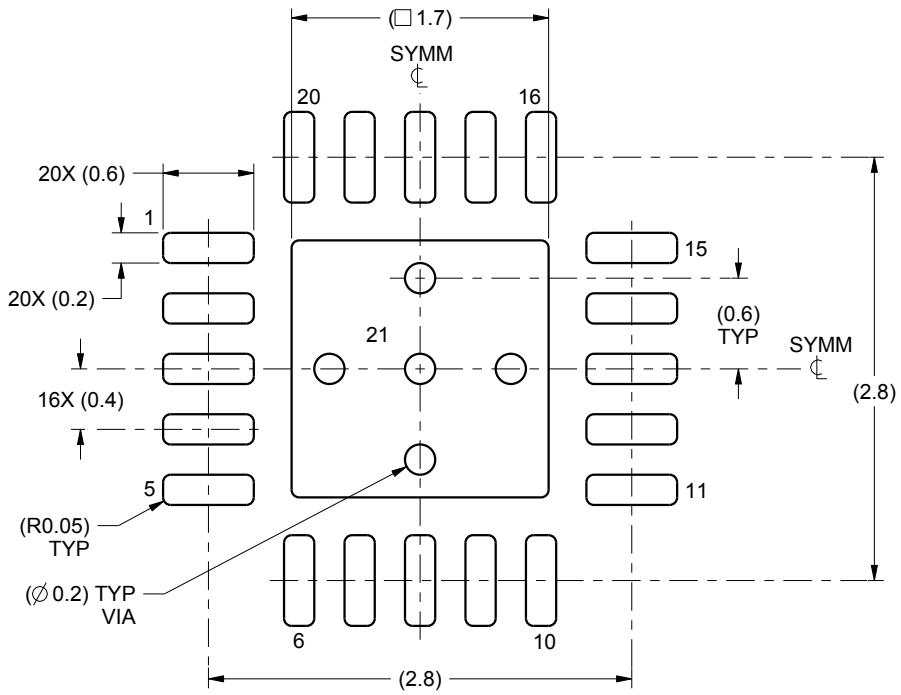
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

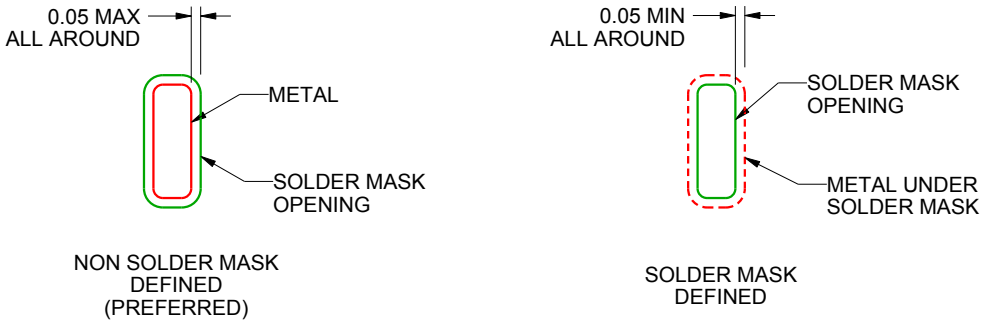


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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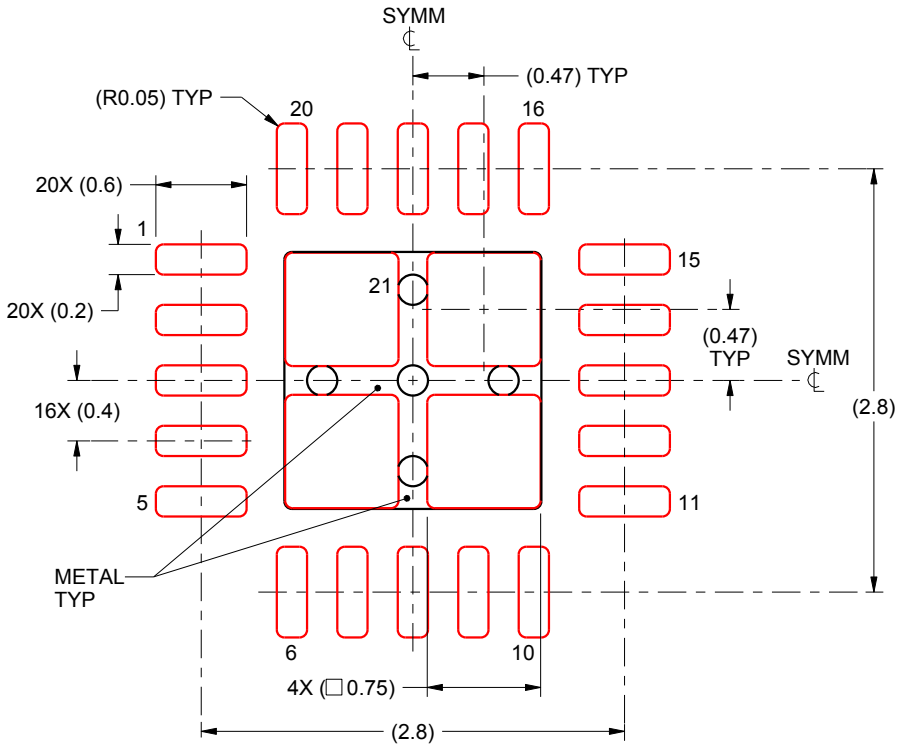
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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