Riverdi

RVT35HHBNWN00

EVE4 IPS 3.5" LCD TFT DATASHEET

Rev.1.6
2022-11-30

TFT MODULE SPECIFICATION

ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally Black/IPS	/
Size	3.5	Inch
Viewing Direction	Free	/
Outside Dimensions (W x H x D)	76.90 x 63.90 x 8.77	mm
Active Area (W x H)	70.08 x 52.56	mm
Pixel Pitch (W x H)	0.219 x 0.219	mm
Resolution	320 (RGB) x 240	/
Brightness	1000	cd/m^2
Color Depth	16.7 M	/
Pixel Arrangement	RGB Vertical Stripe	/
Driver IC of Board	BT817Q	/
Interface	SPI/QSPI	/
QSPI Flash Memory size	256	Mb
Host Connector	RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact	/
With/Without Touch	Without Touch Panel	/
Supply Voltage for Module	3.3	V
Supply Voltage for Backlight	5.0 (TYP.)	V
Audio amplifier	Build in class-D 1.5W audio amplifier	/
Weight	44	g

Note 1. RoHS3 compliant

Note 2. LCM weight tolerance: ± 5%

1. REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2021-04-19	Initial Release	
1.1	2021-06-03	Updating the drawing	
1.2	2021-07-20	Updating the supply voltage for backlight	
1.3	2021-07-30	Updating the drawing (dimensions in inches, adding the speaker), New template	
1.4	2021-12-06	Add the accessory link of Riverdi louder speaker: RVA-SPK1.5W-C150, which is matched with Riverdi all EVE4 series displays.	
1.5	2022-04-13	Correction on figure of simplified audio circuit design from R4, 1K resistor to R4, 100K resistor. R4 100K is the actual resistor value on PCB.	
1.6	2022-11-30	• Update the backlight electrical parameters • Add more detailed info like QSPI flash memory size, Audio amplifier etc. • Drawing update with adding grounding tape and dimensions overhaul	

2. CONTENTS

3. MODULE CLASSIFICATION INFORMATION

RV	T	35	H	H	B	N	W	N	00
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.

NO.	PARAMETER	SYMBOL
1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard
3.	DISPLAY SIZE	35 – 3.5"
4.	MODEL SERIAL NO.	H – High Brightness, IPS
5.	RESOLUTION	H – 320 x 240 px
6.	INTERFACE	B – SPI/QSPI
7.	FRAME	N – Without Mounting Metal Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	N – Without Touch Panel
10.	VERSION	00 – (00-99)

76.90 [3.028](TFT O.D.)
72.08 [2.838](TFT WINDOW)
70.08 [2.759](TFT A.A)
38.45 [1.514]
2.47 [0.097]
3.40 [0.134]
2.41 [0.095]
3.41 [0.134]

MAX 8.77 [0.345](MODULE O.D.)
3.26 [0.128](TFT)

RIBUS, 20PINS, 0.5mm PITCH
DOWNSIDE CONTACT, FLIP

17.52±1.0 [0.690±0.039]

63.90 [2.516](TFT O.D.)
54.56 [2.148](TFT WINDOW)
52.56 [2.069](TFT A.A.)
29.68 [1.169]

17.44±1.0 [0.687±0.039]

Riverdi Made In Poland

P1
P2
P5
A

1 20
1 54
10 1

LOUDSPEAKER OUTPUT
CONNECTOR

DETAIL A
SCALE 4:1
648102131822

2   1
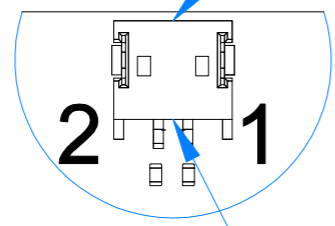
MATCHING CABLE CONNECTOR:
648002113322

LEDA — LEDK
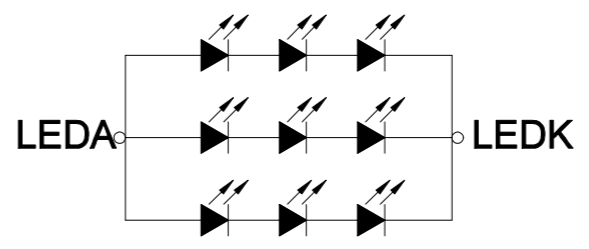
LED Diagram Circuit

TFT NOTES:
1. LCD TYPE: TRANSMISSIVE, NORMALLY BLACK, IPS
2. RESOLUTION: 320x240
3. VIEWING ANGLE: FREE
4. SURFACE LUMINANCE: 1000 cd/m^2
5. DRIVING IC ON THE BOARD: BT817Q
6. INTERFACE: SPI/QSPI
7. SUPPLY VOLTAGE FOR MODULE: 3.3V
8. SUPPLY VOLTAGE FOR BACKLIGHT:5.0V(TYP.),
   BUILT-IN LED INVERTER

GENERAL NOTES:
1. P5 IS AN UNUSED PCAP CONNECTOR ON THIS MODULE
2. OPERATING TEMPERATURE: -20°C ~ 70°C
3. STORAGE TEMPERATURE: -30°C ~ 80°C
4. WITHOUT INDIVIDUAL TOLERANCE: ±0.3mm[0.012inch]
5. RoHS3 COMPLIANT

5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	0	3.6		Note 1
Digital I/O signals (SPI/QSPI/GPIO) Voltage	VIN	-0.5	3.3	V	Note 1, 2
Supply voltage for Backlight	BLVDD	-0.3	7.0		Note 1
Operating Temperature	T_{OP}	-20	70	°C	
Storage Temperature	T_{ST}	-30	80	°C	
Storage Humidity (@ 25 ± 5°C)	H_{ST}	10	-	% RH	
Operating Ambient Humidity (@ 25 ± 5°C)	H_{OP}	10	-	% RH	

Note 1. Exceeding maximum values may cause improper operation or permanent damage to the unit.

Note 2. Digital I/O signals are to be connected to pins 3 ÷ 9, 11 and 12 pins at RiBUS connector (P1).

6. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	3.0	3.3	3.6	V	
Input Voltage "H" Level	V_{IH}	2.0	-	3.3	V	
Input Voltage "L" Level	V_{IL}	0	-	0.8	V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Current drawn from VDD@3.3V	IVDD	-	43	337	mA	Note 1

Note 1. Animated pictures are displayed on the screen and there is no QSPI communication during the measurement of TYP and MAX values.

TYP value is measured when the audio is off.

MAX value is measured when the audio is on, and volume is set to maximum

Riverdi loudspeaker RVA-SPK1.5W-C150 is applied during the measurement.

7. BACKLIGHT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Backlight	BLVDD	4.5	5.0	5.5	V	Note 1
Lifetime	-	-	50,000	-	hours	Note 2

Note 1. The Min voltage of BL driver is 2.7V, the modules will work, but full brightness can't be achieved.

Note 2. Operating life means the period in which the LED brightness goes down to 50% of the initial brightness. Typical operating lifetime is the estimated parameter.

PARAMETER	SYMBOL	MIN BL	50% BL	100% BL	UNIT	NOTE
Current drawn from BLVDD @4.5V	I_{BLVDD}	TBD	TBD	TBD	mA	Note 3
Current drawn from BLVDD @5.0V		4.29	56	135		
Current drawn from BLVDD @5.5V		4.16	51	119		

Note 3. To control the backlight dimming, please refer to subchapter 11.4.

MIN BL is when REG_PWM_DUTY = 1

50% BL is when REG_PWM_DUTY = 64

100% BL is when REG_PWM_DUTY = 128

8. ELECTRO-OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	RMK	NOTE
Response Time	Tr+Tf	θ=0° ∅=0° Ta=25 °C	-	50	-	ms	FIG 1.	4
Contrast Ratio	Cr		-	700	-	---	FIG 2.	1
Luminance Uniformity	δ WHITE		-	75	-	%	FIG 2.	3
Surface Luminance	Lv		-	1000	-	cd/m^2	FIG 2.	2
Viewing Angle Range	θ	∅ = 90°	-	80	-	deg	FIG 3.	6
		∅ = 270°	-	80	-	deg	FIG 3.	
		∅ = 0°	-	80	-	deg	FIG 3.	
		∅ = 180°	-	80	-	deg	FIG 3.	
CIE (x, y) Chromaticity	Rx	θ=0° ∅=0° Ta=25 °C	0.573	0.613	0.653	-	FIG 2.	5
	Ry		0.317	0.357	0.397	-		
	Gx		0.324	0.364	0.404	-		
	Gy		0.263	0.603	0.643	-		
	Bx		0.110	0.150	0.190	-		
	By		0.069	0.109	0.149	-		
	Wx		0.277	0.317	0.357	-		
	Wy		0.299	0.339	0.379	-		

Note 1. Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio } = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 1. The test equipment is BM-7A.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then calculating the average value.

Note 6. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

Note 7. Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A

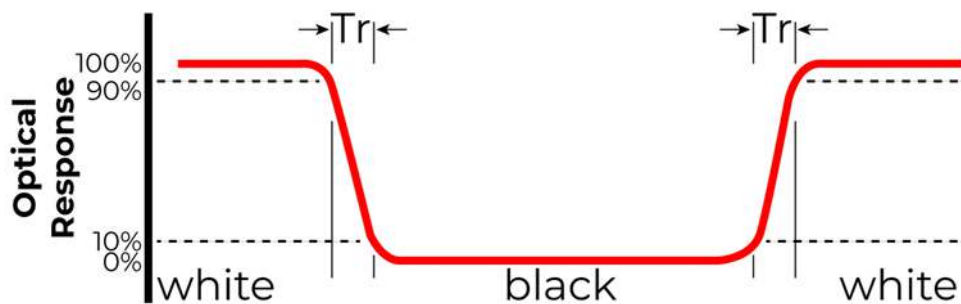*Figure 1. The definition of response time*

Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity
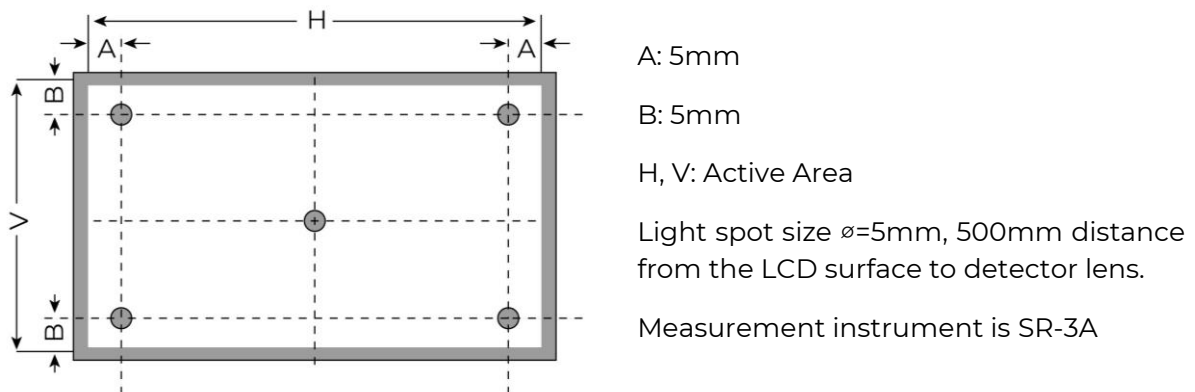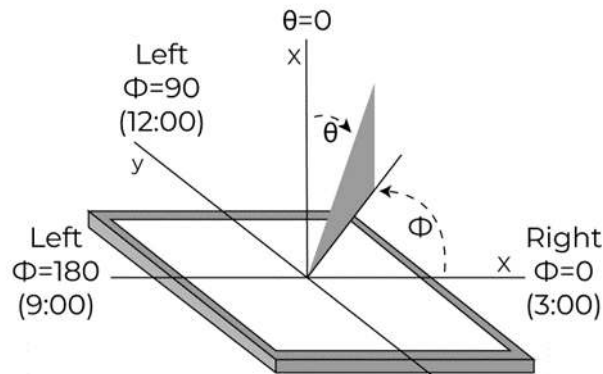

A: 5mm

B: 5mm

H, V: Active Area

Light spot size ⌀=5mm, 500mm distance from the LCD surface to detector lens.

Measurement instrument is SR-3A

Figure 3. The definition of viewing angle

9. INTERFACES DESCRIPTION

9.1 P1 connector - RiBUS description

PIN NO.	CONNECTOR	DESCRIPTION	NOTE
1	VDD	Supply voltage for module; TYP 3.3 V	
2	GND	Ground	
3	SPI_SCLK	SPI SCK signal	
4	MISO/ IO.1	SPI MISO signal / SPI Quad mode: SPI data line 1	
5	MOSI/ IO.0	SPI MOSI signal / SPI Quad mode: SPI data line 0	
6	CS	SPI chips select signal	
7	INT	Interrupt signal from device to the system, Active Low, internally 47k Pull UP	
8	RST/PD	Reset / Power down signal, Active Low, Internally Pulled UP 47k	
9	GPIO.0	GPIO.0	
10	DISP_AUDIO	Display audio in/out	
11	GPIO.1/IO.2	SPI Single/Dual mode: General purpose IO0. QSPI mode: SPI data line 2	
12	GPIO.2/IO.3	SPI Single/Dual mode: General purpose IO1. QSPI mode: SPI data line 3	
13	NC	Not connected	
14	NC	Not connected	
15	NC	Not connected	
16	NC	Not connected	
17	BLVDD	Supply voltage for backlight	
18	BLVDD	Supply voltage for backlight	
19	BLGND	Backlight Ground, internally connected to GND	
20	BLGND	Backlight Ground, internally connected to GND	

Note 1. Matched 20 pins, 0.5 mm pitch, FFC accessory: FFC0520150

## 9.2 P2 connector description - Audio interface description

PIN NO.	SYMBOL	DESCRIPTION	NOTE
1	SPEAKER +	Speaker coil "+" terminal	Note 1
2	SPEAKER -	Speaker coil "-" terminal	

The audio circuit allows for the following 3 modes:

1. To play sounds from BT817Q on internal amplifier U3.

2. To play sounds from host on internal amplifier U3.

3. To play sounds from BT817Q on external amplifier.

Note 1. Matched Riverdi louder speaker for all EVE4 series displays: RVA-SPK1.5W-C150

Figure 4. The simplified audio circuit design
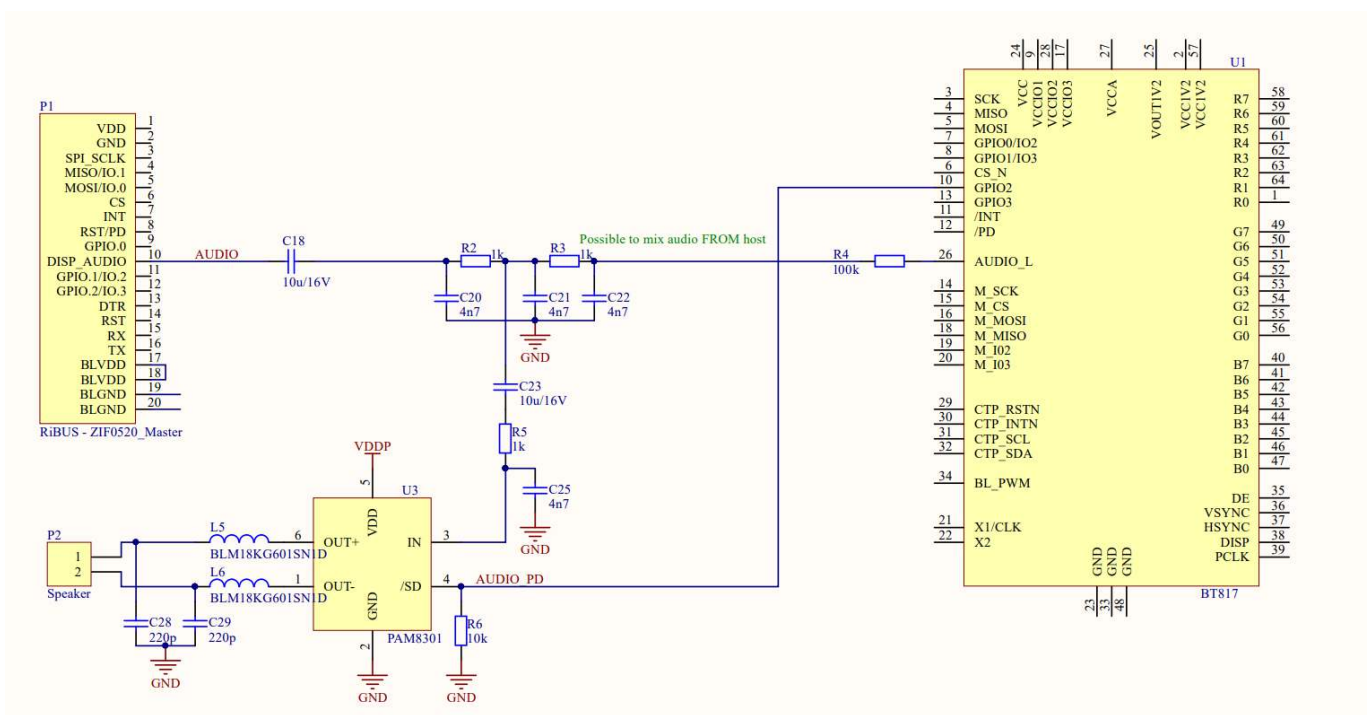
10. BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

10.1 Serial host interface

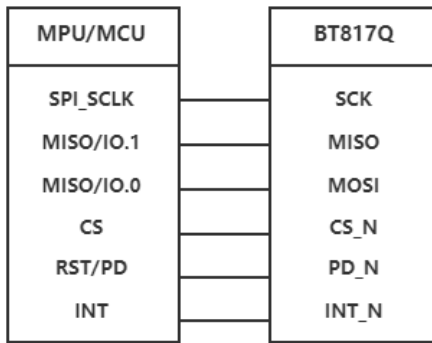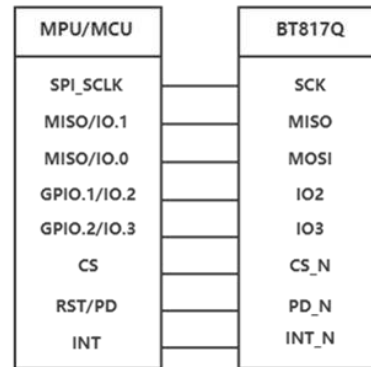Figure 5.SPI single/dual interface connection

Figure 6. QSPI interface connection

**SPI Interface** – the SPI slave interface operates up to 30MHz.

Only SPI mode 0 is supported. The SPI interface is selected by default.

QSPI Interface – the QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH.
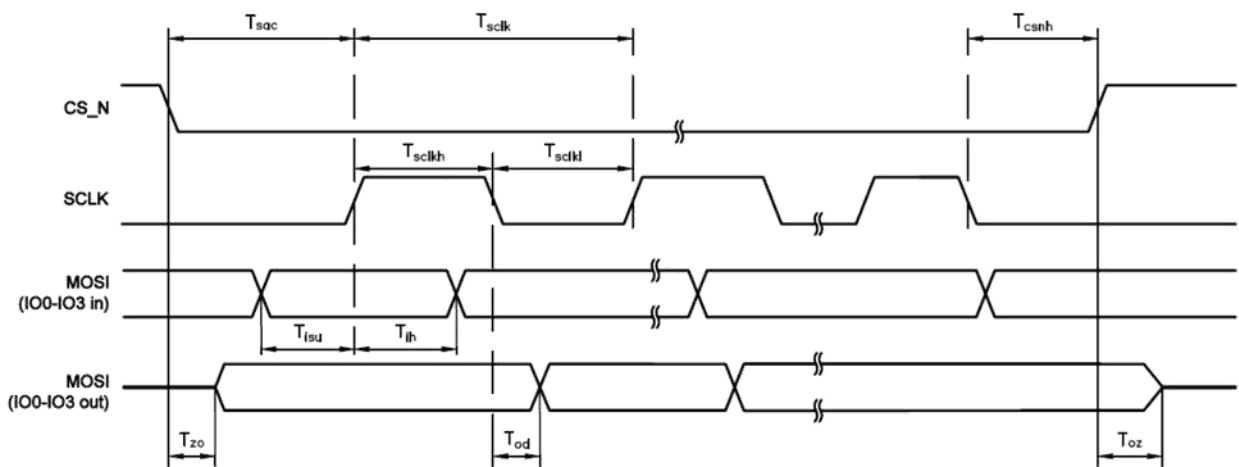
10.2 Block Diagram

Figure 7. BT817Q Block diagram
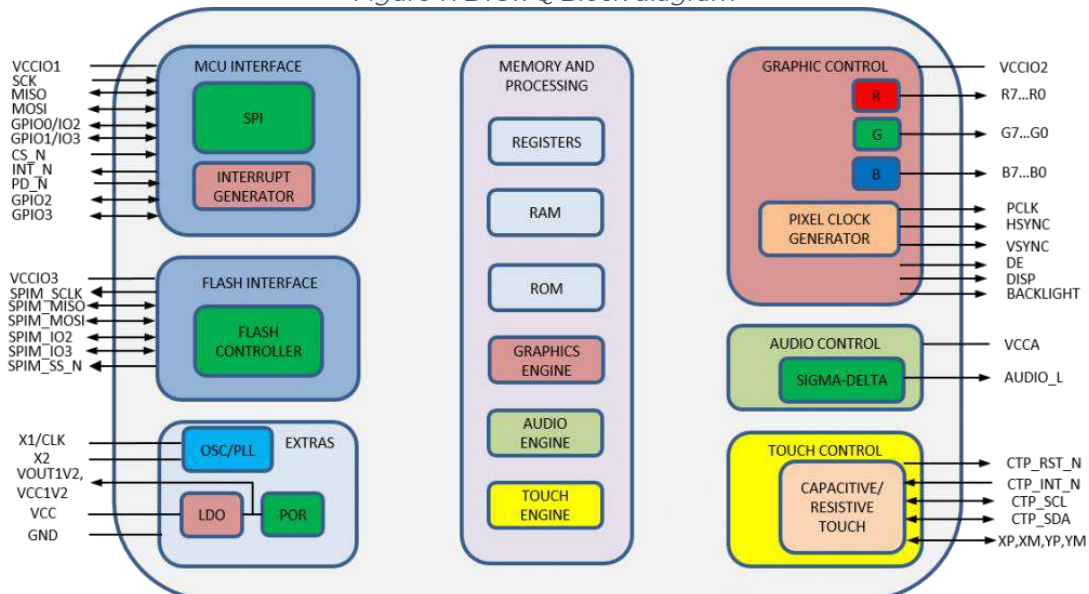
10.3 Host interface SPI mode 0

Figure 8. SPI timing diagram

The meanings of the timings in the Figure 8 are defined in the table below.

PARAMETER	DESCRIPTION	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		Min	Max	Min	Max	Min	Max	
T_{sclk}	SPI clock period	33.3	-	33.3	-	33.3	-	
T_{sclkl}	SPI clock low duration	13	-	13	-	13	-	
T_{sclkh}	SPI clock high duration	13	-	13	-	13	-	
T_{sac}	SPI access time	4	-	3.5	-	3	-	
T_{isu}	Input Setup	4	-	3.5	-	3	-	ns
T_{ih}	Input Hold	0	-	0	-	0	-	
T_{zo}	Output enable delay	-	16	-	13	11	-	
T_{oz}	Output disable delay	-	13	-	11	10	-	
T_{od}	Output data delay	-	15	-	12	11	-	
T_{csnh}	CSN hold time	0	-	0	-	0	-	

For more information about BT817Q controller please go to official BT81x website.
*https://brtchip.com/product/bt817/*

10.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. **REG_PWM_HZ** specifies the PWM output frequency. **REG_PWM_DUTY** specifies the duty cycle.

Refer to BT817Q datasheet for more information.

Figure 9. Backlight driver block diagram
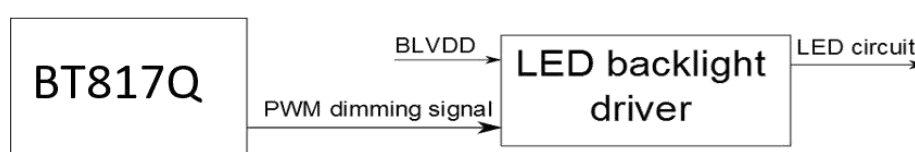
The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED lifetime, as LED current peaks are reduced significantly.

11. 256Mb NOR FLASH MEMORY

The Riverdi EVE4 3.5" series modules are built with a 256Mb NOR flash memory chip. Graphics assets such as fonts, audio, and images can be stored in the flash memory. Up to 410 full resolution (320 * 240 pixels, JPG) images can be stored. If you need to change the memory size, please contact: contact@riverdi.com

There is an additional port P3 for programming the flash memory directly from an external source. This port is designed to be used during production if the customer wants to order pre-programmed EVE4 boards with graphic content of their own choice.

Cable TC2050-IDC-NL is compatible with P3 programming port.
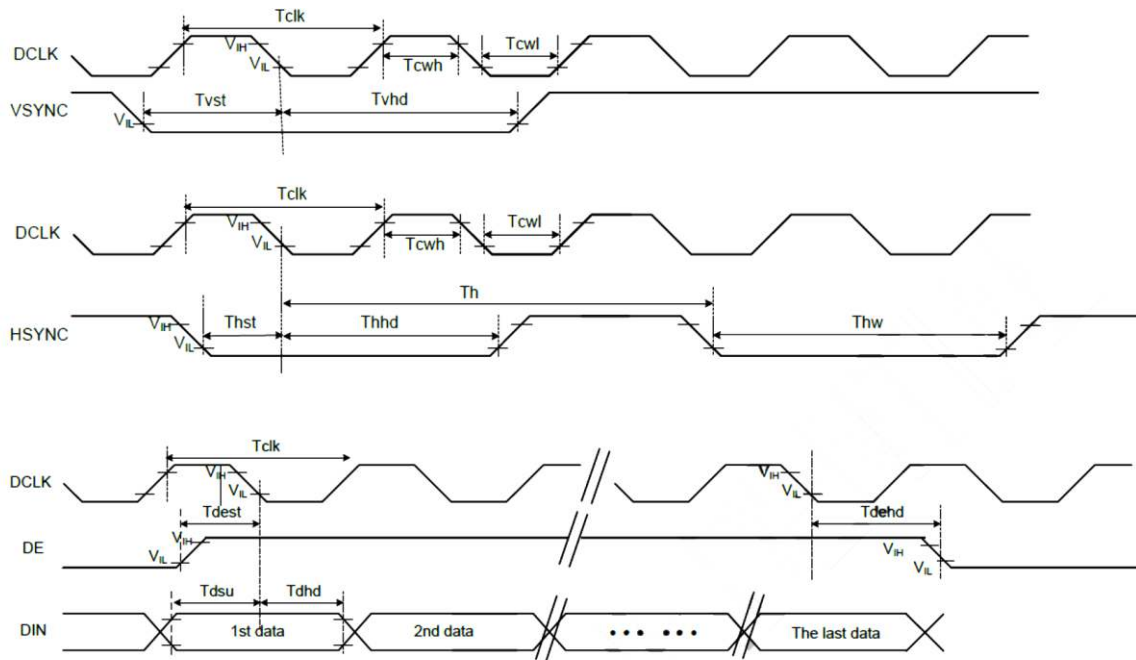
12. TIMING CHARACTERISTICS

12.1 Timing diagram and input setup timing setting

12.1.1 Parallel 24-bit RGB timing table

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
DCLK Frequency		F_{clk}	5	6	8	MHz	
DCLK Period		T_{clk}	125	167	200	ns	
HSYNC	Period Time	T_h	325	371	438	DCLK	
	Display Period	T_{hdisp}		320			
	Back Porch	T_{hbp}	3	43	43		SYNC mode back porch control by H_BLANKING [7:0] setting Thbp= H_BLANKING [7:0]
	Front Porch	T_{hfp}	2	8	75		
	Pulse Width	T_{hw}	2	4	43		
VSYNC	Period Time	T_v	244	260	289	HSYNC	
	Display Period	T_{vdisp}		240			
	Back Porch	T_{vbp}	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING [7:0] setting Tvbp= V_BLANKING [7:0]
	Front Porch	T_{vfp}	2	8	37		
	Pulse Width	T_{vw}	2	4	12		

12.2 System Bus Timing for RGB Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLK Pulse Duty	T_{clk}	40	50	60	%
HSYNC Width	T_{hw}	2	-	-	DCLK
HSYNC Period	T_h	55	60	65	CLK
VSYNC Setup Time	T_{vst}	12	-	-	ns
VSYNC Hold Time	T_{vhd}	12	-	-	
HSYNC Setup Time	T_{hst}	12	-	-	
HSYNC Hold Time	T_{hhd}	12	-	-	
Data Setup Time	T_{dsu}	12	-	-	
Data Hold Time	T_{dhd}	12	-	-	
DE Setup Time	T_{dest}	12	-	-	
DE Hold Time	T_{dehd}	12	-	-	

13. MODULE INITIALIZATION

1. Initialization data, timings and example codes are available on the Riverdi GitHub, at address: https://github.com/riverdi/riverdi-eve

2. REGISTER VALUES:

REGISTER NAME	REGISTER VALUE (DEC.)
REG_HSIZE	320
REG_VSIZE	240
REG_HCYCLE	371
REG_HOFFSET	43
REG_HSYNC0	0
REG_HSYNC1	4
REG_VCYCLE	260
REG_VOFFSET	12
REG_VSYNC0	0
REG_VSYNC1	4
REG_PCLK	1
REG_SWIZZLE	0
REG_PCLK_POL	1
REG_CSPREAD	0
REG_DITHER	0
REG_PCLK_FREQ	34 (0x22)
REG_PCLK_2X	0

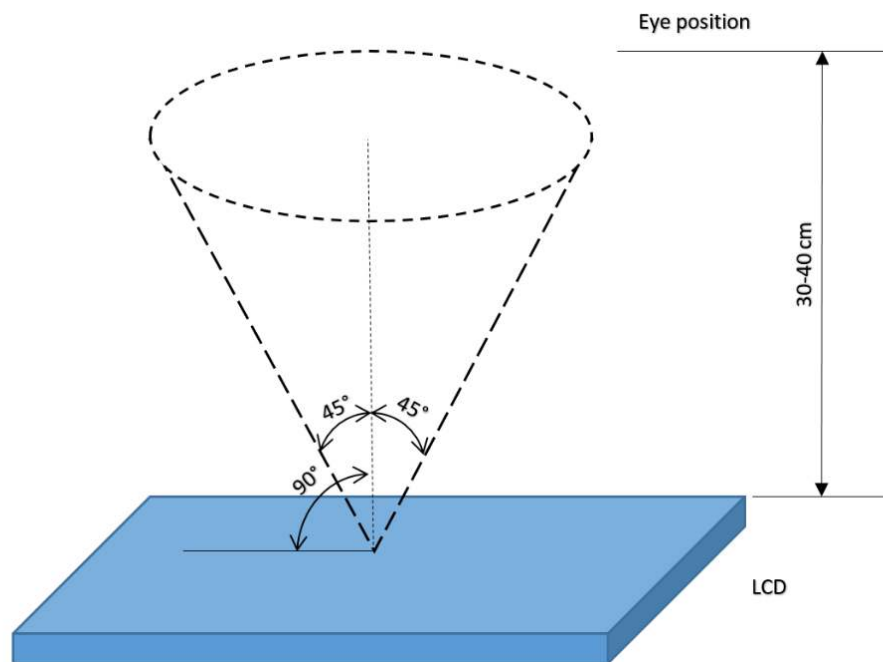## 14. INSPECTION

Standard acceptance/rejection criteria for TFT module

14.1 Inspection condition

Ambient conditions:

- Temperature: 25 ± 2°C
- Humidity: (60 ± 10) %RH
- Illumination: Single fluorescent lamp non-directive (300 to 700 lux)

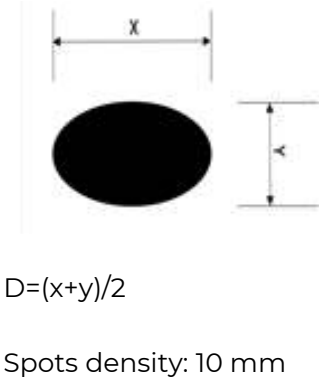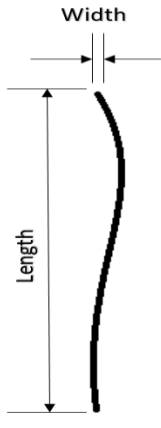Viewing distance: 35 ± 5cm between inspector bare eye and LCD.

Viewing Angle: U/D: 45°/45°, L/R: 45°/45°

14.2 Inspection standard

ITEM	CRITERION		
Black spots, white spots, light leakage, Foreign Particle (round Type)	D=(x+y)/2 Spots density: 10 mm	3.5" ≤ Size ≤ 5"	
		Average Diameter	Qualified Qty
		D ≤ 0.15 mm	Ignored
		0.15 mm < D ≤ 0.3 mm	N≤3
		0.3mm < D	Not allowed

ITEM		CRITERION		
LCD black spots, white spots, light leakage (line Type)	Spots density: 10 mm	3.5" ≤ Size ≤ 5"		
		Length	Width	Qualified Qty
		-	W ≤ 0.03	Ignored
		L ≤ 3.0	0.03 < W ≤ 0.05	2
		L ≤ 3.0	0.05 < W ≤ 0.1	1
		3.0 < L	0.1 < W	Not allowed

Bright/Dark Dots	3.5" ≤ Size ≤ 5"	
	Item	Qualified Qty
	Bright dots	N ≤ 1
	Dark dots	N ≤ 2
	Total Bright and Dark Dots	N ≤ 3

Clear spots	Size < 5.0"	
	Average Diameter	Qualified Qty
	D < 0.2 mm	Ignored
	0.2 mm < D < 0.3 mm	3
	0.3 mm < D < 0.5 mm	2
	0.5 mm < D	0
	Spots density: 10 mm	

Polarizer bubbles	3.5" ≤ Size ≤ 5"	
	Average Diameter	Qualified Qty
	D ≤ 0.2 mm	Ignored
	0.2 mm < D ≤ 0.3 mm	2
	0.3 mm < D ≤ 0.5mm	1
	0.5 mm < D	0
	Total Q'ty	3

15. RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	NOTE
1	High Temperature Storage	80°C/120 hours	Note 1
2	Low Temperature Storage	-30°C/120 hours	
3	High Temperature Operating	70°C/120 hours	
4	Low Temperature Operating	-20°C/120 hours	
5	High Temperature and High Humidity	Humidity 40℃, 90%RH, 120Hrs	
6	Thermal Cycling Test (No operation)	-20℃ for 30min, 70℃ for 30 min. 100 cycles. Then test at room temperature after 1 hour	Note 2
7	Vibration Test	Frequency: 10 ÷ 55 Hz. Stroke: 1.5 mm. Sweep: 10Hz ÷ 55Hz ÷ 10 Hz. 2 hours for each direction of X, Y, Z (Total 6 hours)	
8	Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Note 1. Sample quantity for each test item is 5 ÷ 10 pcs.
Note 2. Before running cosmetic and function tests, the product must have enough recovery time, at least 2 hours at room temperature.

16.LEGAL INFORMATION

CE marking is usually obligatory only for a complete end product. Riverdi display modules are semi-finished goods which are used as inputs to become part of the finished products. Therefore, Riverdi display modules are not CE marked.

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

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