Universal Instrumentation Amplifier Evaluation Module

This user's guide describes the characteristics, operation, and use of two evaluation modules (EVMs) that are compatible with a variety of instrumentation amplifiers (IAs). The schematics and bills of material (BOM) are identical for both EVMs. The only difference is that one EVM is compatible with devices in VSSOP-8 (DGK) packages, and the other EVM is compatible with devices in SOIC-8 (D) packages. They are designed to evaluate the performance of the devices in both single- and dual-supply configurations. This document includes the schematic, printed circuit board (PCB) layouts, and BOM. Throughout this document the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the Universal IA EVM.

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1 Overview

1.1 Features

These EVMs are intended to provide basic functional evaluation of the amplifiers shown in Table 1 with the pinout shown in Figure 1. The EVMs provide the following features:

- Intuitive evaluation with the silkscreen schematic
- Easy access to nodes with surface-mount test points
- Advanced evaluation with two prototype areas
- Reference voltage source flexibility
- Convenient input and output filtering

1.2 IA Pinout

The EVMs are intended to evaluate IAs that have the pinout shown in Figure 1.

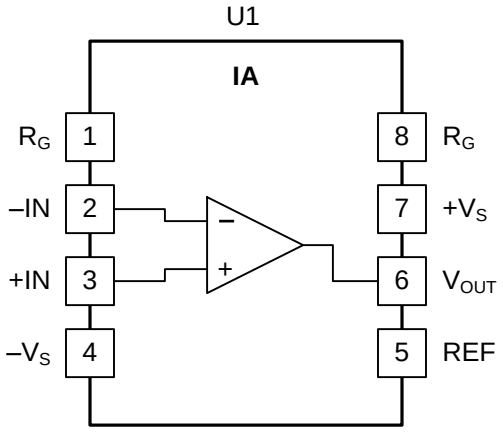

Figure 1. IA Pinout

1.3 Compatible Devices

Devices that are compatible with at least one of the EVMs are shown in Table 1.

Table 1. Compatible Devices

Device	VSSOP-8 (DGK) EVM	SOIC-8 (D) EVM
INA118		X
INA121		X
INA122		X
INA126	X	X
INA128		X
INA129		X
INA141		X
INA155	X	X
INA156	X	
INA188		X
INA333	X	

2 PCB Layout

The schematic and component sides of the VSSOP-8 EVM are shown in Figure 2 and Figure 3, respectively.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing PCBs.

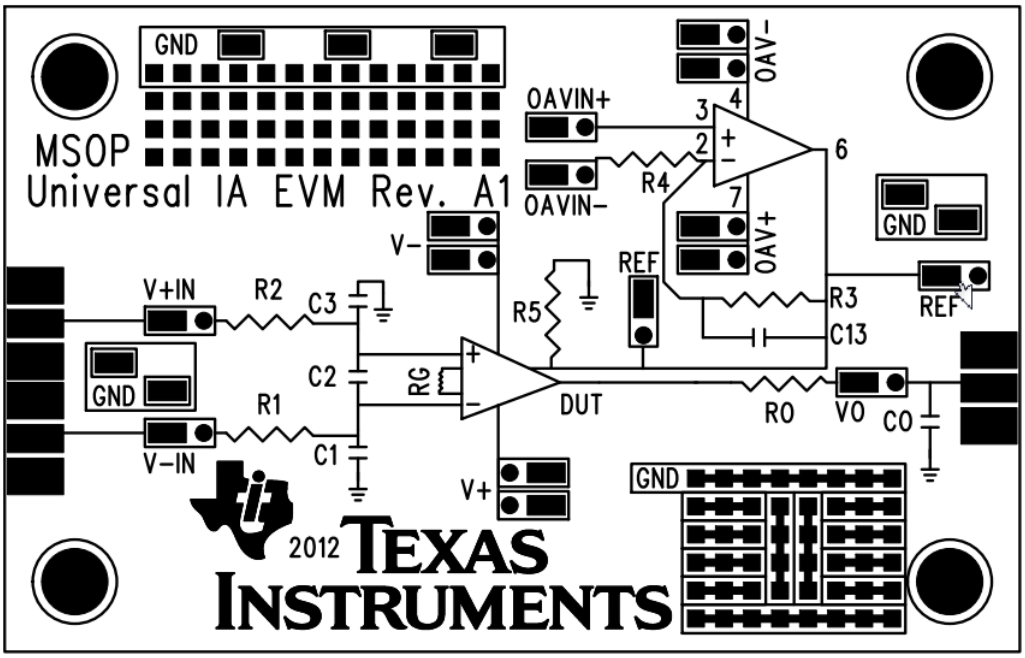

Figure 2. Universal IA EVM Schematic Side (VSSOP-8)

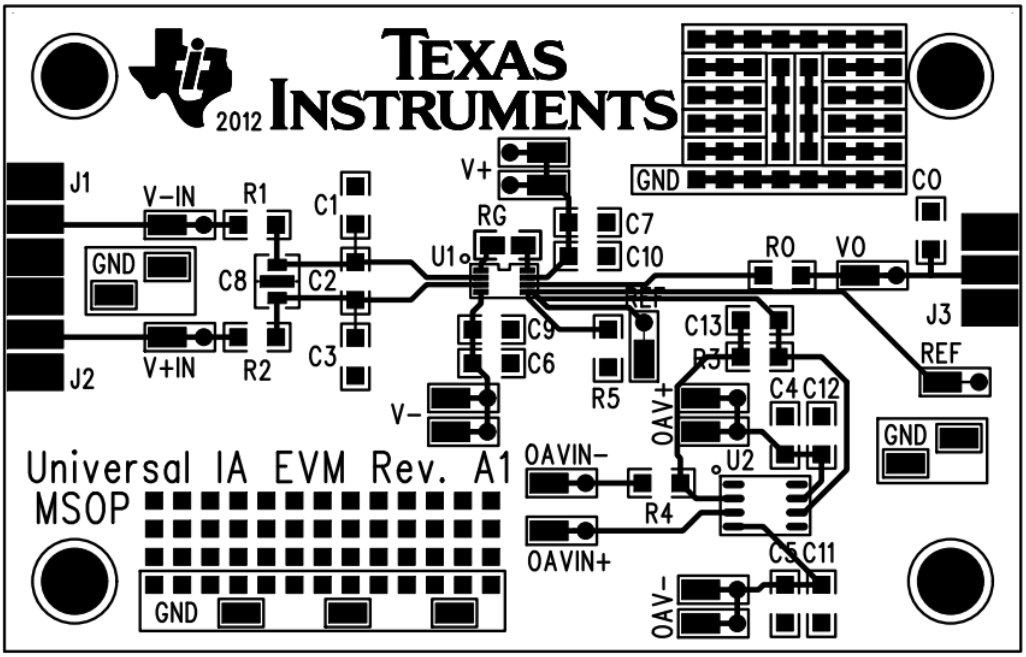

Figure 3. Universal IA EVM Component Side (VSSOP-8)

The schematic and component sides of the SOIC-8 EVM are shown in Figure 4 and Figure 5, respectively.

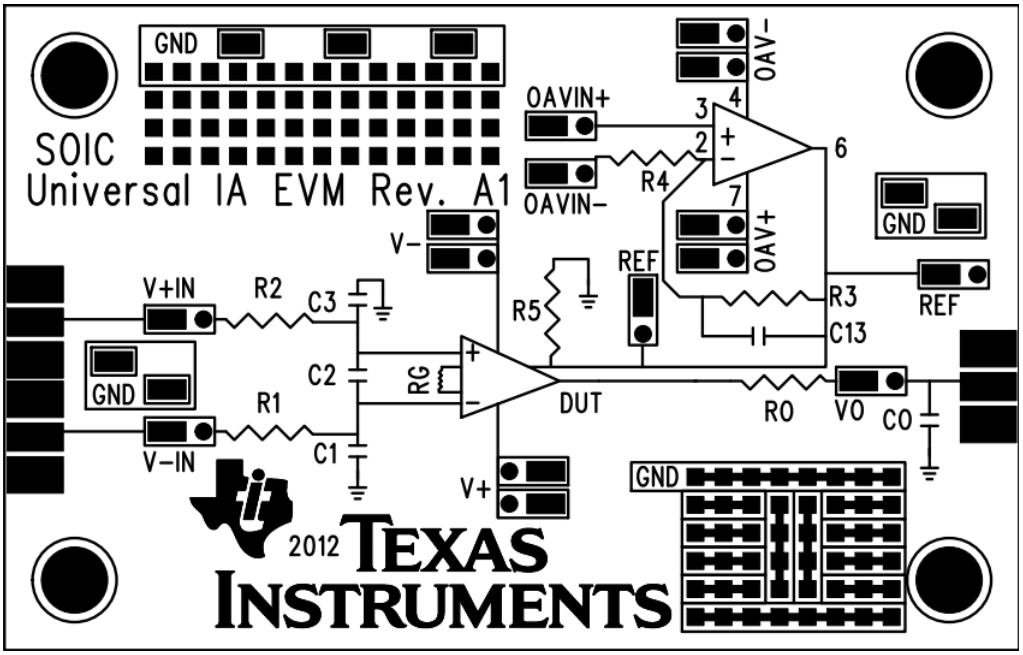

Figure 4. Universal IA EVM Schematic Side (SOIC-8)

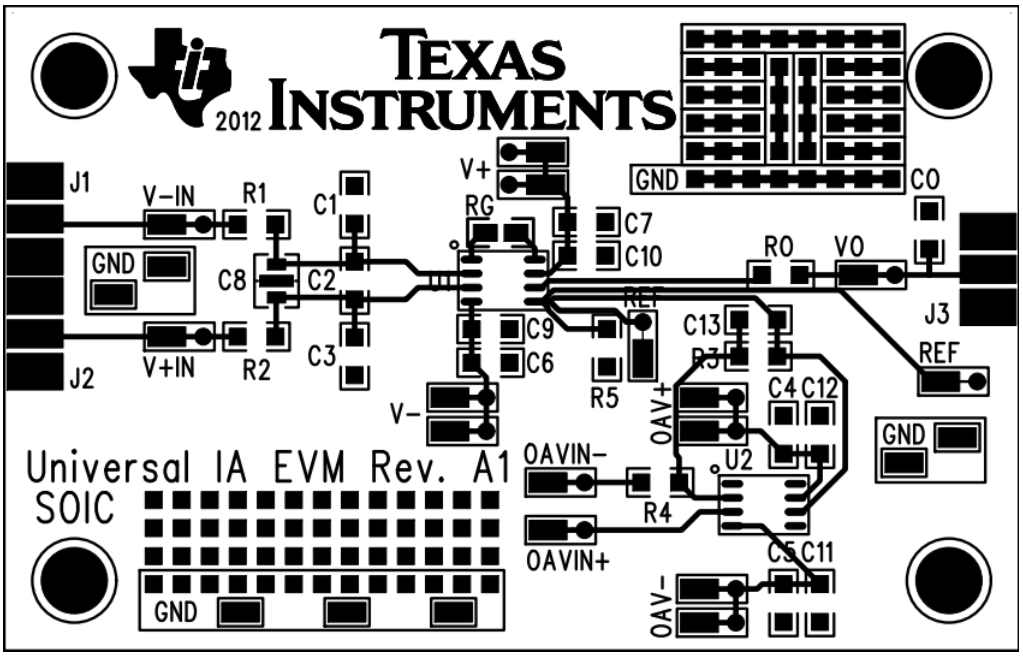

Figure 5. Universal IA EVM Component Side (SOIC-8)

3 Schematic

Figure 6 shows the schematic for the PCB.

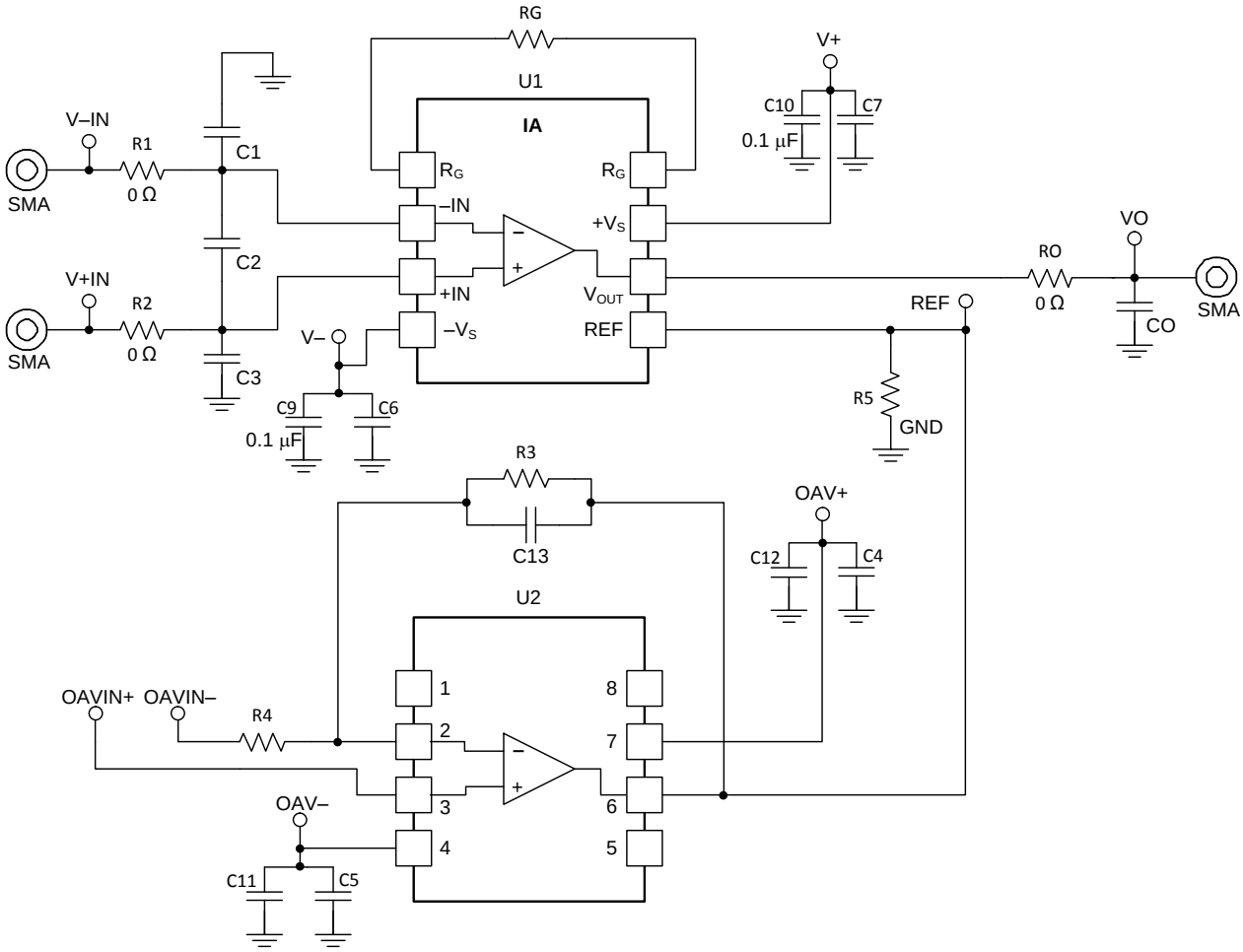

Figure 6. Universal IA EVM Schematic

4 EVM Components

4.1 Power

Power is applied to the device with test points V+ and V–. For the unpopulated device (U2), power is applied using test points OAV+ and OAV–.

4.2 Inputs

Inputs are applied to the device using test points V+IN and V–IN. Alternately, they can be applied by populating the input SMA connectors (J1 and J2). The inputs for U2 are applied through test points OAVIN+ and OAVIN–.

4.2.1 Input Filtering

R1, R2, and C1 through C3 provide the ability to apply common-mode and differential-mode filtering to the inputs. The cutoff frequencies for the filters are shown in Equation 1 and Equation 2. For best performance, make C2 approximately ten times larger than C1 and C3.. These calculations presume R1 = R2 and C1 = C3.

Common-mode cutoff frequency:

$$f_{c\text{-}cm} = \frac{1}{2\pi \times R1 \times C1} \tag{1}$$

Differential-mode cutoff frequency:

$$f_{c\text{-}dm} = \frac{1}{2\pi (R1 + R2)\left(C2 + \frac{C1}{2}\right)} \tag{2}$$

4.3 Output

Access the output of the device with test point VO or by by populating the output SMA connector (J3).

4.3.1 Output Filtering

RO and CO provide the ability to apply a single-pole RC output filter. The cutoff frequency of the output filter is calculated as shown in Equation 3:

$$f_{c\text{-}o} = \frac{1}{2\pi \times RO \times CO} \tag{3}$$

4.4 Reference

There are multiple methods of applying a reference voltage to the device. A straightforward approach is to apply a voltage to the REF test point with U2 unpopulated. If a buffered voltage is desired, U2 can be populated with an operational amplifier in an appropriate SOIC-8 package and pinout. If the reference voltage is GND, either R5 can be populated with a 0-Ω resistor, or the REF test point can be connected to GND.

4.5 Prototype Area

Two prototype areas are provided for flexible evaluation. They can be used, for example, to prototype a voltage divider for a buffered reference voltage, or to supply a direct reference voltage with a device such as the REF3225.

4.6 Miscellaneous

C6, C7, C9, and C10 are the supply bypass capacitors for the device. C9 and C10 are prepopulated with 0.1 µF capacitors that usually provide adequate power supply bypassing for U1. Refer to the instrumentation amplifier data sheet for further information. Similarly, C4, C5, C11, and C12 can be populated to provide supply bypassing for U2. Refer to the buffer amplifier data sheet for further information. C8 can be used with an X2Y® capacitor.

5 Quick Start

The procedures presented in this section describe how to quickly set up and use the Universal IA EVM for evaluation in dual-supply and single-supply configurations.

5.1 Dual-Supply Configuration

Figure 7 shows an example of how to set up the EVM for dual-supply operation.

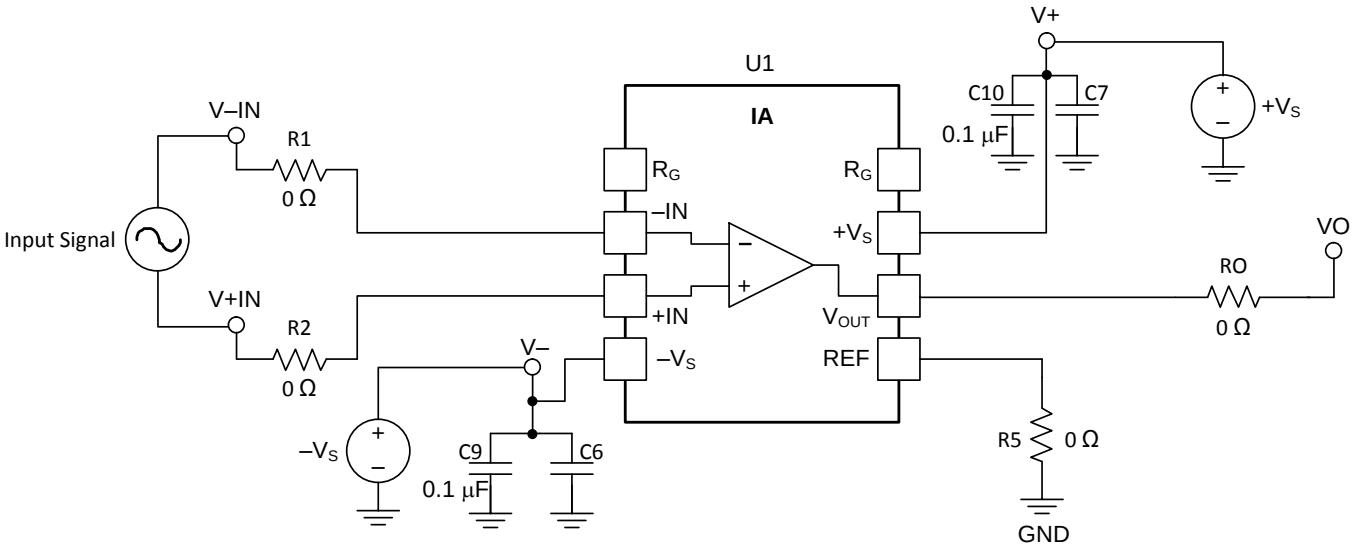

Figure 7. Dual-Supply Configuration

The following connections were made:

1. $+V_S$ to V+ test point
2. $-V_S$ to V– test point
3. Install 0-Ω resistor as R5 (or connect REF test point to GND)
4. Differential input signal connect to V–IN and V+IN test points
5. Observe output at VO test point

Note that C9 and C10 are prepopulated with 0.1-µF power-supply decoupling capacitors. Refer to the device data sheet for additional power-supply decoupling information.

5.2 Single-Supply Configuration

5.2.1 Direct-Reference Connection

Figure 8 shows an example of how to set up the EVM for single-supply operation with a direct voltage connection to the reference (REF pin).

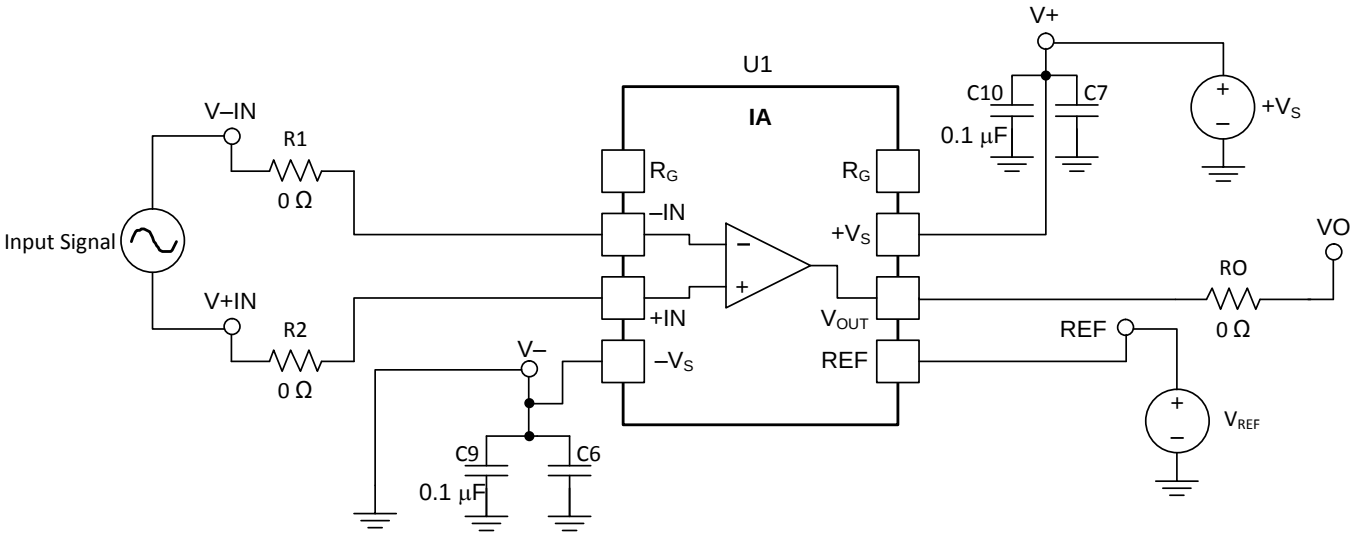

Figure 8. Single-Supply Configuration, Direct REF Connection

The following connections were made:

1. $+V_S$ to V+ test point
2. GND to V– test point
3. Reference voltage to REF test point
4. Differential input signal to V–IN and V+IN test points
5. Observe output at VO test point

Note that C9 and C10 are prepopulated with 0.1-µF power-supply decoupling capacitors. It is not required to remove C9 for proper single-supply operation. Refer to the device data sheet for additional power-supply decoupling information.

5.2.2 Buffered-Reference Voltage Connection

A buffered-reference configuration is useful when the source impedance is high (for example, a voltage divider). Buffering a high-impedance source with an operational amplifier provides a low-impedance source and preserves common-mode rejection. Figure 9 shows an example of how to set up the EVM for single-supply operation with a buffered-reference voltage connection. Depending on the application, desirable single-supply buffer operational amplifiers include the OPA330, OPA376, and OPA378. The OPA277 is a good choice for high-voltage applications.

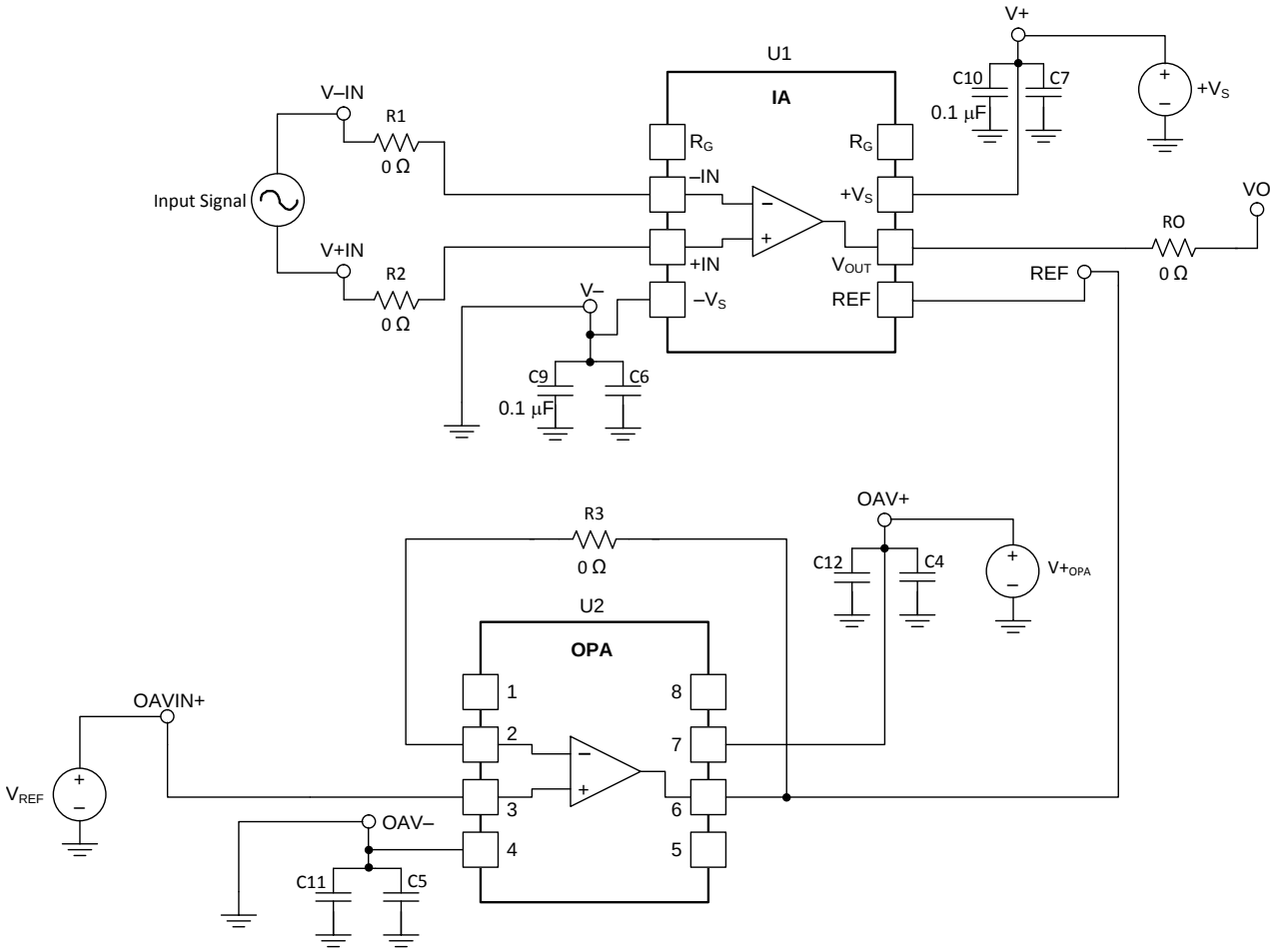

Figure 9. Single-Supply Configuration, Buffered REF Connection

The following connections were made:

1. $+V_S$ to V+ test point
2. $V+_{OPA}$ to OAV+ test point
3. GND to V– and OAV– test points
4. V_{REF} to OAVIN+ test point
5. Ensure that R5 is not populated
6. Populate R3 with a 0-Ω resistor
7. Populate C4, C5, C11, and C12 with appropriate bypass capacitors for buffer amplifier
8. Differential input signal to V–IN and V+IN test points
9. Observe output at VO test point

Note that C9 and C10 are prepopulated with 0.1-µF power-supply decoupling capacitors. It is not required to remove C9 for proper single-supply operation. Refer to the device data sheet for additional power-supply decoupling information.

6 Bill of Materials

Table 2 provides the parts list for the EVM.

Table 2. Universal IA EVM Bill of Materials

Count	RefDes	Value	Description	Part Number	Manufacturer
3	R1, R2, RO	0 Ω	Resistor, 1/4W, 1206	RMCF1206ZT0R00	Stackpole Electronics
2	C9, C10	0.1 µF	Ceramic bypass capacitors, 50 V, X7R, 20%, 1206	12065C104MAT2A	AVX Corporation
1	RG	—	Resistor, 1/4W, 0402-1206	—	—
1	C8	—	Capacitor, X2Y, 1206	—	—
8	N/A	N/A	Bumpon, cylindrical, 0.375 X 0.135, Black	SJ61A8	3M
44	Various	N/A	Surface Mount Test Points	5015	Keystone Electronics

7 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instruments' integrated circuits and support tools for the EVM. This user's guide is available from the TI web site under literature number ***SBOU122***. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site, or call the Texas Instruments' Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 3. Related Documentation

Document	Literature Number
INA118 Product Data Sheet	SBOS027
INA121 Product Data Sheet	SBOS078
INA122 Product Data Sheet	SBOS069
INA126 Product Data Sheet	SBOS062
INA128 Product Data Sheet	SBOS051
INA129 Product Data Sheet	SBOS051
INA141 Product Data Sheet	SBOS052
INA155 Product Data Sheet	SBOS114
INA156 Product Data Sheet	SBOS119
INA188 Product Data Sheet	SBOS632
INA333 Product Data Sheet	SBOS445
OPA376 Product Data Sheet	SBOS406
OPA277 Product Data Sheet	SBOS079
OPA330 Product Data Sheet	SBOS432
OPA378 Product Data Sheet	SBOS417
REF3225 Product Data Sheet	SBVS058

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (September 2015) to B Revision **Page**

- Added two rows to Table 2 for RG and C8 10

Changes from Original (September 2013) to A Revision **Page**

- Changed package name from MSOP to VSSOP to matching industry standard term 1
- Changed package name from SO to SOIC to matching industry standard term 1
- Added INA188 device to Table 1 2
- Added INA188 device to Table 3 10

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265