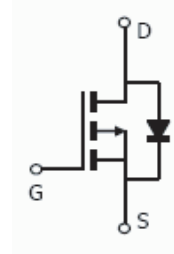


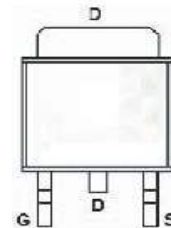
## P-Channel Enhancement Mode Power MOSFET

### Description

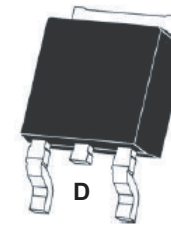
The RM35P30LD uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.



Schematic diagram



Marking and pin assignment



G S  
TO-252-2L top view

### General Features

- $V_{DS} = -30V, I_D = -35A$   
 $R_{DS(ON)} < 20m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 32m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low  $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Halogen-free

**100% UIS TESTED!**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
35P30	RM35P30LD	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-35	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	-22	A
Pulsed Drain Current	$I_{DM}$	-70	A
Maximum Power Dissipation	$P_D$	34.7	W
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	72.2	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3.6	$^\circ C/W$
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## Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

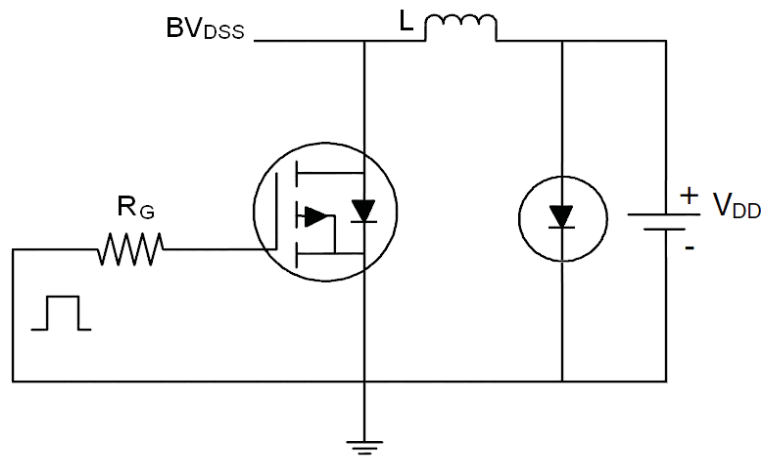
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	-	-	20	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A	-	-	32	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-10A	-	5	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, F=1.0MHz	-	1345	-	PF
Output Capacitance	C <sub>OSS</sub>		-	194	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	158	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-15V, I <sub>D</sub> =-15A V <sub>GS</sub> =-10V, R <sub>GEN</sub> = 3.3 Ω	-	4.4	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	11.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	34	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	18	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-15A, V <sub>GS</sub> =-4.5V	-	12.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-35	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = -15A di/dt = 100A/μs (Note 3)	-	12.4	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	5	-	nC

### Notes:

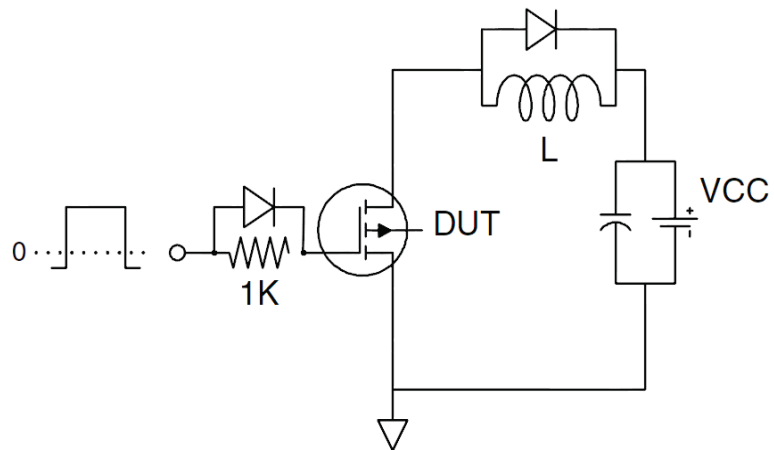
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E<sub>AS</sub> condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=-25V, V<sub>G</sub>=-20V, L=0.5mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=29A

## Test Circuit

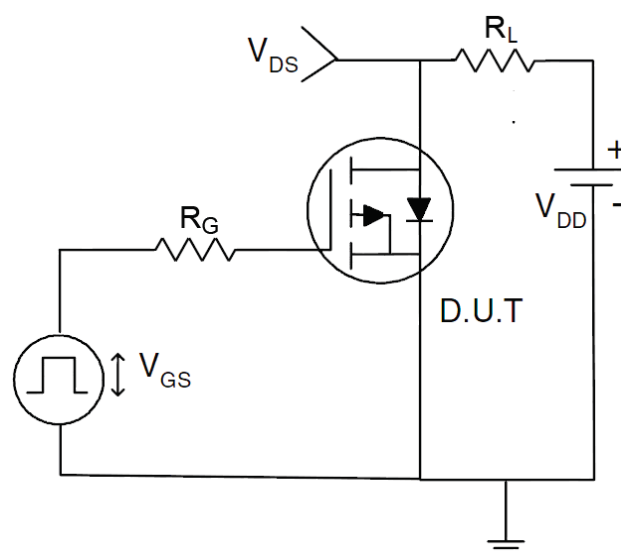
### 1) $E_{AS}$ Test Circuit



### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit



# RATING AND CHARACTERISTICS CURVES (RM35P30LD)

C

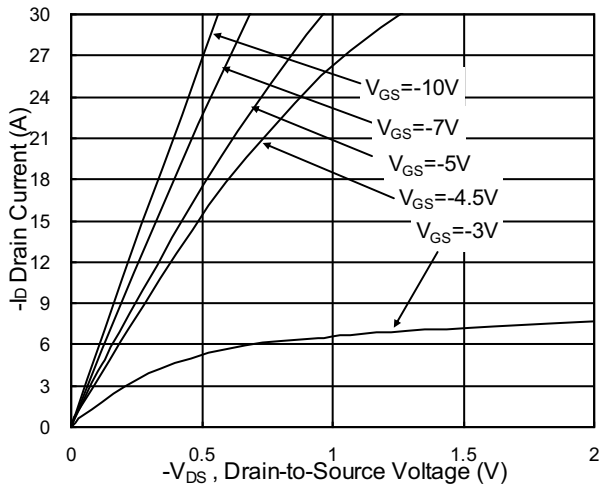


Fig.1 Typical Output Characteristics

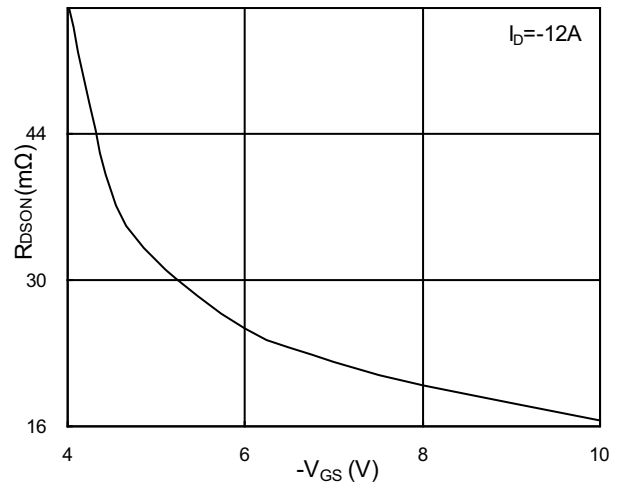


Fig.2 On-Resistance v.s Gate-Source

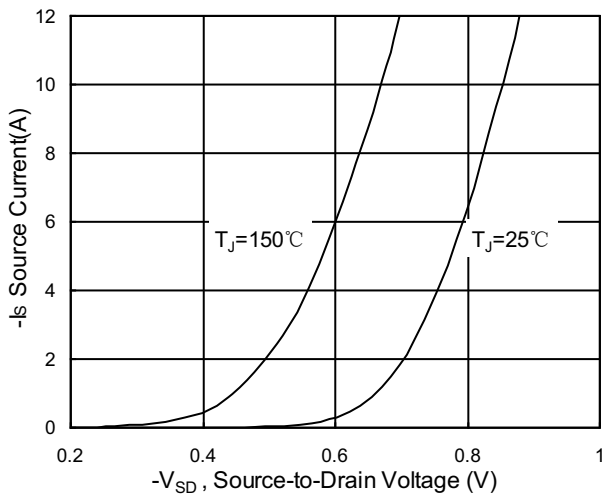


Fig.3 Forward Characteristics of Reverse

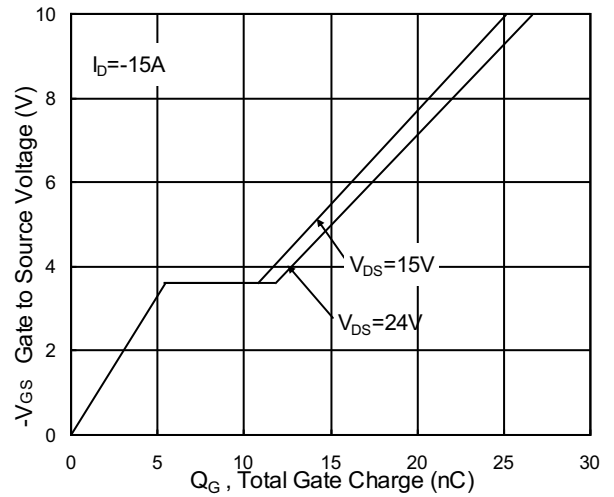


Fig.4 Gate-Charge Characteristics

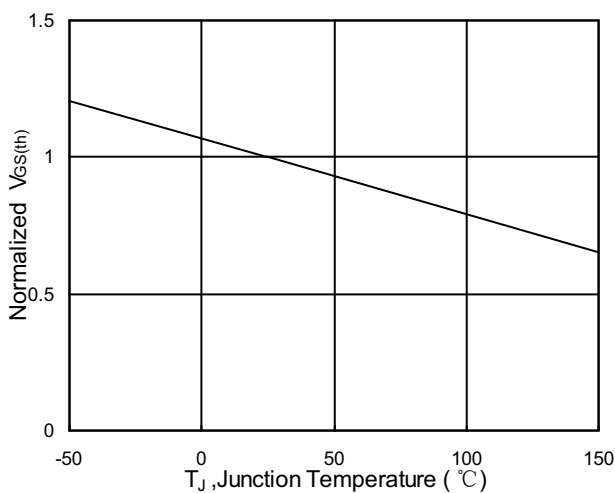


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$

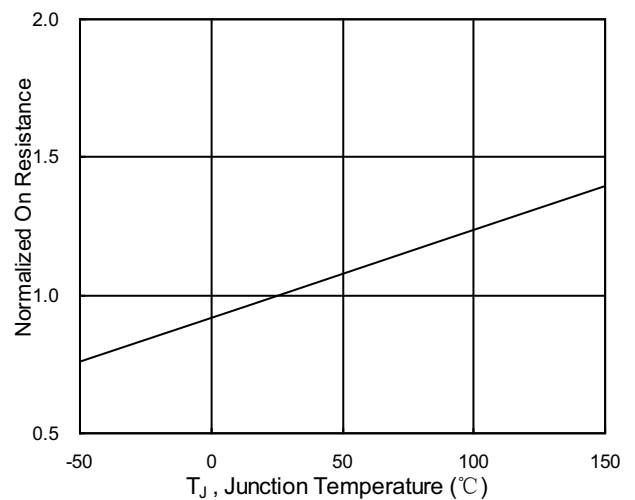


Fig.6 Normalized  $R_{bSON}$  v.s  $T_J$

# RATING AND CHARACTERISTICS CURVES (RM35P30LD)

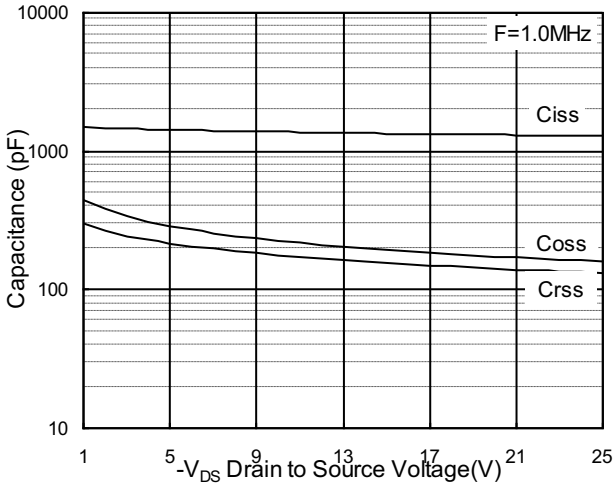


Fig.7 Capacitance

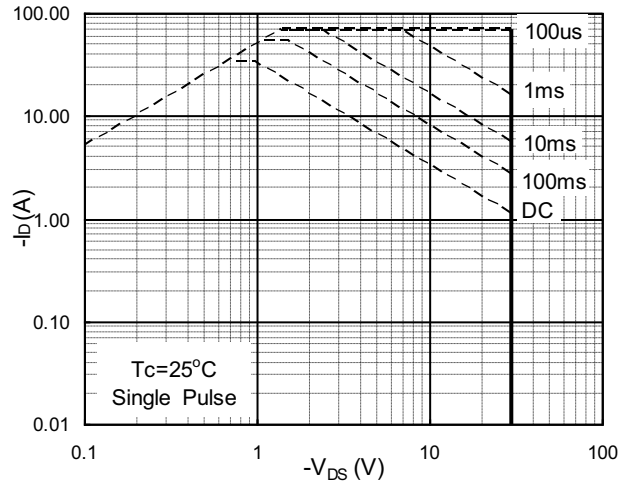


Fig.8 Safe Operating Area

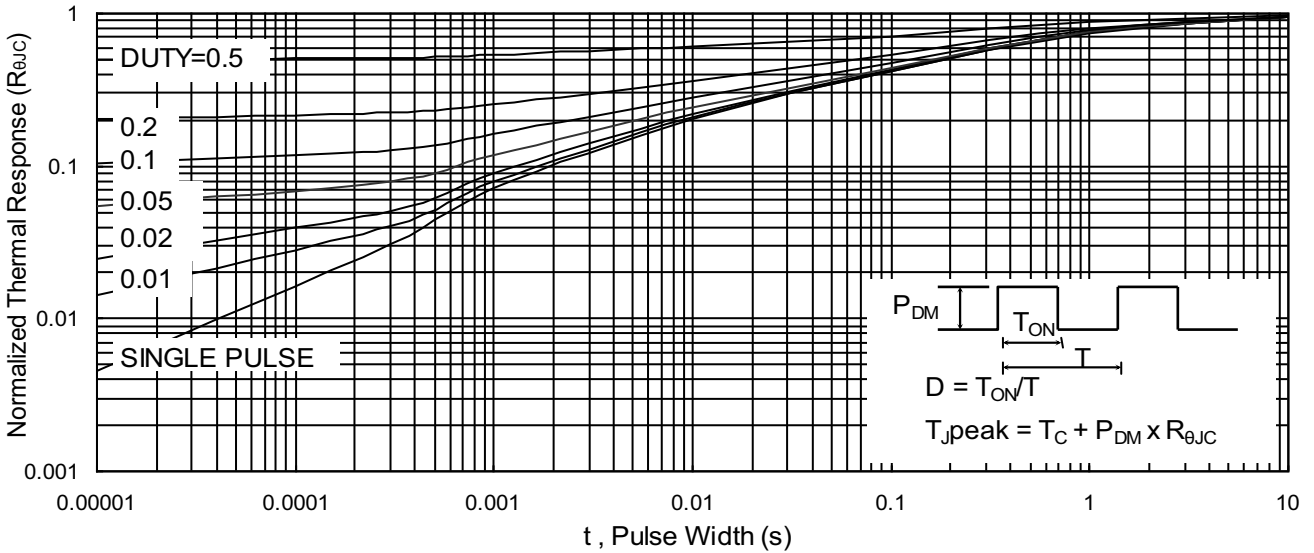


Fig.9 Normalized Maximum Transient Thermal Impedance

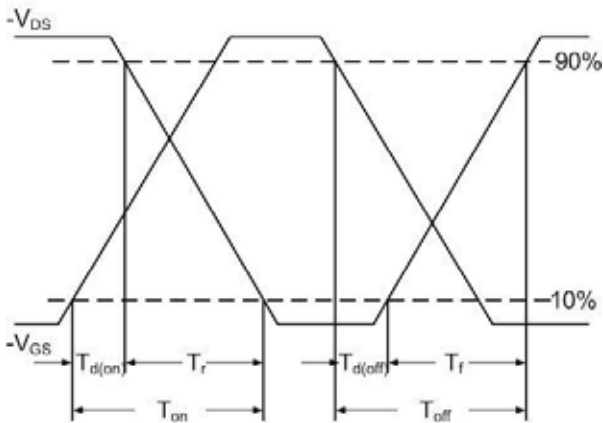


Fig.10 Switching Time Waveform

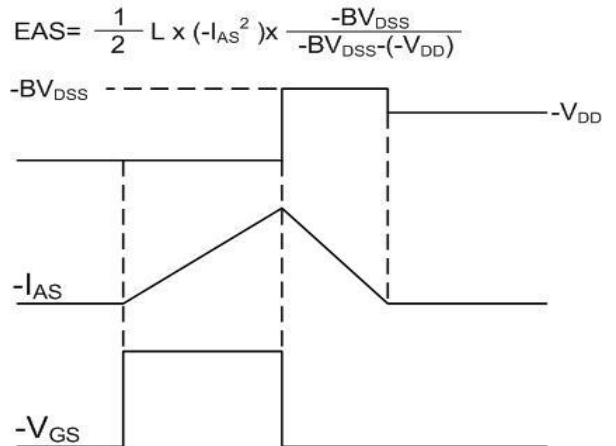
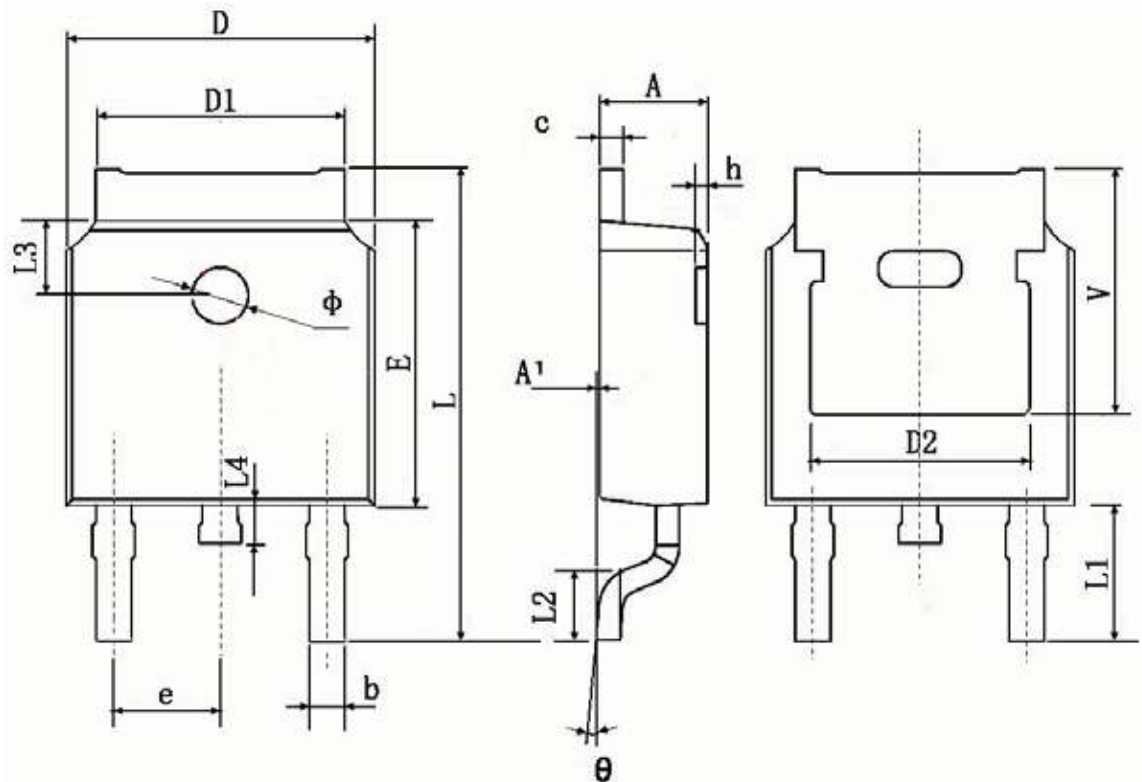


Fig.11 Unclamped Inductive Switching Waveform

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
$\Phi$	1.100	1.300	0.043	0.051
$\theta$	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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