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Evaluating the ADAU1463 and ADAU1467 SigmaDSP Audio Processors

FEATURES

4 analog inputs
8 analog outputs
Stereo S/PDIF input and output
Self boot EEPROM
Headers for interfacing to off board peripherals

EVALUATION KIT CONTENTS

EVAL-ADAU1467Z evaluation board
EVAL-ADUSB2EBZ (USBi) communications adapter
USB cable with Mini-B plug
6 V ac to dc power supply

HARDWARE REQUIRED

PC running Windows XP, Windows Vista, or Windows 7
Analog, stereo audio source with an output cable terminated with a 3.5 mm (1/8 inch) plug (for the analog input)
Headphones, desktop speakers, or audio input with a cable terminated with a 3.5 mm (1/8 inch) plug (for the analog output)
S/PDIF audio source and receiver, each with optical cables terminated with TOSLINK connectors (for digital input/output)

SOFTWARE REQUIRED

SigmaStudio software, available for download from the SigmaStudio product page

DOCUMENTS NEEDED

ADAU1467 data sheet
AD1937 data sheet
AN-1006 Application Note

GENERAL DESCRIPTION

This user guide details the design, setup, and operation of the EVAL-ADAU1467Z evaluation board. This board is suitable for the evaluation of, and software development for, the ADAU1467 and ADAU1463 SigmaDSP® processors. Note that the ADAU1467 and the ADAU1463 are functionally identical; however, the ADAU1467 has more program and data memory than the ADAU1463. When using this evaluation board to evaluate the ADAU1463, select the ADAU1463 block (see the Setting Up Communications in SigmaStudio section) rather than the ADAU1467, as shown in Figure 16. Performing this action informs the compiler to limit the amount of memory allocated to match the ADAU1463. All other procedures and instructions in this user guide are identical for the ADAU1463 and ADAU1467.

This evaluation board provides access to the digital serial audio ports of the ADAU1467. Four analog inputs and eight analog outputs are provided by the AD1937 codec included in the evaluation kit. Switches enable the evaluation of alternate features provided by many of the pins with multiplexed functionality, and numerous headers provide access to serial audio ports and the master and slave control ports. These selectable modes and headers make the EVAL-ADAU1467Z well suited to prototyping larger application circuits, as well as initial device evaluation. The ADAU1467 core is programmed using Analog Devices, Inc., SigmaStudio® software, which interfaces to the evaluation board via a USB interface (USBi). The on-board, electronically erasable programmable read only memory (EEPROM) can be programmed for self boot mode. The evaluation board is powered by a 6 V dc supply, which is regulated to the voltages required on the board. The printed circuit board (PCB) is a 4-layer design with a ground plane and a power plane on the inner layers. The evaluation board includes connectors for external analog inputs and outputs and optical Sony/Philips Digital Interface (S/PDIF) interfaces. The master clock is provided by the integrated oscillator circuit and the on-board 12.288 MHz passive crystal.

For full details, see the ADAU1467 and AD1937 data sheets, which must be used in conjunction with this user guide when using the evaluation board.

TABLE OF CONTENTS

REVISION HISTORY

10/2017—Revision 0: Initial Version

EVAL-ADAU1467Z EVALUATION BOARD PHOTOGRAPH

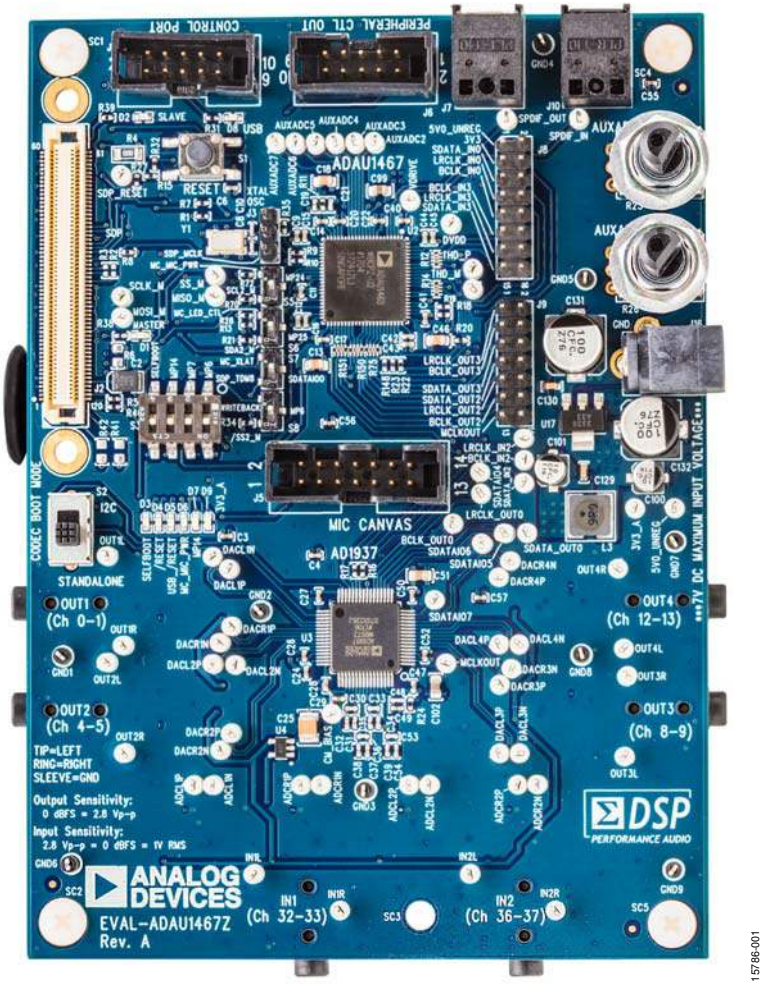


Figure 1.

SETTING UP THE EVALUATION BOARD

Using the EVAL-ADAU1467Z evaluation board requires a PC running Windows® XP or later with a USB interface and an internet connection. The PC communicates with the evaluation board using the included USBi interface. The software tool chain used with the ADAU1467 is SigmaStudio, a fully graphical user interface (GUI)-based programming environment. No DSP programming is required. A full version of SigmaStudio, which includes a library of DSP building blocks and the required USBi drivers, is available for download from the SigmaStudio software page on the Analog Devices website at www.analog.com/SigmaStudio.

INSTALLING THE SigmaStudio SOFTWARE

To download the latest version of SigmaStudio, take the following steps:

1. Go to the SigmaStudio software page on the Analog Devices website, and select the latest version of the SigmaStudio software from the **Downloads and Related Software** section.
2. Determine whether the software must be installed on a 32-bit or 64-bit version of Windows, and locate the latest release version of SigmaStudio as appropriate.
3. Download the installer and execute the executable. Follow the prompts, and accept the license agreement to install the software.

INSTALLING THE USBi (EVAL-ADUSB2EBZ) DRIVERS

SigmaStudio must be installed to use the USB interface (USBi). After the SigmaStudio installation is complete, take the following steps:

1. Connect the USBi to an available USB 2.0 port using the USB cable included in the evaluation board kit. Note that the USBi does not function properly with a USB 3.0 port.
2. Install the driver software (see the Using Windows XP section or the Using Windows 7 or Windows Vista section for more information).

Using Windows XP

*Figure 2. **Found New Hardware** Notification*

After connecting the USBi to the USB 2.0 port, Windows recognizes the device (see Figure 2) and prompts the user to install the drivers. To install these drivers, take the following steps:

1. From the **Found New Hardware Wizard** window, select the installation from a list or from a specific location using the advanced option, and click **Next** (see Figure 3).

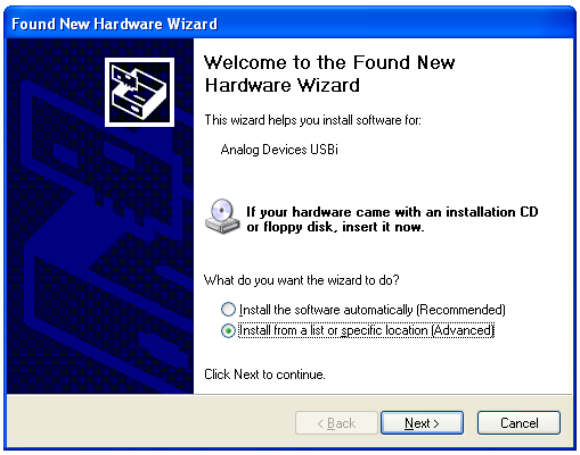


*Figure 3. **Found New Hardware Wizard** Installation*

2. Click **Search for the best driver in these locations**, select **Include this location in the search**, and click **Browse** to find the USB drivers subdirectory within the SigmaStudio directory (see Figure 4).

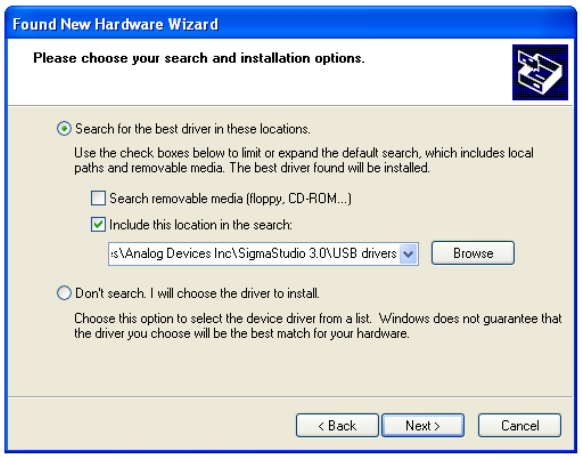


*Figure 4. **Found New Hardware Wizard**—Search and Installation Options*

3. When the warning about Windows logo testing appears, click **Continue Anyway** (see Figure 5).

*Figure 5. **Hardware Installation**—Windows Logo Testing Warning*

The USBi drivers are now installed. Leave the USBi connected to the PC.

Using Windows 7 or Windows Vista

After connecting the USBi to the USB 2.0 port, Windows 7 or Windows Vista recognizes the device and installs the drivers automatically (see Figure 6). After the installation is complete, leave the USBi connected to the PC.

Figure 6. USBi Driver Installed Correctly

Confirming Proper Installation of the USBi Drivers

To confirm that the USBi drivers are installed properly, take the following steps:

1. With the USBi still connected to the USB 2.0 port of the computer, check that both the yellow I²C LED and the red power indicator LED are illuminated (see Figure 7).

Figure 7. State of the USBi Status LEDs After Driver Installation

2. In the Windows **Device Manager**, under the **Universal Serial Bus controllers** section, check that **Analog Devices USBi (programmed)** is displayed (see Figure 8).

Figure 8. Confirming Driver Installation Using the Device Manager

DISABLING THE SELF BOOT SWITCH

When setting up the EVAL-ADAU1467Z evaluation board, ensure that the SELFBOOT switch is in the off position. SELFBOOT is the first switch of the four position, dual inline package (DIP) switches, S3. The off position is toward the bottom of the board, away from the silkscreen label, SELFBOOT.

The default position of this switch is the off (disabled) position, which prevents the ADAU1467 from executing a self boot operation at power-up. When the switch is in the on position, the LED D3 is illuminated, and a self boot operation is executed, causing the ADAU1467 to attempt to load code from the EEPROM (U10) when it powers up or comes out of reset.

POWERING UP THE EVALUATION BOARD

Power is supplied to the evaluation board using a dc power supply with a female positive center plug. The plug has a 2.1 mm inner diameter, a 5.5 mm outer diameter, and a 9.5 mm length (see Figure 9). The output must range between 5 V and 7 V and must be able to source at least 1.5 A of current. Connect the power supply to Connector J4. The unregulated supply powers the operational amplifiers used in the active audio filters for the analog audio inputs and outputs. An on-board linear regulator (U17) generates the 3.3 V dc supply required for the ADAU1467 and AD1937, as well as other supporting ICs. When the power supply is connected properly, LED D9 illuminates.

Figure 9. DC Power Supply Plug and Cable

To power up the evaluation board, take the following steps:

1. Connect the included power supply to the wall outlet (100 V to 240 V, ac 50 Hz to 60 Hz).
2. Connect the female plug of the power supply to the J4 male connector on the EVAL-ADAU1467Z, as shown in Figure 10.

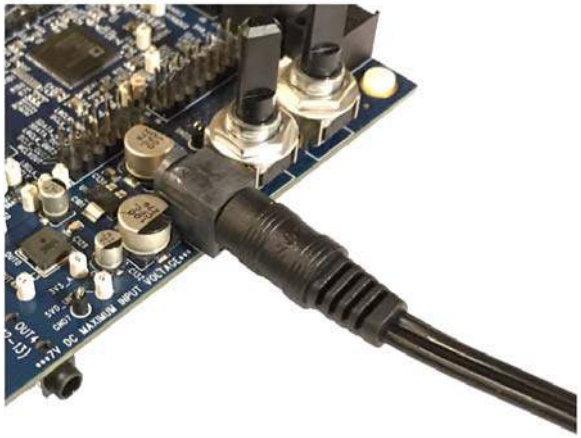


Figure 10. Connecting the Power Supply

3. After the power supply is connected, the D2 status LED (A_3V3) illuminates.
4. Connect the ribbon cable of the USBi to the control port of the EVAL-ADAU1467Z (see Figure 11). The USBi must already be connected to the USB 2.0 port of the computer.

Figure 11. Connecting the USBi to the Serial Peripheral Interface (SPI) Control Port Header

CONNECTING THE AUDIO CABLES

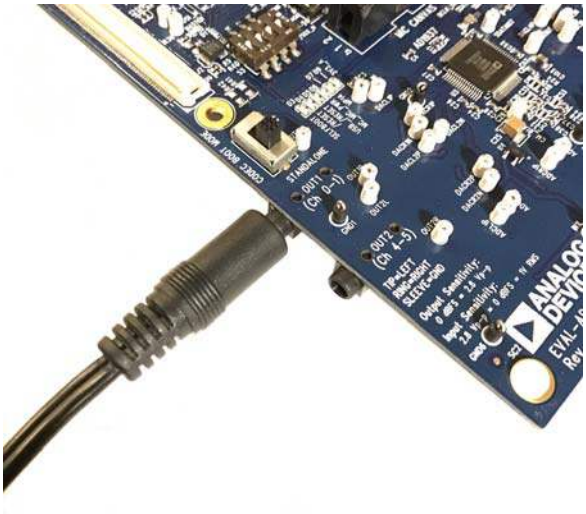
To connect the audio cables to the evaluation board, take the following steps:

1. Connect a stereo audio source to J14 (IN1) with a standard 3.5 mm (1/8 inch) stereo tip, ring, sleeve (TRS) audio cable. The audio signals must be single-ended and line level, with a maximum voltage of 2.8 V p-p. The tip of the plug is the left channel of audio, the ring is the right channel of audio, and the sleeve is the common or ground.
2. Connect headphones or powered speakers to J12 (OUT1).

Figure 12 shows the input source connection. Figure 13 shows the output connection. Figure 14 shows the location of the connectors on the board.

15786-012

Figure 12. Analog Stereo Input Source Connection



15786-013

Figure 13. Analog Stereo Output Connection

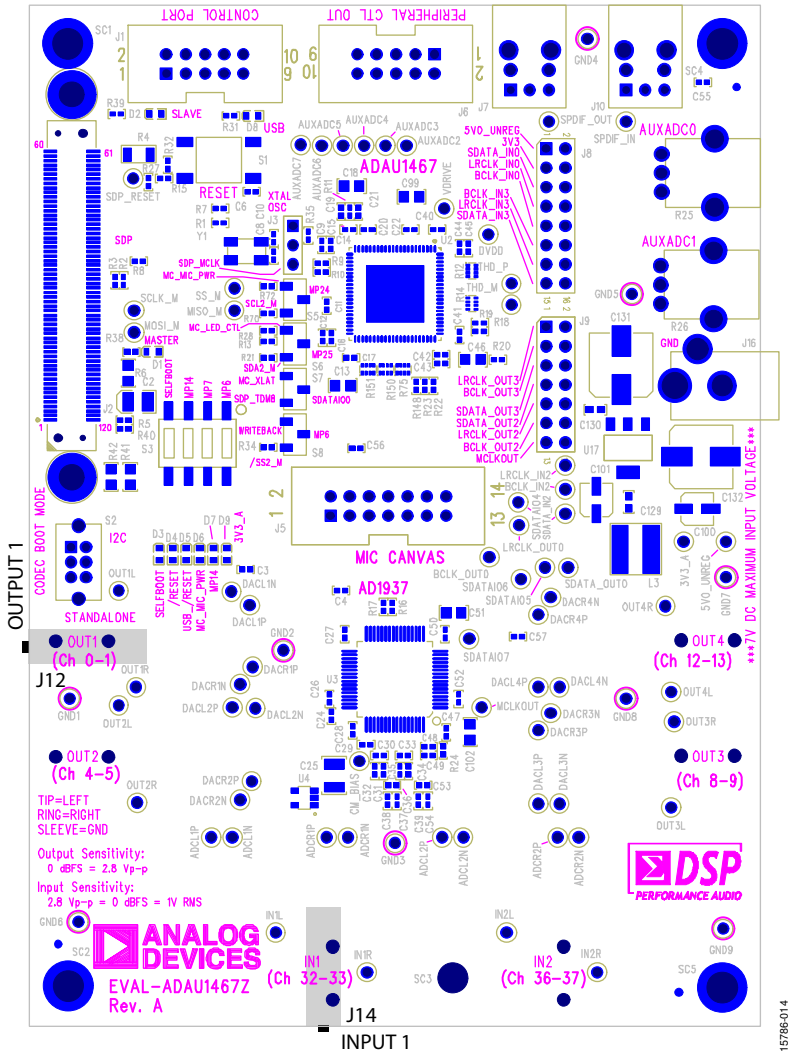


Figure 14. Location of Stereo Output OUT1 (J12) and Stereo Input IN1 (J14)

SETTING UP COMMUNICATIONS IN SigmaStudio

To set up communications in SigmaStudio, take the following steps:

1. Start the SigmaStudio software by double clicking the shortcut on the desktop or by finding and executing the executable file in Windows Explorer.
2. To create a new project, select **New Project** from the **File** menu or press **CTRL + N**. (The default view of the new project is the **Hardware Configuration** tab.)
3. In the **Hardware Configuration** tab, add the appropriate components to the project space by clicking and dragging them from the **Tree ToolBox** on the left of the window to the empty white space located on the right of the window.
   a. Click **USBi** to add a USBi component from the **Communication Channels** subsection of the toolbox (see Figure 15).

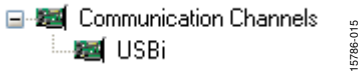


Figure 15. Adding the USBi Communication Channel

   b. Add an ADAU1467 component from the **Processors (ICs/DSPs)** subsection of the toolbox (see Figure 16).

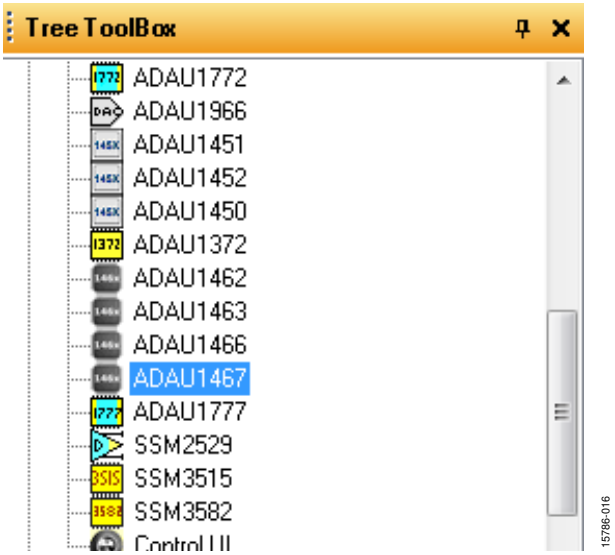


Figure 16. Adding an ADAU1467

4. Ensure that SigmaStudio can detect the USBi on the USB port of the PC as follows:
   a. When SigmaStudio detects the USBi, the background of the **USB** label is green in the **USB Interface** box (see Figure 17).

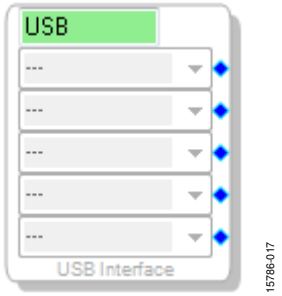


Figure 17. USBi Detected by SigmaStudio

   b. When SigmaStudio cannot detect the USBi on the USB port of the PC, the background of the **USB** label is red (see Figure 18). This error can occur when the USBi is not connected or when the drivers are installed incorrectly.

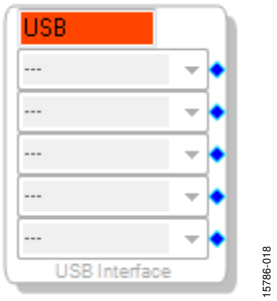


Figure 18. USBi Not Detected by SigmaStudio

   c. To connect the USBi block (USB interface) to the target integrated circuit (IC) block of the ADAU1467, click and drag a line, representing a wire, between the blue pin of the USBi and the green pin of the IC (see Figure 19). This connection allows the USBi to communicate with the ADAU1467. The corresponding dropdown box of the USBi automatically fills with the default mode and channel for that IC. In the case of the ADAU1467, the default communications mode is SPI, the default slave select line is 1, and the default address is 0.

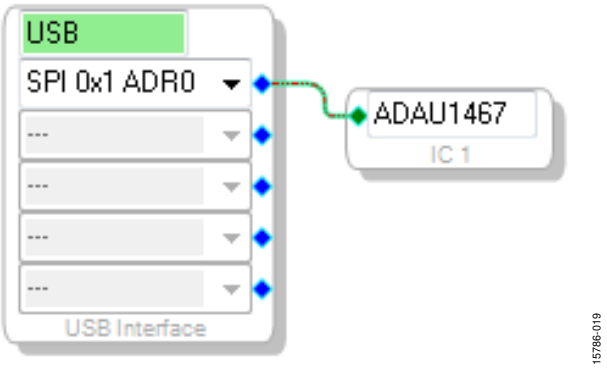


*Figure 19. Connecting the USBi to an ADAU1467 in the **Hardware Configuration** Tab*

CREATING A BASIC SIGNAL FLOW

To create a signal processing flow, take the following steps:

1. Click the **Schematic** tab near the top of the window (see Figure 20).

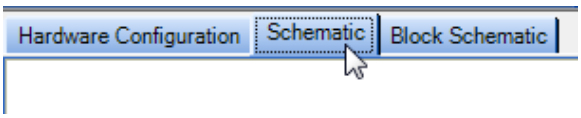


*Figure 20. **Schematic** Tab*

2. To add the appropriate elements to the project space, click and drag the elements from the **Tree ToolBox** on the left of the window to the empty white space located on the right of the window. The toolbox contains all of the algorithms that can run in SigmaDSP.
   a. To add an **Input** block, from the **(IC1) ADAU1467** > **IO** > **Input** > **sdata 32-39** folder, click **Input** (see Figure 21) and drag it into the project space to the right of the toolbox (see Figure 22). By default, Channel 0 and Channel 1 are selected. This configuration matches the analog audio source hardware connections shown in Figure 12 and Figure 13; therefore, no modifications are required.

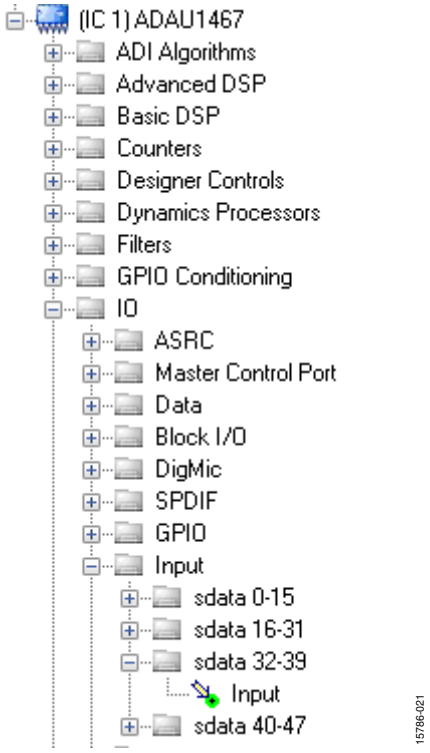


Figure 21. Input Block Selection

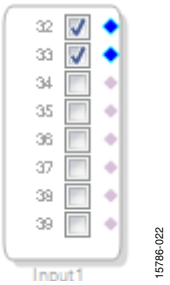


Figure 22. Input Block

   b. Add two **Output** blocks as follows, ensuring that these blocks are assigned to Channel 0 and Channel 1:
      i. From the **(IC1) ADAU1467** > **IO** > **Output** folder, click **Output** (see Figure 23) and drag it into the project space to the right of the toolbox.

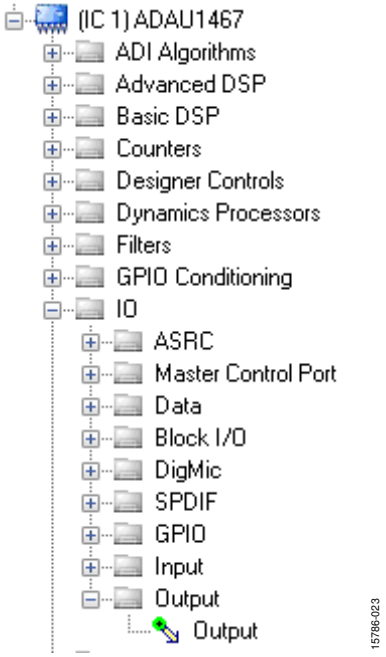


Figure 23. Output Block Selection

      ii. Repeat the previous step to add another output (see Figure 24).

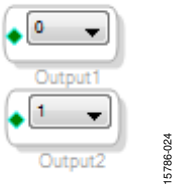


Figure 24. Output Blocks

3. To connect each input channel to its corresponding output channel, click and drag a line, representing a wire, between the blue pin of the input channel and the green pin of the output channel (see Figure 25). Input Channel 0 connects to Output Channel 0, and Input Channel 1 connects to Output Channel 1.

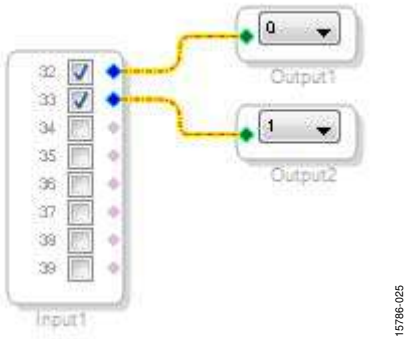


Figure 25. Connected Signal Flow with Stereo Input and Stereo Output

The default register settings in SigmaStudio are configured to match the hardware of the EVAL-ADAU1467Z, including the signal routing between the ADAU1467 and the AD1937 codec.

When these steps are complete, the basic signal flow is complete, and the stereo analog input source passes directly through the SigmaDSP and connects to the stereo analog output.

Add Volume Control

To add a volume control block, take the following steps:

1. From the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder, click **Single Volume,** and drag it into the project space to the right of the toolbox.

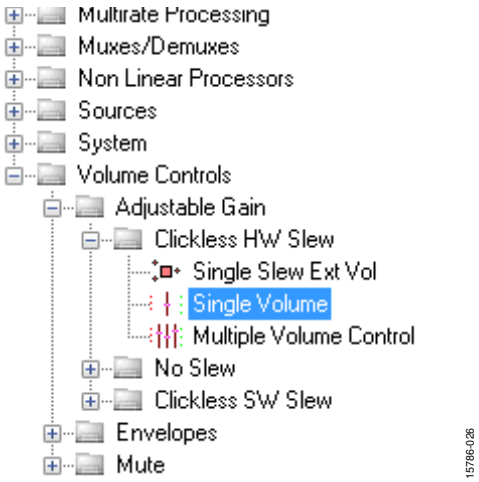


Figure 26. Single Volume Block Selection

2. By default, the volume control block has one input and one output.; in other words, it is a single channel. To add another channel, right click in the empty white space of the **Single-Volume** block, and, from the dropdown menu that appears, select **Grow Algorithm** > **1. Gain (HW Slew)** > **1** (see Figure 27).
3. To delete the existing yellow connection wires (that is, the connections added in Step 3 of the Creating a Basic Signal Flow section), click the **connection wires + Delete**.

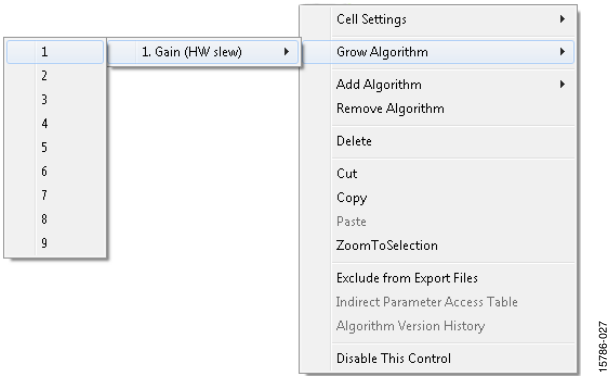


Figure 27. Growing the Volume Control to Two Channels

4. Connect the blocks as shown in Figure 28.

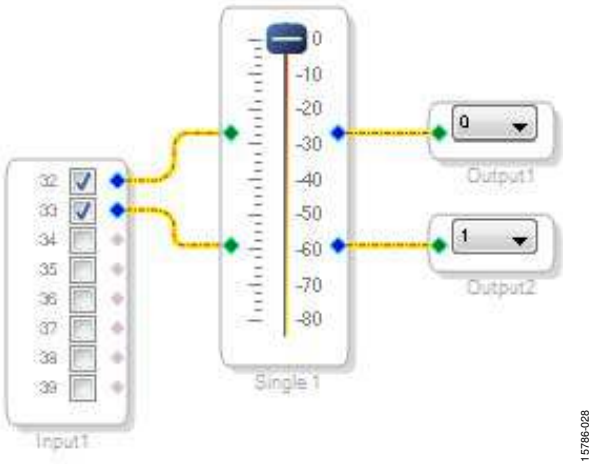


Figure 28. Completed Signal Flow with Volume Control

The schematic is ready to be compiled and downloaded to the evaluation board.

DOWNLOADING THE PROGRAM TO THE DSP

To compile and download the code to the digital signal processor (DSP), click the **Link/Compile/Download** button in the main toolbar of SigmaStudio (see Figure 29). Alternatively, press **F7**.

*Figure 29. **Link/Compile/Download** Button*

After the code downloads to the DSP, the following events occur in order:

1. If the compiler completes compiling the project, the compiled data downloads from SigmaStudio via the USBi to the ADAU1467, and the SigmaDSP starts running.
2. The status bar turns from blue to green, and the mode displayed changes from **Design Mode** to **Active: Downloaded** in the lower right corner of the window (see Figure 30 and Figure 31). Until this point, SigmaStudio is in design mode, as denoted by the blue bar at the bottom of the screen and the words **Design Mode** displayed in the lower right corner of the SigmaStudio window (see Figure 30).

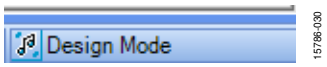


Figure 30. Design Mode and Blue Status Bar

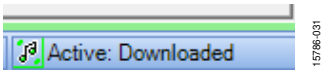


Figure 31. Active Downloaded Mode and Green Status Bar

The signal flow runs on the evaluation board, and the audio passes from the analog input to the analog output. To change the volume in real time, click and drag the volume control slider in the **Schematic** tab.

If the **Output** window is open at the time of compilation, a compiler output log displays, as shown in Figure 32. The **Output** window can be opened or closed by using the keyboard shortcut **CTRL + 4**. The **Output** window shows the compiler output log only if it is open when the **Link/Compile/Download** button is clicked.

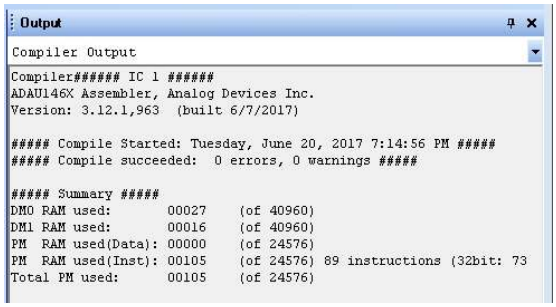


Figure 32. Compiler Output Window

ADDING THE S/PDIF INPUT AND OUTPUT TO THE PROJECT

The EVAL-ADAU1467Z evaluation board has two optical S/PDIF interfaces. One interface is an input that converts the optical signal to an electrical signal, which is sent to the ADAU1467 S/PDIF receiver (the SPDIFIN pin). The other interface is an optical output that takes the electrical output from the ADAU1467 S/PDIF transmitter (the SPDIFOUT pin) and converts it to an optical signal.

Figure 33 shows the locations of the optical input connector and the optical output connector. The connectors are located on the underside of the PCB.

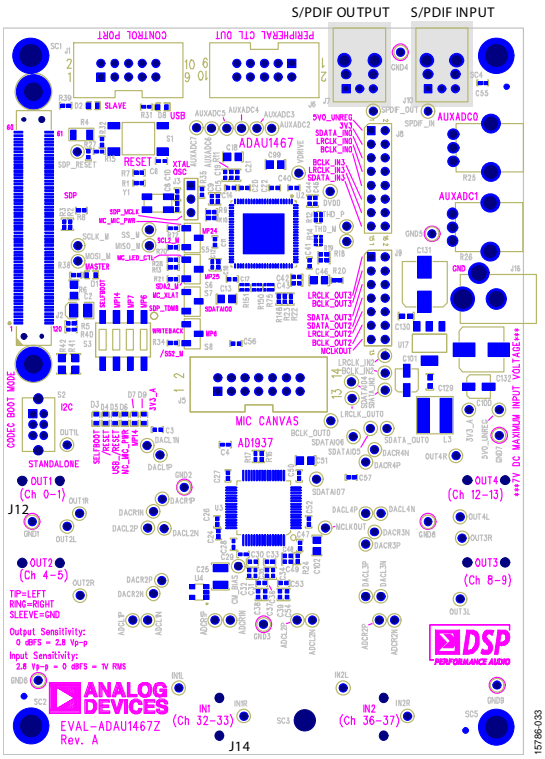


Figure 33. Location of S/PDIF Optical Input (J10) and Output (J7), Rotated 90°

S/PDIF Optical Transmitter and Receiver

The ADAU1467 S/PDIF interfaces are connected directly to optical transmitter and receiver connectors, which convert the electrical signals to and from optical signals, respectively. The connectors accept standard TOSLINK connectors and optical fiber cables (see Figure 34).

Figure 34. TOSLINK Connector and Optical Fiber Cable for the S/PDIF Input and Output

The ADAU1467 S/PDIF receiver accepts signals with sample rates between 18 kHz and 192 kHz. Because the incoming signal is asynchronous to the system sample rate, an asynchronous sample rate converter (ASRC) must be used to convert the sample rate of the incoming signal. Optionally, the SigmaDSP core can be configured to start processing audio samples based on the sample rate of the incoming S/PDIF receiver signal, meaning that no ASRC is required. However, using an ASRC is strongly recommended for performance and reliability reasons.

The ADAU1467 S/PDIF transmitter typically transmits signals from the DSP core, meaning that the sample rate of the audio coming out of the S/PDIF transmitter on the EVAL-ADAU1467Z is typically 44.1 kHz or 48 kHz. Optionally, the S/PDIF transmitter can be configured in a pass through mode, where it simply transmits a copy of the signal directly from the receiver.

Both the S/PDIF receiver and transmitter carry two channels of uncompressed audio.

To add an S/PDIF input and output to the project in SigmaStudio, take the following steps:

1. Connect an S/PDIF source to the EVAL-ADAU1467Z evaluation board by using a standard TOSLINK optical cable and connecting it to the S/PDIF receiver connector, U2 (see Figure 35).

Figure 35. Photograph of the Optical S/PDIF Input Connection

2. Configure the S/PDIF input and output by modifying the ADAU1467 registers as follows:
   a. Click the **Hardware Configuration** tab, then click the **IC 1 - ADAU1467 Register Controls** tab at the bottom of the window (see Figure 36).

*Figure 36. **IC 1 – ADAU1467 Register Controls** Tab*

   b. To access the **SPDIF** tab, click the right arrow to scroll (see Figure 37).Then, click the **SPDIF** tab (see Figure 38). There are several register control tabs listed across the top of the window.

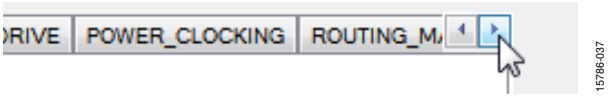


Figure 37. Using the Register Tab Scroll Button

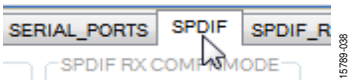


*Figure 38. Selecting the **SPDIF** Tab*

   c. Enable the SPDIF_RESTART register by clicking **Do not restart the audio once a re-lock has occurred** in the **SPDIF RESTART** box. When this button is clicked, the text displayed on the button changes to **Restarts the audio once a re-lock has occurred** and the button color changes from red to green (see Figure 39).

Figure 39. Activating the SPDIF_RESTART Register

   d. To activate the S/PDIF interface, click the **Disabled** button in the **SPDIF TX EN** box. When this button is clicked, the text displayed on the button changes to **Enabled** and the button color changes from red to green (see Figure 40).

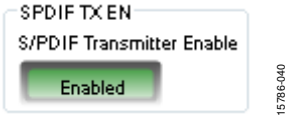


Figure 40. Activating the SPDIF_TX_EN Register

   e. To enable the S/PDIF receiver to operate at a sample rate up to 192 kHz, click **SYSCLKDIV2** in the **SPDIF RX MCLKSPEED** box. When this button is clicked, the text changes to **SYSCLK** and the button color changes from green to red in the **SPDIF TX MCLKSPEED** box. To enable the S/PDIF transmitter to operate at a sample rate up to 192 kHz, click **SYSCLKDIV2** in the **SPDIF RX MCLKSPEED** box. When this button is clicked, the text changes to **SYSCLK** and the button color changes from green to red in the **SPDIF TX MCLKSPEED** box (see Figure 41).

Figure 41. Setting the Maximum Sample Rate of the S/PDIF Receiver and Transmitter

3. Click the **ROUTING_MATRIX** tab (see Figure 42) to allow the configuration of the routing matrix.

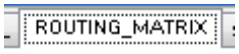


Figure 42. Selecting the ROUTING_MATRIX Tab

4. To configure the S/PDIF receiver signal routing, click the first asynchronous sample rate converter, **ASRC 0** (see Figure 43) and configure ASRC 0 using the dropdown menus until it matches what is shown in Figure 44. This configuration routes the S/PDIF receiver signal through an ASRC before it is accessed in the DSP core. Routing the signal in this way is necessary because the clock recovered from the S/PDIF source is not synchronous to the ADAU1467.

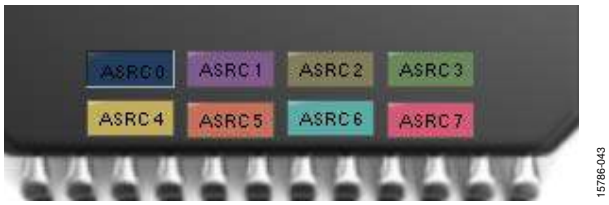


Figure 43. ASRC 0 Control Button

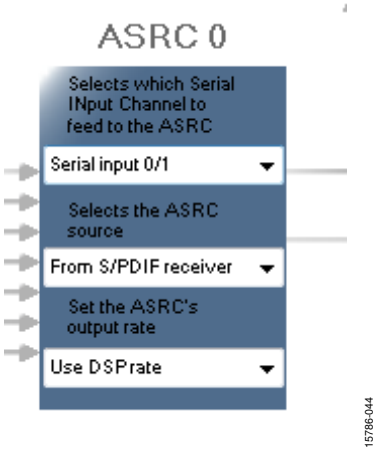


Figure 44. Configuring the ASRC 0 Routing Matrix Registers

5. Configure the S/PDIF transmitter (Tx) signal routing as follows:
   a. Click the **S/PDIF TX** box (see Figure 45).

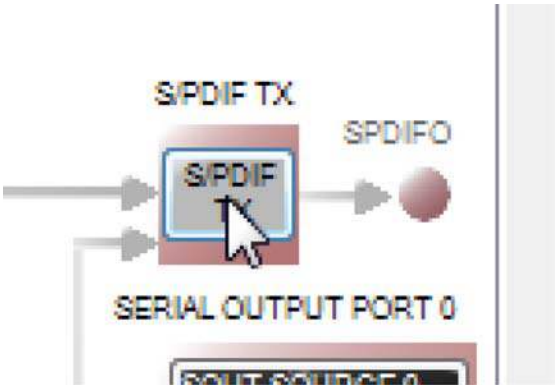


Figure 45. Configuring the S/PDIF Transmitter Routing Matrix Register

   b. From the dropdown menu that appears, select **From DSP** to choose the signal coming from the DSP core (see Figure 46).

Figure 46. Routing the DSP Core Outputs to the S/PDIF Transmitter

   c. Close the dialog box shown in Figure 46.
   d. Confirm that the setting has taken effect by verifying that the color of the **S/PDIF TX** box has changed from gray to black (see Figure 47). If the color of the box changes to black, the DSP core has been routed to the S/PDIF transmitter; therefore, the output of ASRC 0 can be used in the DSP program.

Figure 47. Confirming that the DSP Core Outputs are Routed to the S/PDIF Transmitter

6. Click the **Schematic** tab at the top of the window to return to the schematic design view.
7. Add an S/PDIF input to the project as follows:
   a. From the **IO > ASRC > From ASRC** folder, click **Asrc Input** (see Figure 48) and drag it into the project space to the right of the toolbox (see Figure 49).

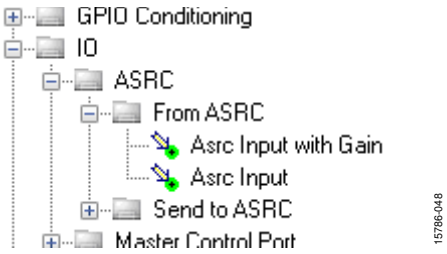


Figure 48. ASRC Input Block Selection

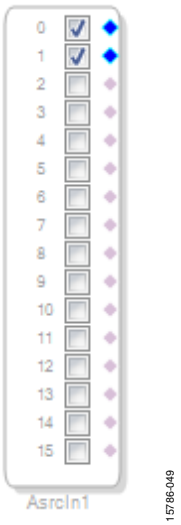


Figure 49. ASRC Input Block

Because the left and right signals of the S/PDIF receiver are passing through the ASRC 0, the input to the DSP program is the **Asrc Input** block in SigmaStudio. This naming convention is such that all blocks in SigmaStudio are named from the perspective of the DSP core. Therefore, the **Asrc Input** block in SigmaStudio represents the input to the DSP from the ASRC outputs. The inputs to the ASRCs themselves are defined in the register window (see Figure 44).

By default, Channel 0 and Channel 1 are active when their corresponding checkboxes are selected. Because the ASRC 0 outputs correspond to Channel 0 and Channel 1, this default configuration can be used (see Figure 49). For reference, a mapping of the ASRC outputs to the corresponding channels on the **Asrc Input** block in the DSP schematic is provided in Table 1.

Table 1. ASRC Output to SigmaStudio Input Channel Mapping

ASRC Output	Corresponding Channels on ASRC Input Block in SigmaStudio
ASRC 0	Channel 0 and Channel 1
ASRC 1	Channel 2 and Channel 3
ASRC 2	Channel 4 and Channel 5
ASRC 3	Channel 6 and Channel 7
ASRC 4	Channel 8 and Channel 9
ASRC 5	Channel 10 and Channel 11
ASRC 6	Channel 12 and Channel 13
ASRC 7	Channel 14 and Channel 15

8. Add two S/PDIF outputs to the project as follows:
   a. From the **IO** > **SPDIF** > **Output** folder, click **Spdif Output** (see Figure 50) and drag it into the project space to the right of the toolbox.

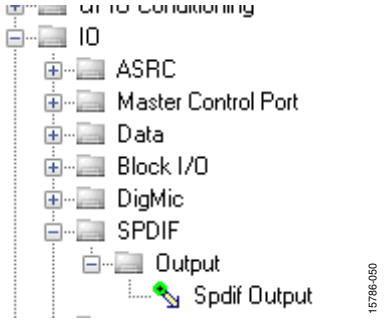


Figure 50. S/PDIF Output Block Selection

   b. Repeat the previous step to add another **Spdif Output** block.
9. Connect the signals from the **Asrc Input** block to the **Spdif Output** blocks so that the resulting signal flow resembles Figure 51.

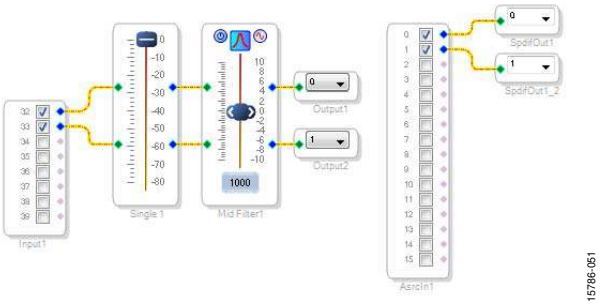


Figure 51. Signal Flow Including S/PDIF Input (via the ASRC) and S/PDIF Output

10. Click the **Link/Compile/Download** button (see Figure 29) or press **F7**. The signal flow then compiles and downloads to the hardware.
11. Confirm proper operation by checking that any signal input to the S/PDIF optical receiver is copied and output on the S/PDIF optical transmitter.

Add a Filter

To add a filter, take the following steps:

1. Add a **Medium-Size Eq** block to the project space as follows:
   a. From the **Filters** > **Second Order** > **Double Precision** folder, click **Medium-Size Eq** (see Figure 52) and drag it into the project space to the right of the toolbox.

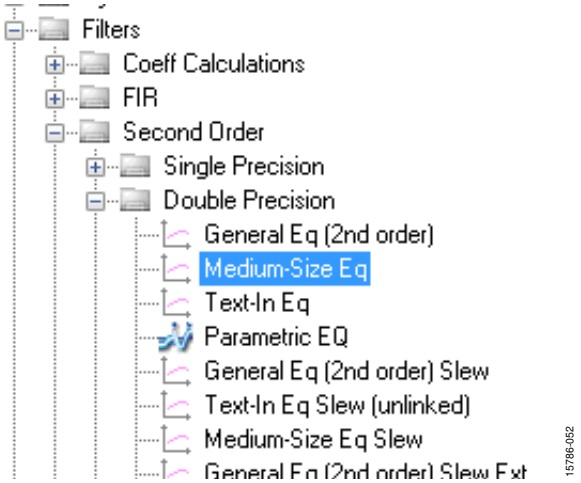


*Figure 52. **Medium-Size Eq** Block Selection*

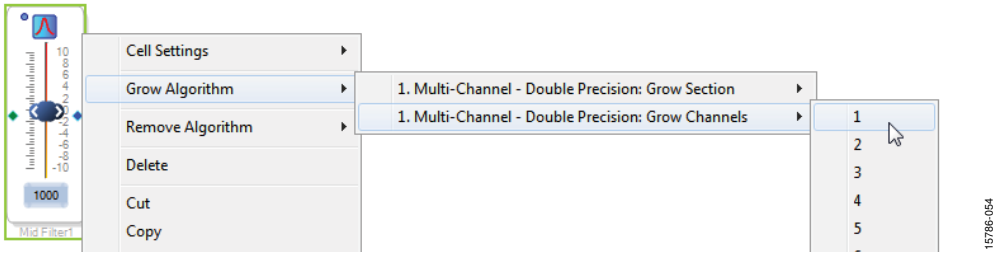


Figure 53. Adding a Channel to the Filter

   b. By default, the block has one input and one output (single-channel). To add another channel, right click in the empty white space of the **Medium-Size Eq** block, then select **Grow Algorithm** > 1. **Multi-Channel - Double Precision: Grow Channels** > 1 from the dropdown menu that appears (see Figure 53).

2. Connect the filter in series between the **Asrc Input** block and the **Spdif Output** blocks so that the filter can be applied to the signals passing through the DSP. The completed signal flow resembles Figure 54.

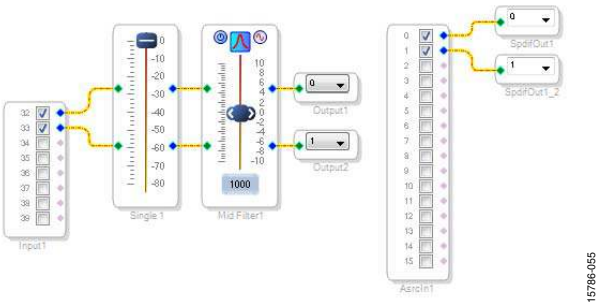


Figure 54. Completed Signal Flow

3. Click the **Link/Compile/Download** button (see Figure 29) or press **F7** to compile the signal flow and download it to the hardware. The audio signal passes from the S/PDIF receiver through the ASRCs into the DSP and the EQ filter, and then out on the S/PDIF transmitter. To change the settings of the EQ filter, click the blue icon at top of the block. To change the filter gain in real time while the project is running, drag the control slider in SigmaStudio.

CONTROLLING VOLUME WITH A POTENTIOMETER

The 10-bit auxiliary analog-to-digital converter (ADC) on the ADAU1467 eliminates the need for a microcontroller in many applications by using analog control signals as user interface devices. For example, the EVAL-ADAU1467Z includes two 10 kΩ linear potentiometers connected to Auxiliary ADC Channel 0 (AUXADC0) and Auxiliary ADC Channel 1 (AUXADC1). These potentiometers can be used as an inexpensive, versatile, and physical way to control parameters such as gain, filter corner frequency, slew rate, and compression level.

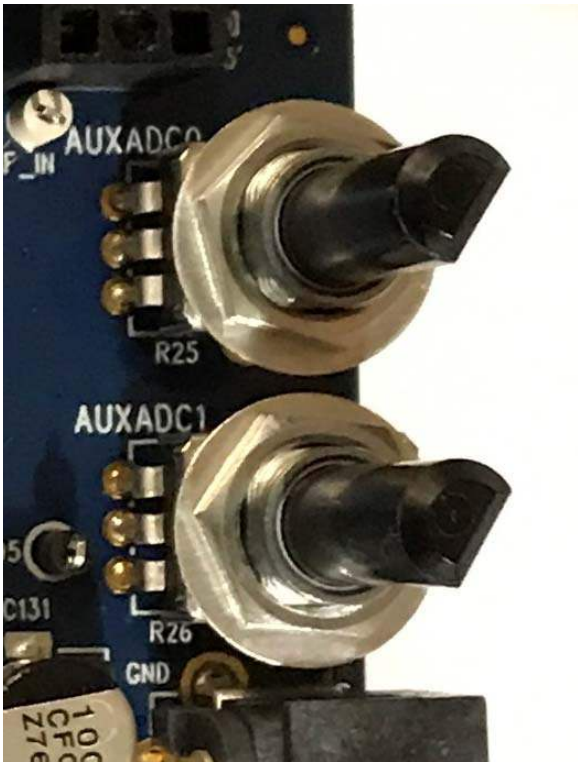


Figure 55. Potentiometers Connected to AUXADC0 and AUXADC1

The following example procedure demonstrates how a potentiometer can be configured as a stereo volume control.

1. Create a new project in SigmaStudio, and use the **Hardware Configuration** tab to set up the ADAU1467 as described in the Setting Up Communications in SigmaStudio section.
2. Add an input and two output blocks as described in the Creating a Basic Signal Flow section.
3. Add an **Auxiliary ADC Input** block to the project space as follows:
   c. From the **IO** > **GPIO** > **Input** folder, click **Auxiliary ADC Input** (see Figure 56) and drag it into the project space to the right of the toolbox.

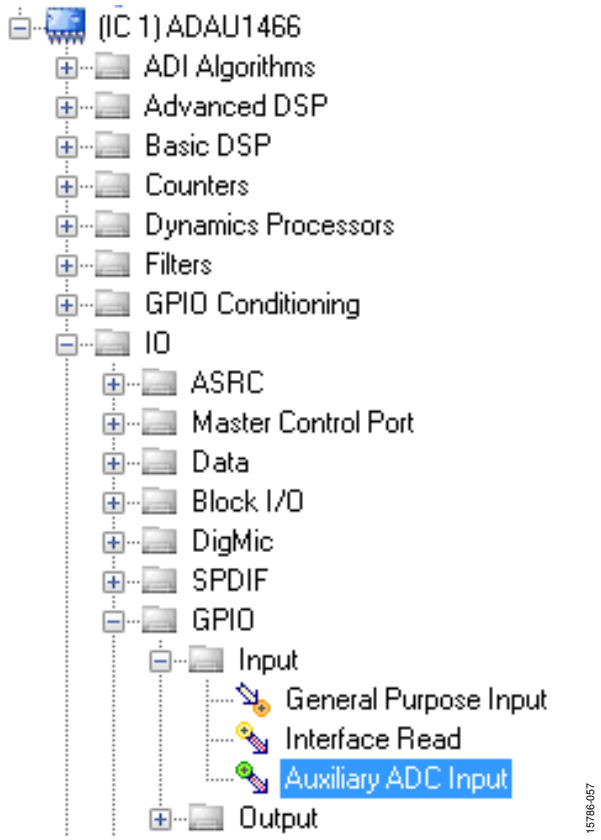


*Figure 56. **Auxiliary ADC Input** Block Selection*

4. Add an **Arithmetic Shift** block to the project space as follows:
   a. From the **Basic DSP** > **Arithmetic Operations** folder, click **Arithmetic Shift** (see Figure 57) and drag it into the project space to the right of the toolbox.

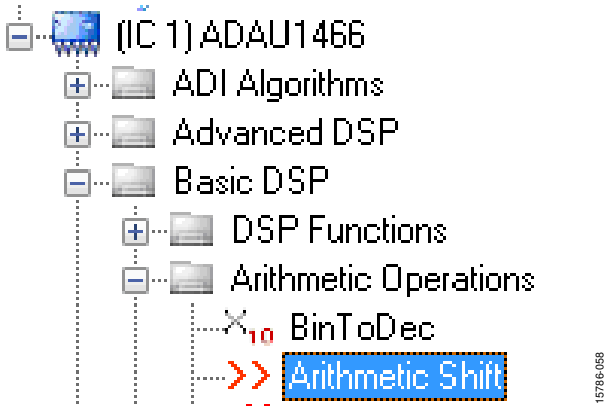


*Figure 57. **Arithmetic Shift** Block Selection*

   b. The arithmetic shift block performs a bitwise right shift or left shift. Click the blue button to select the direction. Ensure the block is performing a left shift. The block appears as shown in Figure 62.
   c. To set the number of bits by which the input is shifted to 14, click and type in the yellow text box. The block appears as shown in Figure 62.
5. Add two **DSP Readback** blocks to the project and set their numeric format as follows:
   a. From the **Basic DSP** > **DSP Function** folder, click **DSP Readback** (see Figure 58) and drag it into the project space to the right of the toolbox.

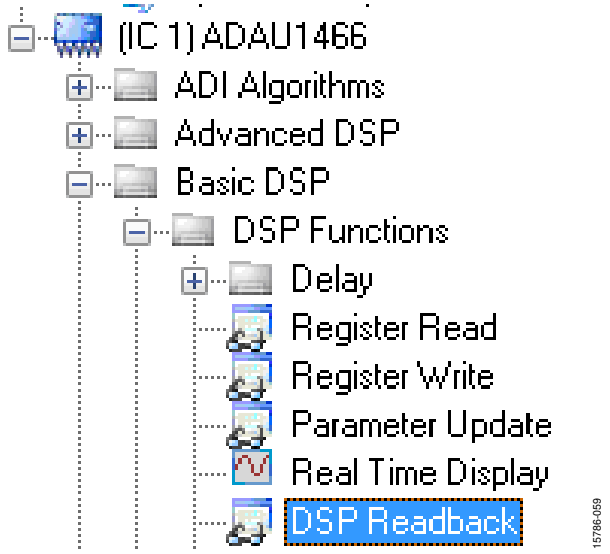


Figure 58. DSP Readback Block Selection

   b. Repeat the previous step to add another **DSP Readback** block.

c. The **DSP Readback** block uses the USBi interface to read the value of a signal from the memory of the DSP core as the algorithm is executing. The block passes the signal through from its input to its output unchanged.
   i. Press the **Read** button to obtain the instantaneous value of the signal passing through the block. It is also possible to set the block to poll the value repeatedly. This feature is useful for debugging, but it increases the amount of processing, USB communication, and screen refreshes performed by SigmaStudio substantially. Avoid setting a large number of **DSP Readback** blocks to read continuously because this action may cause the PC to run slowly. Note that this action does not affect the real-time processing on the SigmaDSP core.
   ii. On each of the two **DSP Readback** blocks, click on the blue dot to the left of the **Read** button to read both blocks continuously (see Figure 59).

Figure 59. Activating Continuous Readback

   iii. For one of the DSP readback blocks, change the numeric format used to decode and display of the value of the signal to 32.0 by typing 32 in the left format box then pressing the **Tab** key. SigmaDSP uses a numeric format of 8.24 for audio signals.

6. Add a **Single Slew Ext Volume** block to the project space as follows:
   a. From the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder, click **Single Slew Ext Vol** (see Figure 60), and drag it into the project space to the right of the toolbox.

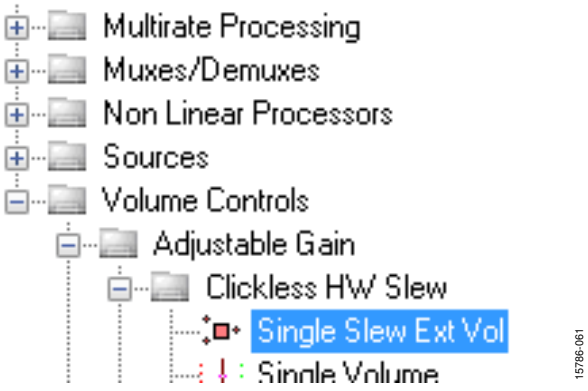


*Figure 60. **Single Slew Ext Vol** Block Selection*

   b. By default, the **Single Slew Ext Vol** block has one audio signal input. To add another channel, right click in the empty white space of the **Single Slew Ext Vol** block, and select **1 > 1. Gain (HW slew) > Grow Algorithm** from the dropdown menu that appears (see Figure 61).

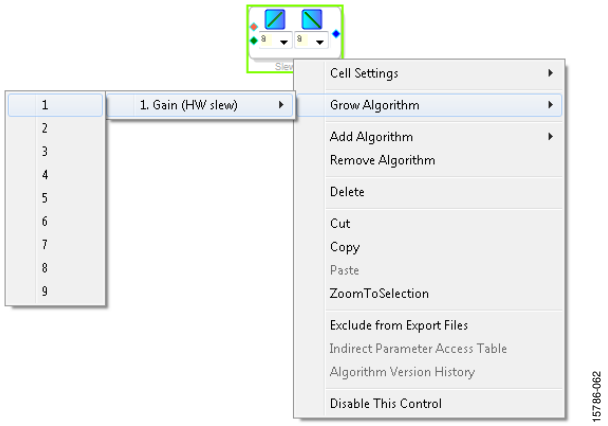


*Figure 61. Growing the **Single Slew Ext Vol** Block to Two Channels*

7. Wire the blocks together as shown in Figure 62. Note that the position of blocks in the diagram does not matter.
8. Click the **Link/Compile/Download** button (see Figure 29) or press **F7** to compile the signal flow and download it to the hardware. The audio signal passes from the S/PDIF receiver through the ASRCs into the DSP and the EQ filter, and then out on the S/PDIF transmitter. To change the settings of the EQ filter, click the blue icon at top of the block. Drag the control slider in SigmaStudio to change the filter gain in real-time while the project is running.

The schematic (see Figure 62) shows audio from input Channel 0 and Channel 1 connected to the input of a volume control block. The volume is controlled by the value of the AUXADC1 channel, which is controlled by the left potentiometer (R1).

The output of the auxiliary ADC on the ADAU1467 is a 10-bit integer value in a 32-bit register. The first **DSP Readback** block, before the left shift, displays the output of the ADC in 32.0 format, which can be interpreted as 32 integer bits and 0 fractional bits. When the potentiometer is turned fully counter clockwise, this block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1023 (within the range of the component tolerance).

The native audio format of the ADAU1467 is 8.24. In this example, the volume control multiplies the input signal by a fractional value ranging from 0 (silence) to 1 (unity gain). Therefore, the control signal from the ADC must be left shifted 14 bits to scale the maximum value appropriately.

The second **DSP Readback** block, after the left shift, displays the output of the ADC in 8.24 format, which may be interpreted as 8 integer bits and 24 fractional bits. When the potentiometer is turned fully counter clockwise, this block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1 (within the range of the component tolerance).

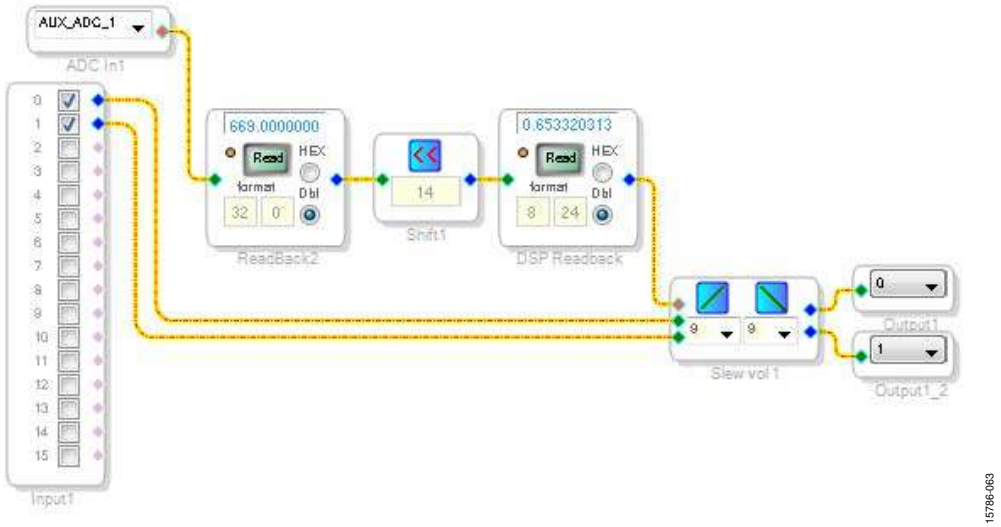


Figure 62. Completed Signal Flow with DSP Readback

EVALUATION BOARD FEATURES

The EVAL-ADAU1467Z provides access to the serial ports, S/PDIF interfaces, multipurpose pins, and auxiliary ADCs of the ADAU1467.

AD1937 CODEC

One of the four serial input ports and one SDATAIOx pin are connected to the ADCs of the AD1937, and one of the four serial output ports and three SDATAIOx pins are connected to the digital-to-analog converts (DACs) of the AD1937. Each serial data pin carries two channels of serial audio in I²S format, for a total of four channels of analog audio input and eight channels of analog audio output.

AD1937 Boot Mode

The AD1937 is capable of running in standalone mode or being booted and configured through its I²C control port. Switch S2 selects the boot mode of the AD1937 codec as shown in Figure 63, and this switch is set to STANDALONE by default. When running in standalone mode, the serial ports of the AD1937 are configured as clock slaves. Therefore, the corresponding serial ports on the ADAU1467 must be set as clock masters. By default, all serial ports on the ADAU1467 are set as clock masters when a new project is created in SigmaStudio.

Standalone mode eliminates the need for the user to configure the registers of the AD1937 via its I²C port. This mode fixes the sample rate of the AD1937 at 44.1 kHz or 48 kHz. The analog audio inputs and outputs on the EVAL-ADAU1467Z can be distorted or silent if a sample rate other than 44.1 kHz or 48 kHz is used for the ADAU1467 serial ports.

The alternate I²C master port pins of ADAU1467 are connected to the I²C control port of the AD1937 when Switch S2 is set to I²C boot mode; this requires reconfiguration of the master control port from SPI to I²C and enabling the alternate I²C port on the MP24 pin and MP25 pin. This configuration is beyond the scope of this user guide; however, it enables the ADAU1467 to boot and configure all of the control registers of the AD1937. When configured manually, the codec is flexible and can run at any sample rate up to 192 kHz.

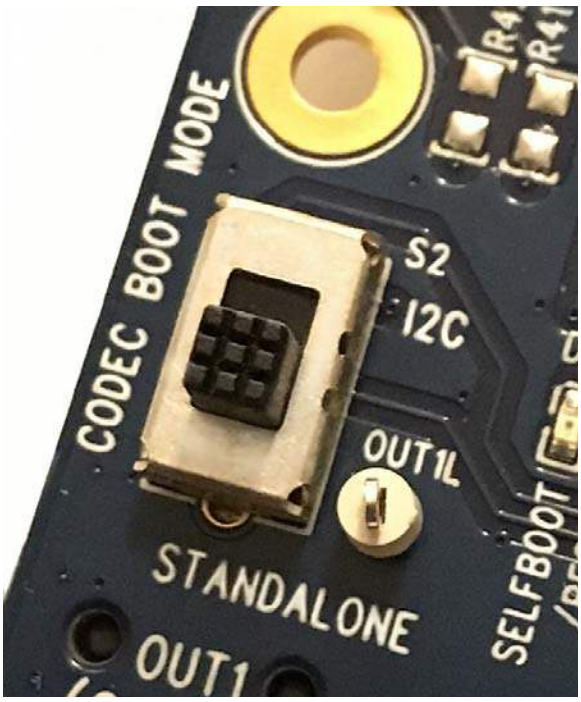


Figure 63. AD1937 CODEC Boot Mode Selection Switch S2

Stereo Line Inputs

Two stereo input jacks allow four, single-ended, line level, analog input signals. The AD1937 ADC inputs are configured such that the full scale is 2.8 V p-p, which is approximately 1 V rms for a sine wave. Any signal that exceeds 2.8 V p-p at the audio jack is clipped, which creates distortion. The signals are fed to active low-pass filters and converted to differential pairs before reaching the ADCs of the AD1937. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

Figure 64. Standard Stereo TRS 1/8 Inch Mini Audio Plug and Cable

The stereo input jacks accept standard stereo TRS 3.5 mm (1/8 inch) mini plugs (tip connected to left, ring connected to right, sleeve connected to ground) with two channels of audio (see Figure 64).

The signals pass through the AD1937 ADCs and then are sent to the ADAU1467 serial input ports in I²S format. The mapping of input signals to input channels in SigmaDSP and SigmaStudio is shown in Table 2. See the Serial Port Configuration Using the SDATAIOx Pins section for the configuration of the SDATAIOx pins.

Table 2. Mapping of Stereo Analog Input Signals to SigmaStudio Channels

Input Jack	Plug Contact	AD1937 ADC Pins	ADAU1467 Serial Input Pins	Input Channel in SigmaStudio
J14	Left (tip)	ADC1LN, ADC1LP	SDATA_IN2	32
J14	Right (ring)	ADC1RN, ADC1RP	SDATA_IN2	33
J15	Left (tip)	ADC2LN, ADC2LP	SDATAIO4	36
J15	Right (ring)	ADC2RN, ADC2RP	SDATAIO4	37

Stereo Line Outputs

Four stereo output jacks allow eight line level analog output signals. The AD1937 DAC outputs are configured such that a full-scale signal is 2.8 V p-p at the jack, which is approximately 1 V rms for a sine wave. The signals output from the DACs are fed to active low-pass filters and then ac-coupled before reaching the output jacks. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

The output filters are designed to drive high impedance loads, for instance, loads at the input to active speakers. Some low impedance loads (for example, loads from headphones) can also be driven by these outputs. However, very low impedance loads (for example, loads from passive speakers) cannot be driven by these outputs.

The stereo output jacks accept standard stereo TRS 3.5 mm (1/8 inch) mini plugs (tip connected to left, ring connected to right, sleeve connected to ground) with two channels of audio (see Figure 64).

The signals pass from the ADAU1467 serial outputs in I2S format to the AD1937 DACs, where they are converted to analog signals and sent through the output filters to the output jacks. The mapping among the SigmaStudio output channels, output serial ports, and output jacks is shown in Table 3.

See the Serial Port Configuration Using the SDATAIOx Pins section for the configuration of the SDATAIOx pins.

Table 3. Mapping of SigmaStudio Channels to Output Jacks

Output Jack	Plug Contact	AD1937 DAC Pin	ADAU1467 Serial Output Pin	Output Channel in SigmaStudio
J12	Left (tip)	OL1	SDATA_OUT0	0
J12	Right (ring)	OR1	SDATA_OUT0	1
J13	Left (tip)	OL2	SDATAIO5	4
J13	Right (ring)	OR2	SDATAIO5	5
J18	Left (tip)	OL3	SDATAIO6	8
J18	Right (ring)	OR3	SDATAIO6	9
J17	Left (tip)	OL4	SDATAIO7	12
J17	Right (ring)	OR4	SDATAIO7	13

SERIAL AUDIO DATA INPUT AND OUTPUT

The EVAL-ADAU1467Z demonstrates how the SDATAIOx pins make serial ports on the ADAU1467 more flexible. Only one input serial port and one output serial port is required to connect the ADAU1467 to the AD1937 codec using only stereo digital data lines. The remaining serial ports are available to connect to other audio inputs and outputs.

Input Serial Port 0 and Input Serial Port 3 are available on Header J8. Output Serial Port 2 and Output Serial Port 3 are available on Header J9. These headers are standard, two column headers with 0.1 inch (2.54 mm) spacing. There is one signal column and one ground column. Always connect at least one ground wire between the header and the external signal source or sink to maintain proper signal integrity. A standard ribbon cable provides signal integrity over longer distances because signal wires are separated by ground wires.

In addition to the signals from the serial audio data ports, Header J8 includes connections to the unregulated 5 V power supply and the regulated 3.3 V power supply. Header J9 includes a buffered connection to MCLK, the master clock from the CLKOUT pin from the ADAU1467.

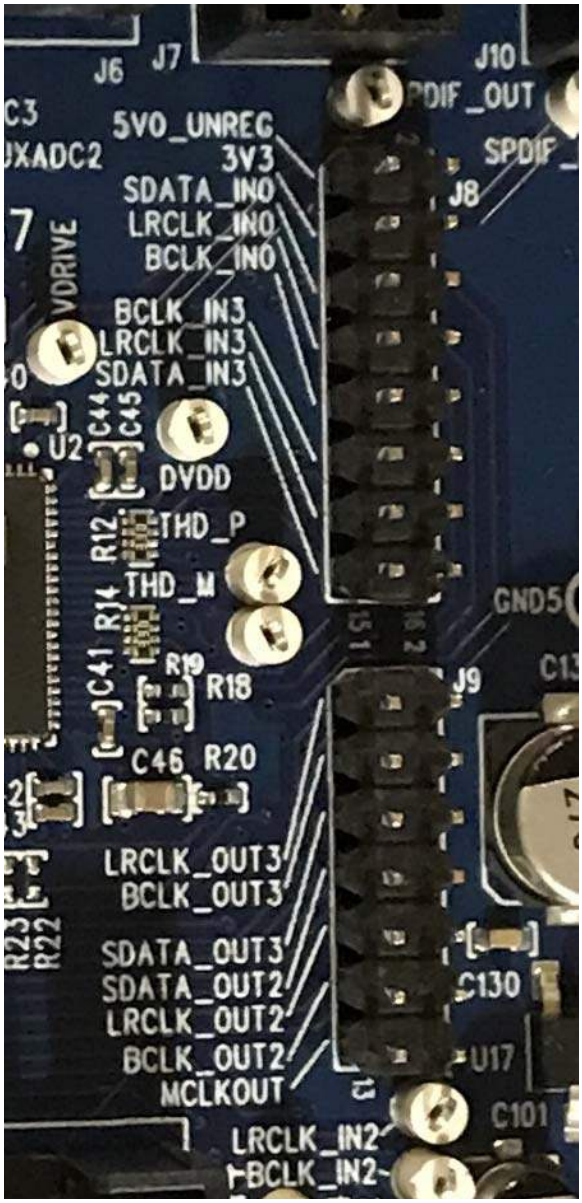


Figure 65. Serial Port Headers, J8 and J9

MULTIPURPOSE PINS (MPx)

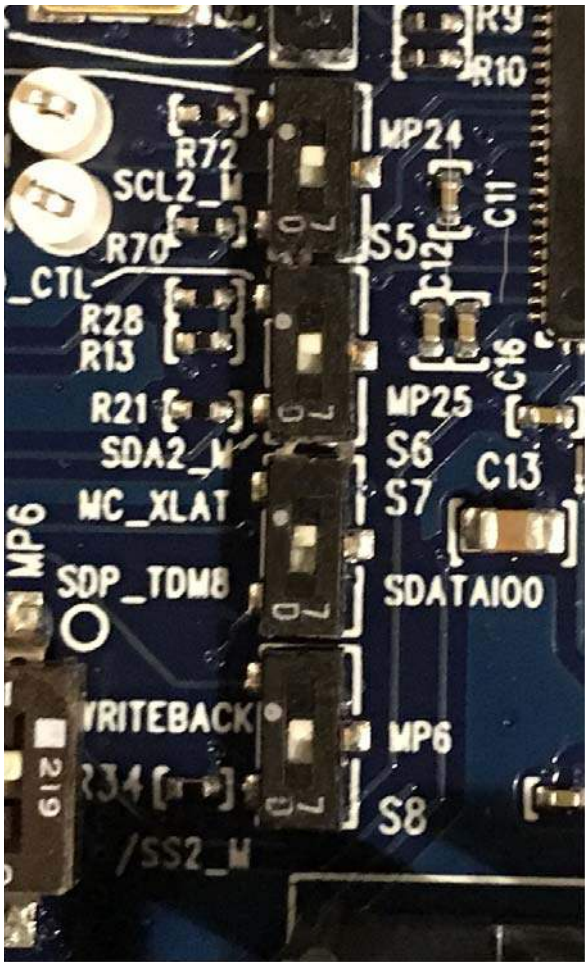


Figure 66. Multipurpose Pin Function Selection Switches S5 to S8

The multipurpose pins on the ADAU1467 can be used for general-purpose inputs or outputs when configured as such using the ADAU1467 control registers. Of the 14 multipurpose pins, three are connected to switches that pull the pins low or tie them high, three are on test points and connected to high impedance inputs to LED drivers, and two are available headers. The remaining six pins are used for other functionality and are, therefore, unavailable for use as multipurpose pins.

The signal from the LRCLK_OUT1/MP5 pin is fed to an inverter that drives LED D4. The signal from the LRCLK_OUT3/MP9 pin is fed to an inverter that drives LED D3. The signal from the LRCLK_IN1/MP11 pin is fed to an inverter that drives LED D5.

The five multipurpose pins available for use as general-purpose inputs or outputs, along with their access points on the evaluation board, are described in Table 4.

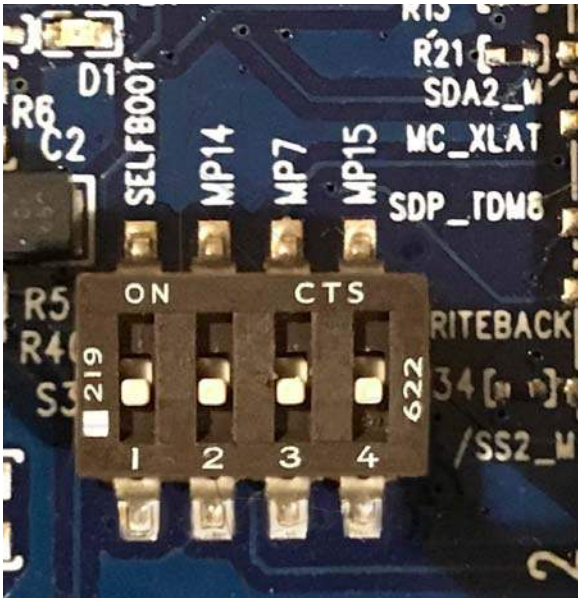


Figure 67. Self Boot Slide Switch

To configure the operation of the multipurpose pins, navigate to the **MULTIPURPOSE** tab in the **Hardware Configuration** tab in SigmaStudio (see Figure 68).

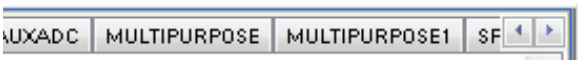


Figure 68. Multipurpose Pin Configuration in SigmaStudio

Table 4. Multipurpose Pins and Hardware Access Points

Multipurpose Pin	Connection	Access Point
LRCLK_OUT1/MP5	Input to inverter (LED D4)	TP56
LRCLK_OUT3/MP9	Input to inverter (LED D3)	TP48
LRCLK_IN1/MP11	Input to inverter (LED D5)	TP29
LRCLK_IN2/MP12	Pin multiplexed with LRCLK_IN2	Header J3, Pin 4
LRCLK_IN3/MP13	Pin multiplexed with LRCLK_IN3	Header J2, Pin 4

STATUS LEDs

Six status LEDs provide information about the state of the EVAL-ADAU1467Z evaluation board (see Figure 69). For additional information pertaining to the status LEDs, see Table 6.

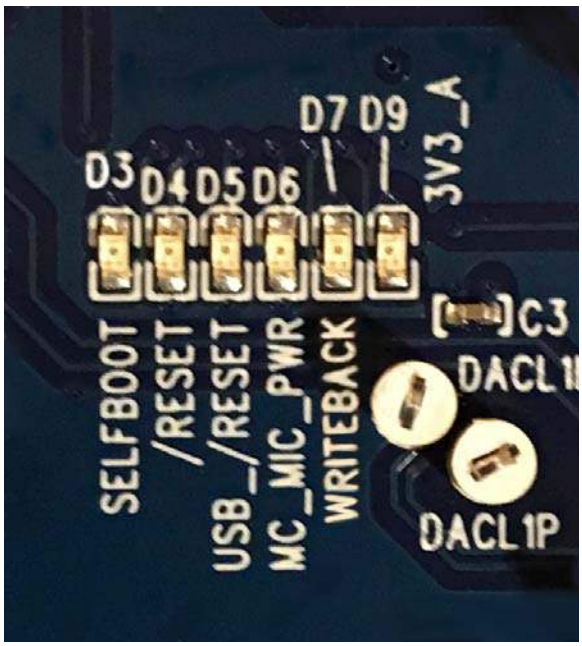


Figure 69. Status LEDs

AUXILIARY ADC PINS

The ADAU1467 has a 10-bit, successive approximation register (SAR) ADC multiplexed across six input channels. Channel AUXADC0 and Channel AUXADC1 are connected to linear Potentiometer R1 and Potentiometer R2. Channel AUXADC2 to Channel AUXADC5 are accessible on test points next to the ADAU1467. Inputs to the ADCs between 0 V and 3.3 V can be connected to these pads and then used in the SigmaStudio signal flow (see Figure 70).

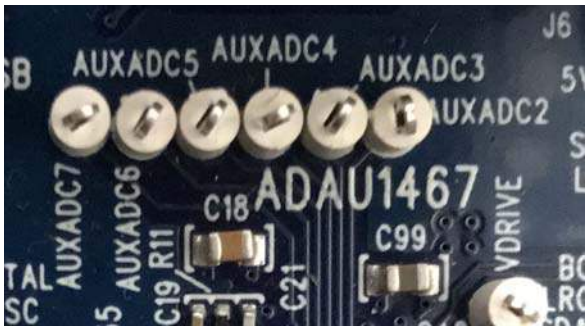


Figure 70. Auxiliary ADC Test Points Communications Header

The communications header is a 10-pin header designed to work with the EVAL-ADUSB2EBZ or USBi. The SPI signals are wired from the communications header to the corresponding SPI slave port pins on the ADAU1467. The I^2C pins are not used in this design. A reset line is also included, which allows the user to reset the devices on the board via a command in SigmaStudio. When the USBi is connected and powered and the computer recognizes the USBi on its USB 2.0 port, LED D1 illuminates (see Figure 11).

SELF BOOT

A 1 Mb, 20 MHz, SPI, serial EEPROM memory is included on the EVAL-ADAU1467Z evaluation board. The ADAU1467 is capable of booting and executing a program without help from an external microcontroller. This feature allows any project developed within SigmaStudio to execute when the ADAU1467 powers up or on a rising edge of the $\overline{\text{RESET}}$ pin. Position 1 of Switch S3 switch, the top position of the DIP switch (see Figure 71), sets the state of the SELFBOOT pin of the ADAU1467, which determines whether a self boot operation occurs.

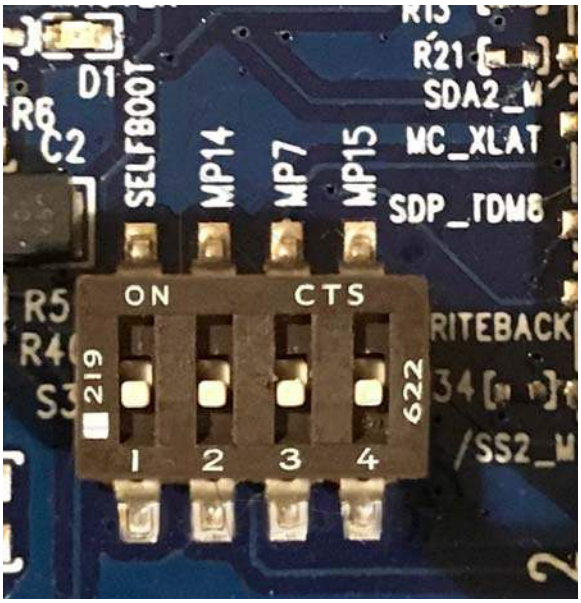


Figure 71. Self Boot Slide Switch

To use the self boot functionality, take the following steps:

1. Add an **E2Prom** block to the project space of the **Hardware Configuration** tab. From the **Processors (ICs/DSPs)** folder, click **E2Prom** (see Figure 72) and drag it into the project space to the right of the toolbox.

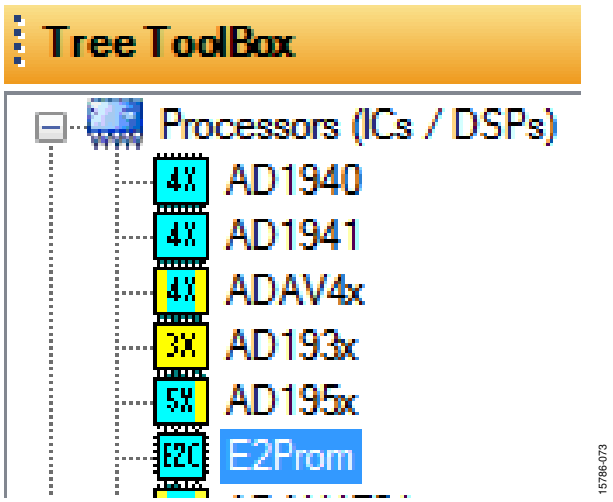


Figure 72. E2Prom IC Selection in SigmaStudio

2. Connect the green input pin of the **E2Prom** IC to one of the available blue output pins of the **USB Interface** block.
3. Set the communication mode to **SPI 0x1 ADR0** (see Figure 73). (There is no physical connection between the USBi connector and the EEPROM on the EVAL-ADAU1467Z. SigmaStudio writes a small program to the ADAU1467, which then writes the self boot data from the master SPI port to the EEPROM.)

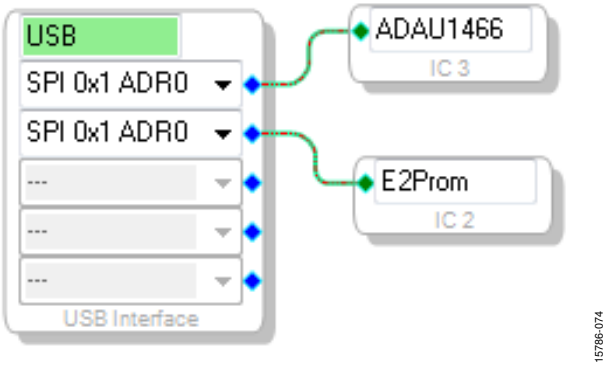


Figure 73. E2Prom Setup in the Hardware Configuration Tab

4. Before downloading the self boot data to the EEPROM, click the **Link-Compile-Download** button (see Figure 29) or press **F7** to compile the SigmaStudio project file.
5. When writing to the EEPROM, set the self boot switch (Position 1 of Switch S3) to the disabled position.
6. Right click the empty white space in the ADAU1467 **IC** block in the **Hardware Configuration** tab of SigmaStudio. From the menu that appears, select **Self-boot Memory**, then **Write Latest Compilation through DSP** (see Figure 74).

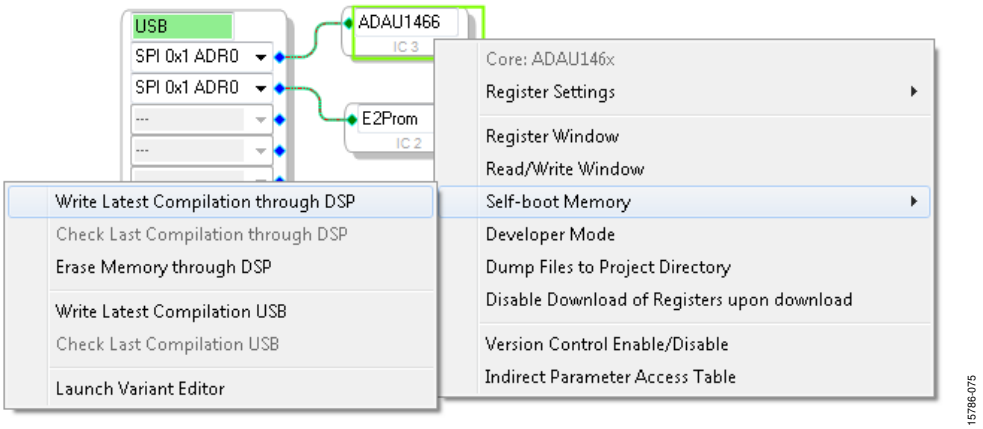


Figure 74. Writing to the EEPROM Through the ADAU1467 Master SPI Port

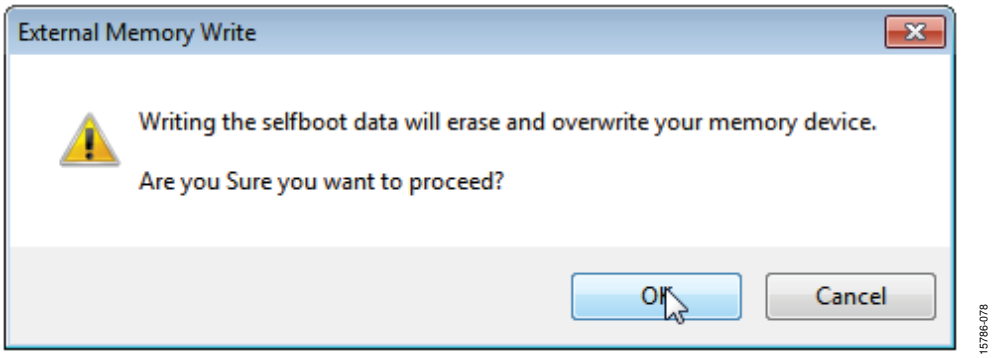


Figure 75. External Memory Erase and Overwrite Warning Window

7. An **EEPROM Properties** dialog box appears. Enter the appropriate values into the text fields as shown in Figure 76, then click **OK**.

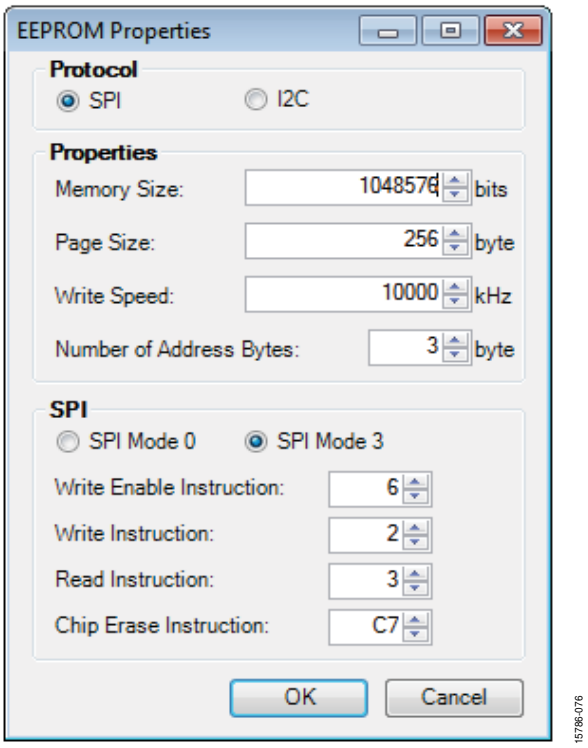


*Figure 76. **EEPROM Properties** Window and Required Settings*

8. A warning dialog box appears to remind the user that executing an external memory write erases and overwrites any data currently stored on the EEPROM (see Figure 75). Click **OK** to proceed.
9. SigmaStudio begins the EEPROM write operation. This operation can take several minutes to complete (see Figure 77). When the status window disappears, the operation is complete.

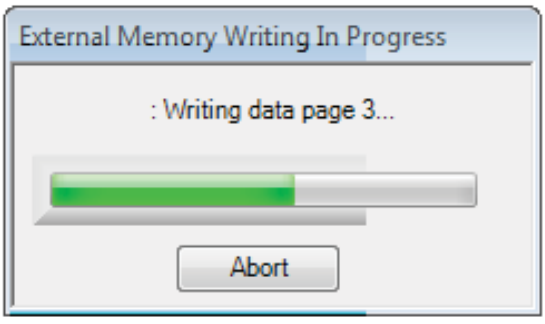


Figure 77. External Memory Write Operation Status Window

To execute a self boot operation, take the following steps:

1. Set the self boot switch (S2) to enabled.
2. Press and release the RESET push-button (S1).

A self boot operation is then performed, and the ADAU1467 runs a program.

RESET

To manually reset the ADAU1467 and AD1937, press and release the RESET push-button, S1 (see Figure 78). A reset generator circuit toggles the reset pins on the ADAU1467 and AD1937 to perform a full hardware reset of both devices.

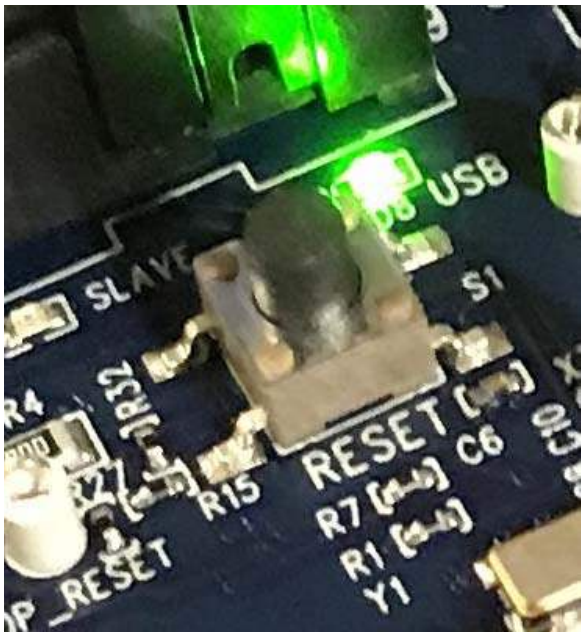


Figure 78. Manual Reset Push-Button

To generate a reset in software, right click in the empty white border of the **USB Interface** block in the **Hardware Configuration** tab, and then choose **Device Enable/Disable** from the menu that appears (see Figure 79). Performing this action sets the system reset signal to logic low.

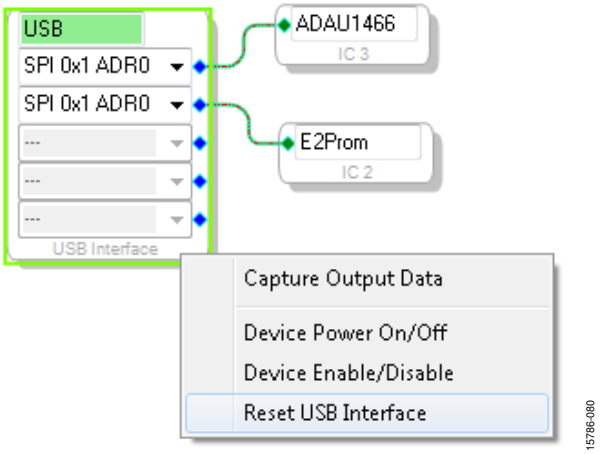


Figure 79. Toggling the Reset Signal in SigmaStudio

SERIAL PORT CONFIGURATION USING THE SDATAIOx PINS

The SDATAIOx pins provide additional serial audio data inputs or outputs and expand the functionality and versatility of the serial ports. In earlier generations of the SigmaDSP architecture, serial ports are limited to a single SDATA pin. If this serial data pin is configured in a stereo mode, the remaining channels associated with the port are inaccessible. Device interfaces with a single LRCLK and BCLK pair and multiple stereo data lines (for example, in a case with multiple connections in the I²S format) required using multiple SigmaDSP serial ports.

The SDATAIOx pins on the ADAU1463 and ADAU1467 eliminate this bottleneck. The connection between the SigmaDSP and the AD1937 codec uses four I²S data lines for the eight DAC channels and two I²S data lines for the four ADC channels. The EVAL-ADAU1467Z supplements the SDATA_OUT0 pin with three SDATAIOx pins and the SDATA_IN2 pin with one SDATAIOx pin. This configuration connects all of the audio channels of the AD1937 while using only one input serial port and one output serial port. The connections are shown in Figure 80.

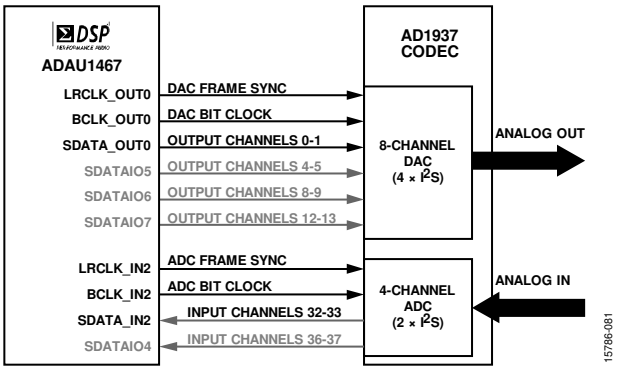


Figure 80. Serial Ports Connections to the AD1937 Codec

EVALUATION BOARD HARDWARE

IC DESCRIPTIONS

Table 5. IC Descriptions

Reference	Functional Name	Description
U1	Clock buffer, 1:9	Buffers the master clock signal (MCLK) for distribution to multiple ICs and to headers.
U2	ADAU1467 SigmaDSP audio processor	Acts as an audio hub for all audio inputs and outputs in the system and performs digital signal processing on those signals.
U3	AD1937 audio codec	Converts analog audio inputs to digital data for the ADAU1467 processor and takes digital data back from the ADAU1467 to convert to analog audio output signals.
U4	ADA4610-1 junction gate field-effect transistor (JFET) input single op-amp	Buffers the common-mode output of the AD1937 codec for distribution to the analog filters. This signal is the bias reference voltage for the ADA4841-2 amplifiers, which have a single ended supply voltage.
U5	ADM811MARTZ reset voltage supervisor	Generates a master reset signal for the ADAU1467 and the AD1937 if the RESET push-button (S1) is pressed, if SigmaStudio sends a reset command via the USBi, or if the unregulated 5 V dc supply voltage drops below 3.08 V dc.
U7	74ACT04SC hexadecimal inverter	Buffers logic signals and drives status LEDs.
U8, U9, U11, U12 to U16	ADA4841-2 dual, low power, low noise, and low distortion rail-to-rail output amplifier	Implements the analog audio filtering required for the stereo line inputs and outputs.
U10	Microchip 25AA1024 serial EEPROM	Stores data, allowing the ADAU1467 to perform a self boot operation.
U17	ADP3338AKCZ-3.3-R7 or ADP3338AKCZ-3.3-RL7 3.3 V, dc LDO voltage regulator	Accepts the unregulated dc supply voltage between 5 V and 7 V that is provided to connector J16 and regulates the supply voltage down to 3.3 V.

STATUS LED DESCRIPTIONS

Table 6. LED Descriptions

Reference	Functional Name	Description
D1	SDP master	Not used.
D2	SDP slave	Not used.
D3	Self boot status LED	Illuminates when the self boot switch (Position 1 of Switch S3) is set to the on position, signifying that a self boot operation is to be executed on the rising edge of the ADAU1467 $\overline{\text{RESET}}$ signal or when the ADAU1467 is powered up. LED D3 does not illuminate when the self boot slide switch is set to off, which signifies that no self boot operations is to occur.
D4	$\overline{\text{RESET}}$	Illuminates when the master reset signal being generated by U5 is asserted low. This occurs when the supply voltage IOVDD drops below 3.08 V, when reset is asserted by the USBi from within the SigmaStudio software, or when the reset switch (S1) is pressed.
D5	USB_$\overline{\text{RESET}}$	USB_$\overline{\text{RESET}}$ illuminates when reset is asserted by the USBi from within the SigmaStudio software.
D6	Mic canvas header microphone power status	Illuminates when power for the microphones is supplied to the mic canvas connector.
D7	MP14	Not used.
D8	USBi connected	Illuminates when the USBi is recognized by Windows after the USBi is connected to the Control Port J1 and the USB port of the computer.
D9	3.3 V supply status LED	Illuminates when the output of the ADP3338AKZXZ3.3 or ADP3338AKZXZ3.3-R7 LDO voltage regulator has reached a level sufficient to exceed the V_{IH} logic high level input of the 74ACT04SC inverter. (When this LED is illuminated, it does not guarantee that the LDO voltage output is 3.3 V. It only shows that the LDO is about 2 V or greater. To perform a more detailed measurement of the LDO output level, measure the voltage on the 3V3_A test point.)

EVALUATION BOARD SCHEMATICS AND ARTWORK

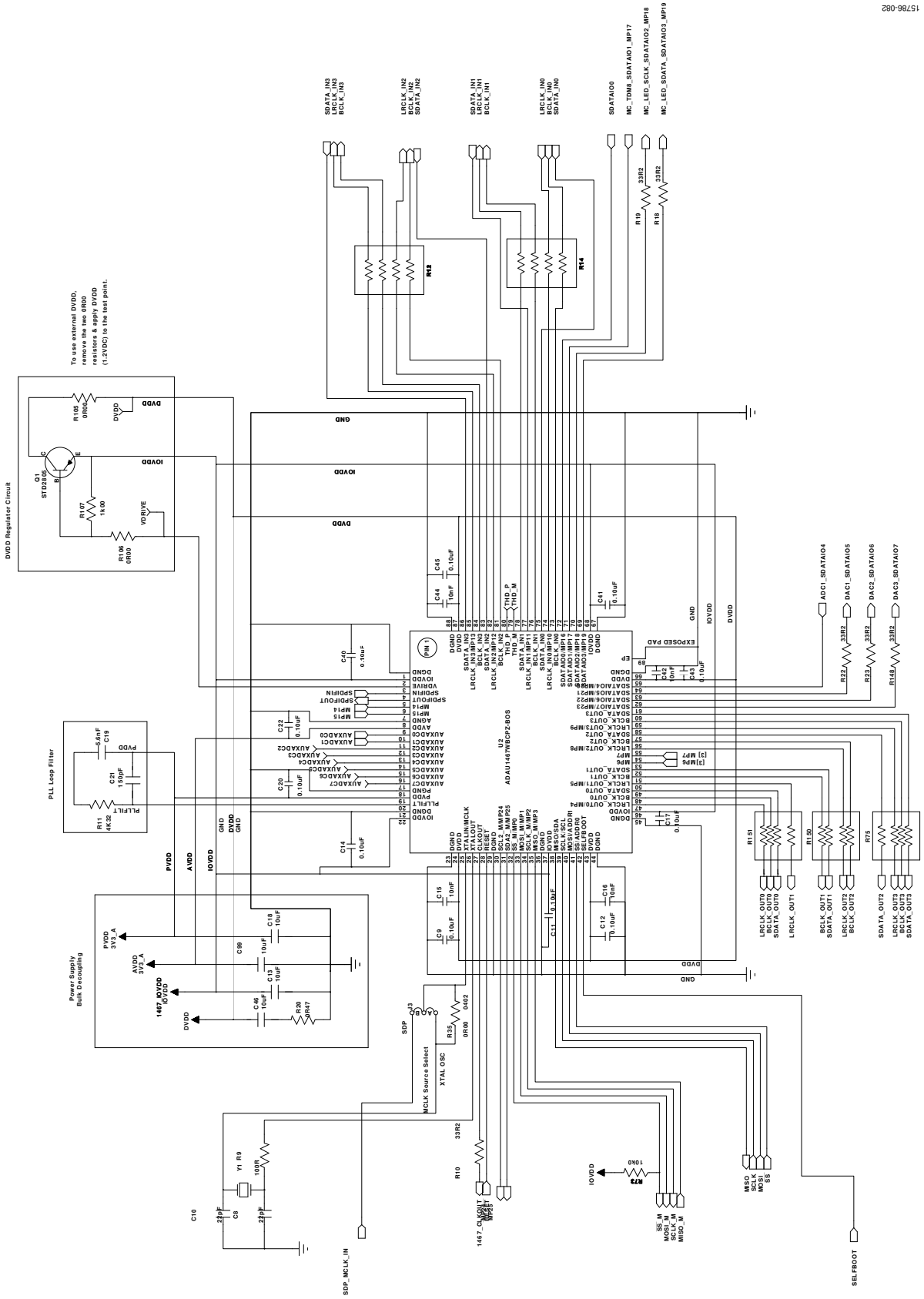


Figure 81. SigmaDSP Audio Processor Schematic

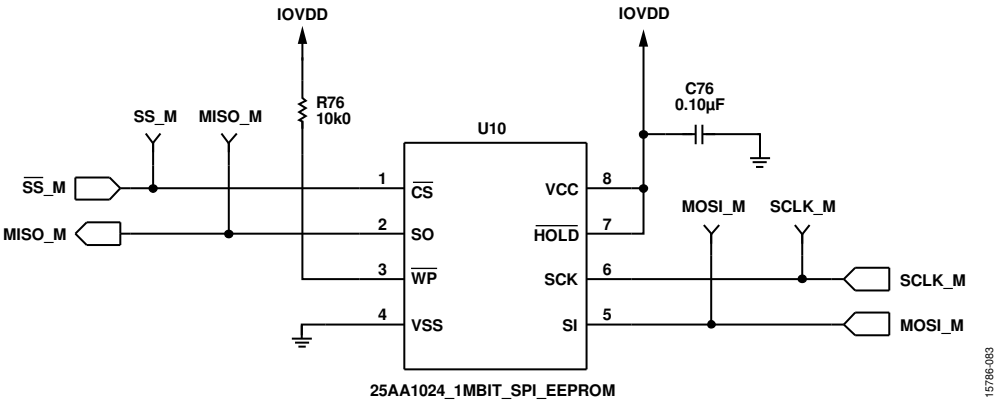


Figure 82. Analog Common-Mode Bias Reference Schematic

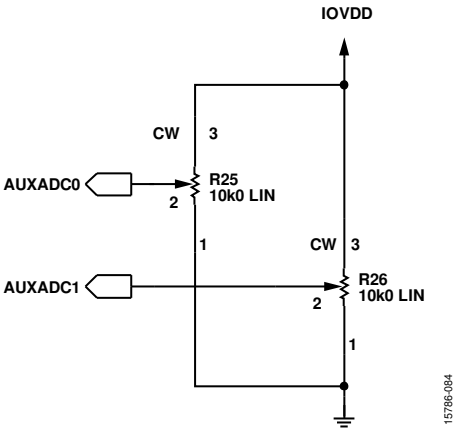


Figure 83. AUXADCx Potentiometer Schematic

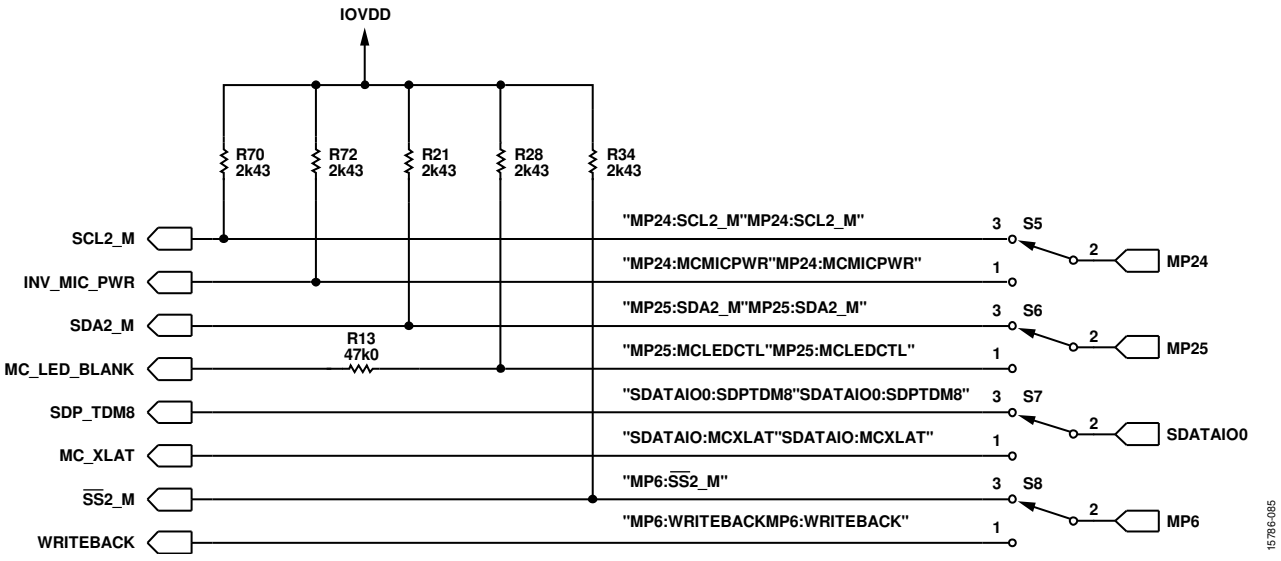


Figure 84. Configuration Option Switches Schematic

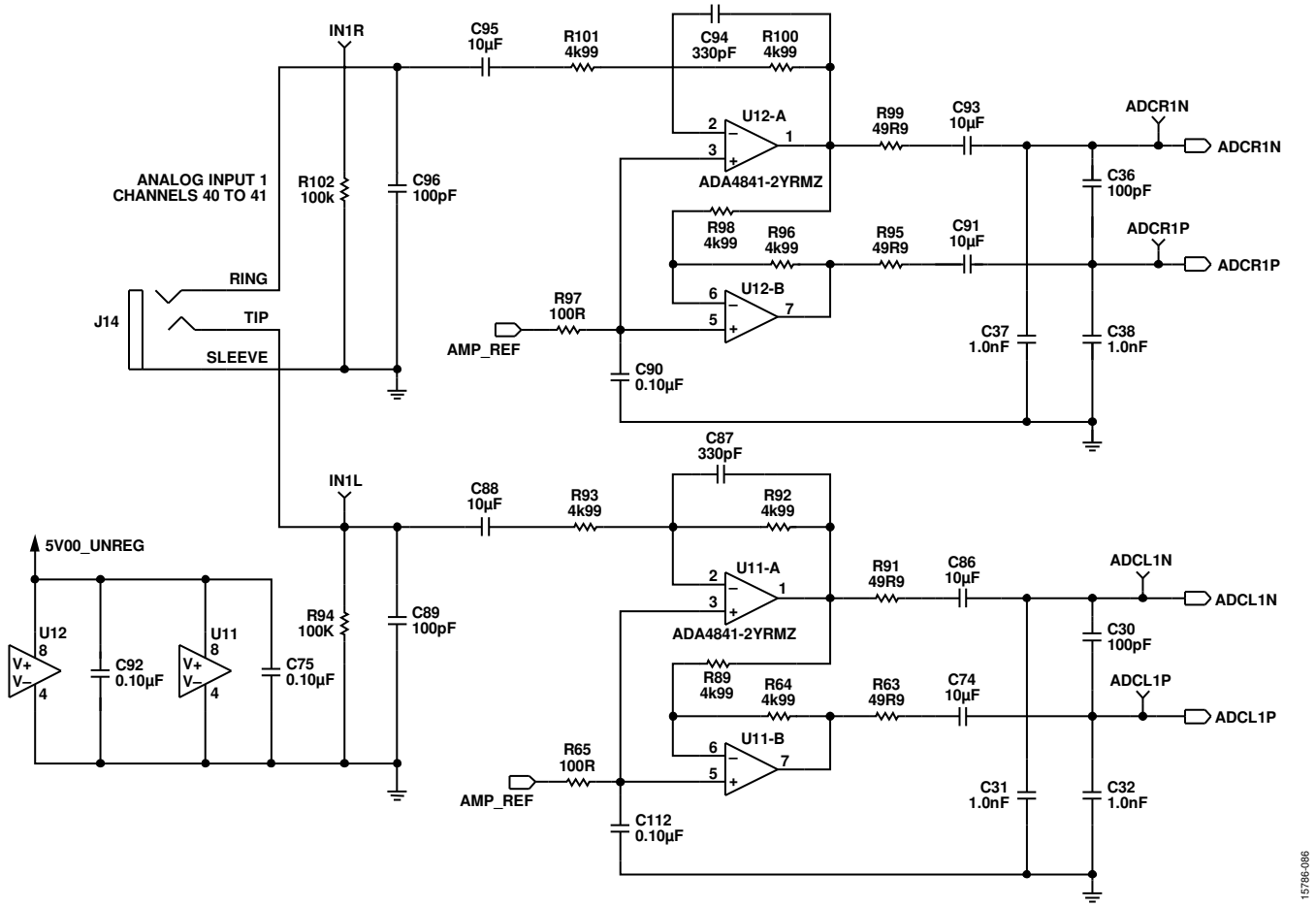


Figure 85. Analog Audio Input 1—Channel 40 to Channel 41 Schematic

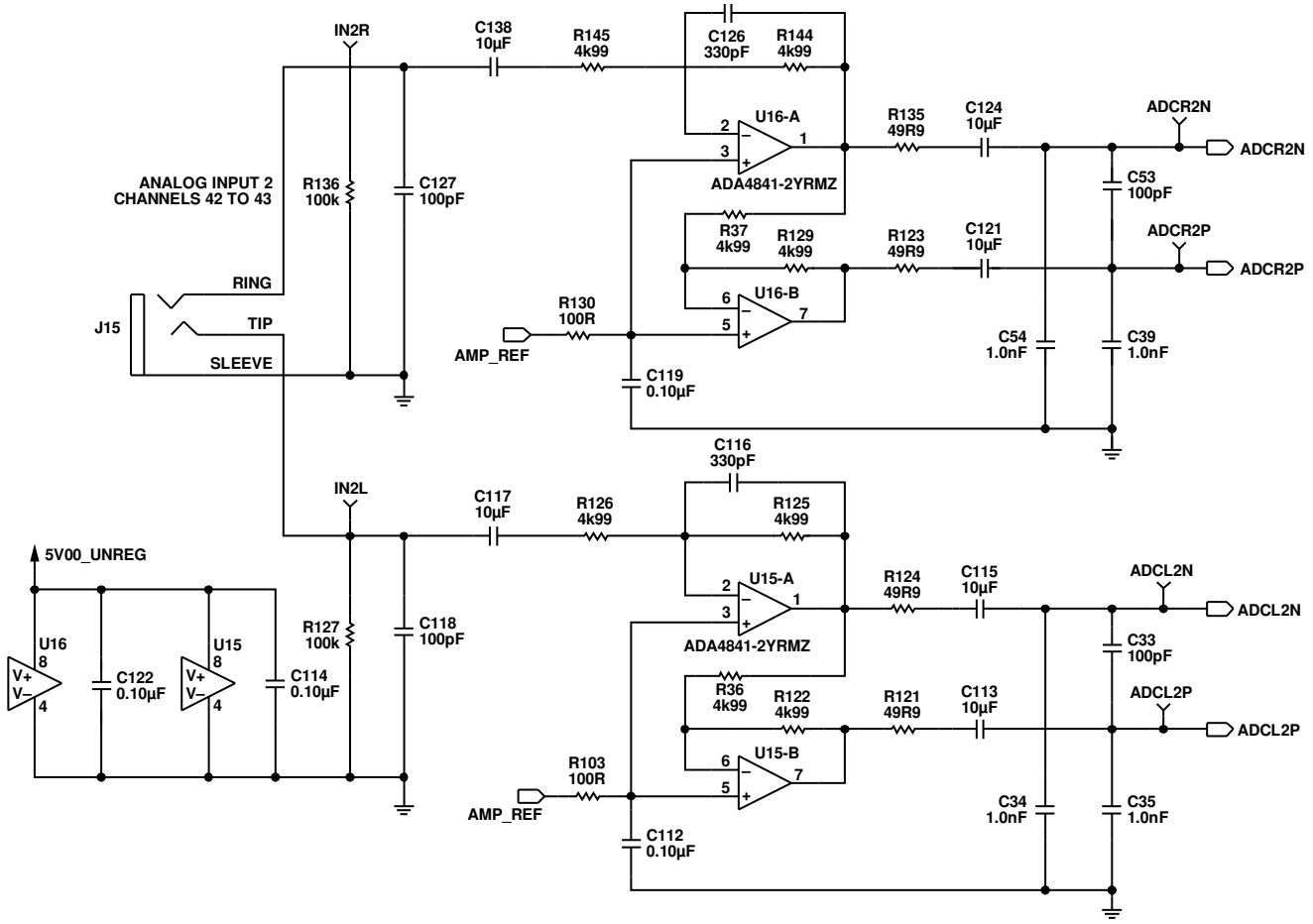


Figure 86. Analog Audio Input 2—Channel 42 to Channel 43 Schematic

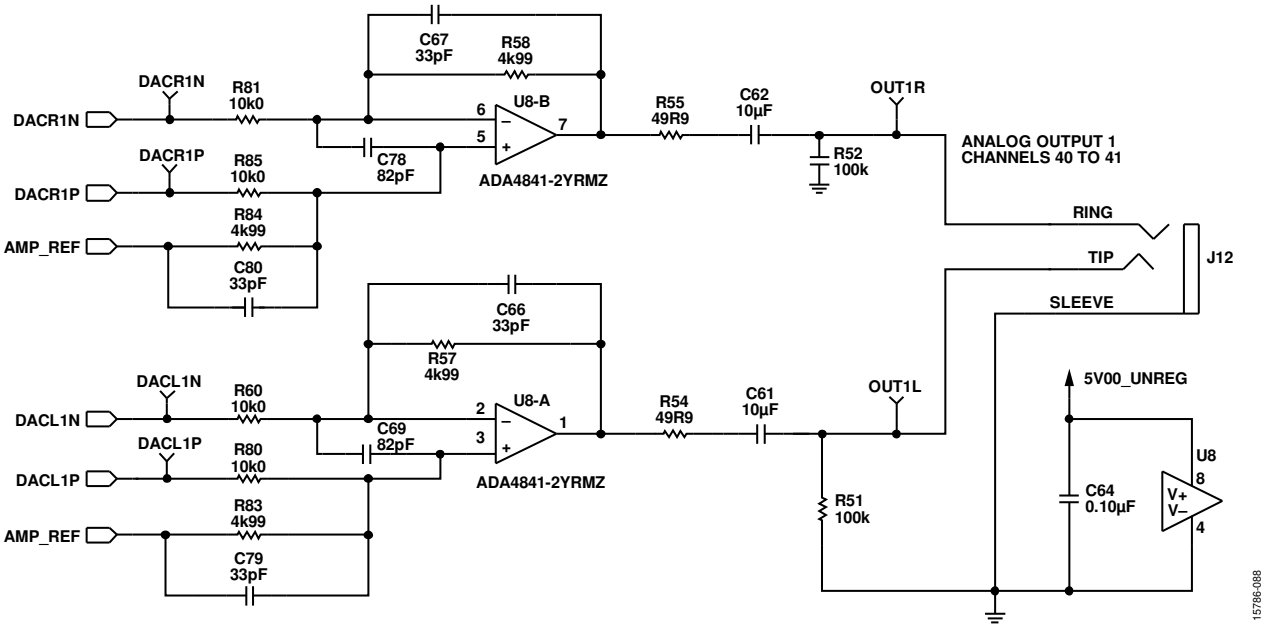


Figure 87. Analog Audio Output 1—Channel 40 to Channel 41 Schematic

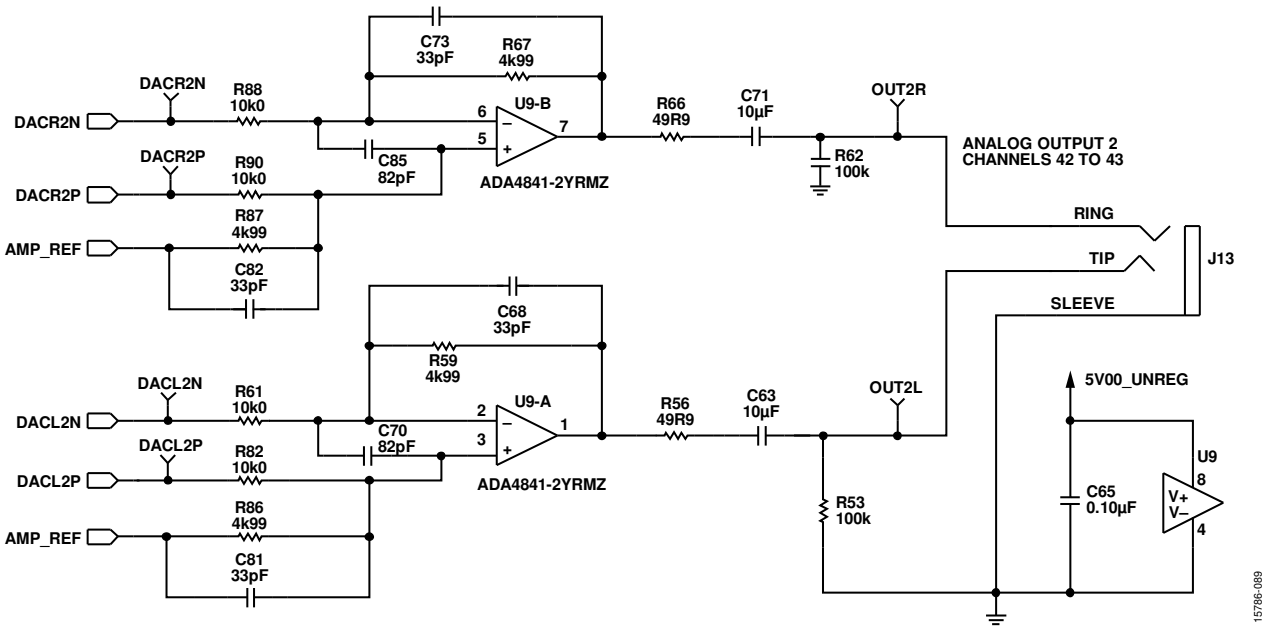


Figure 88. Analog Audio Output 2—Channel 42 to Channel 43 Schematic

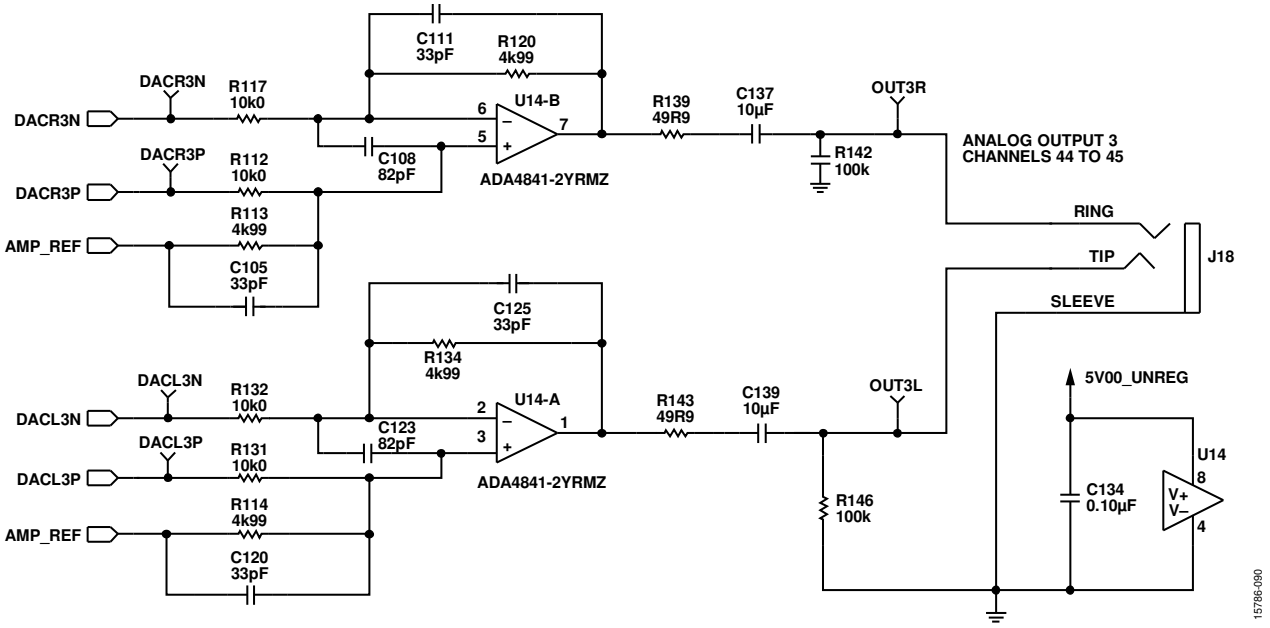


Figure 89. Analog Audio Output 3—Channel 44 to Channel 45 Schematic

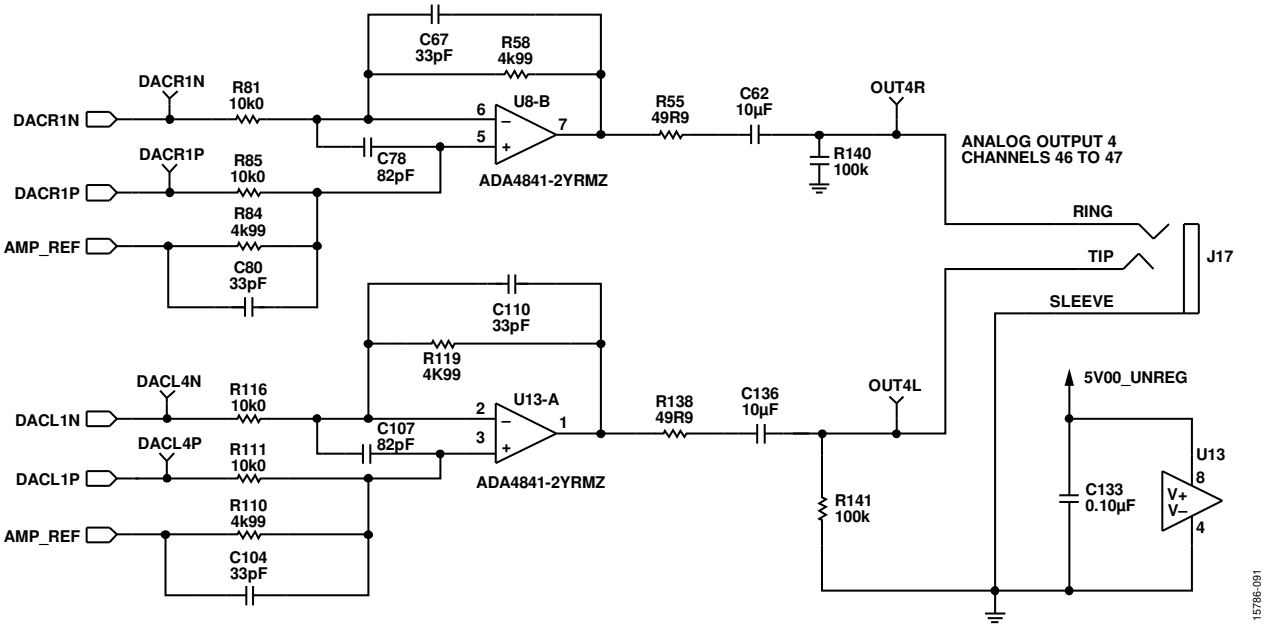


Figure 90. Analog Audio Output 2—Channel 46 to Channel 47 Schematic

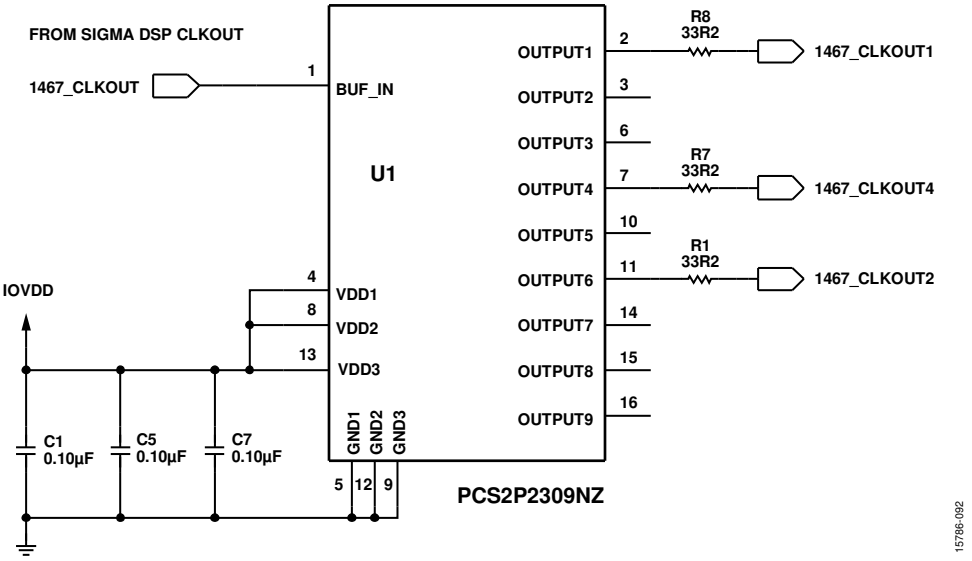


Figure 91. Master Clock Distribution Schematic

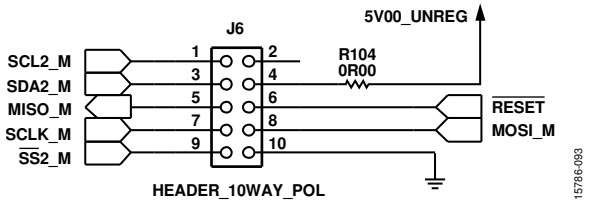


Figure 92. Master Control Port Output Header Schematic

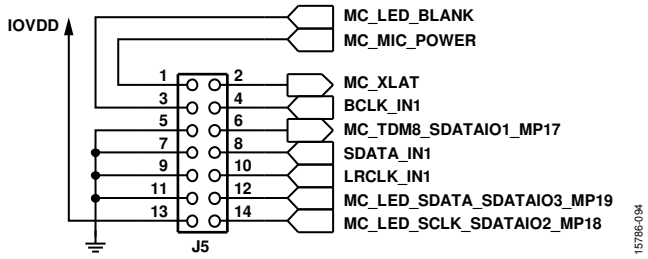


Figure 93. Microphone Canvas Header Schematic

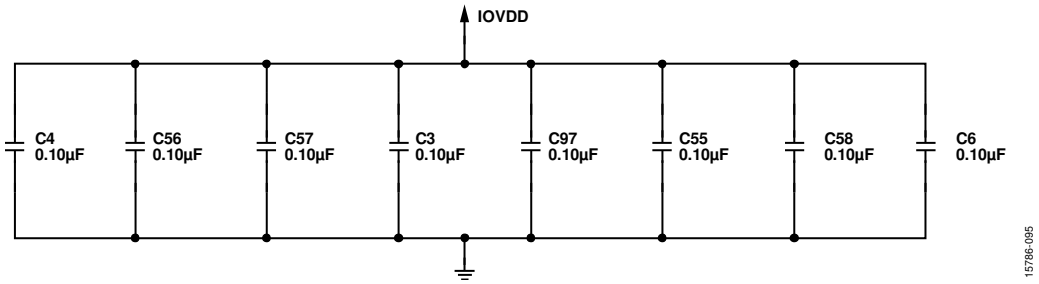


Figure 94. Plane Stitching Bypass Capacitor Schematic

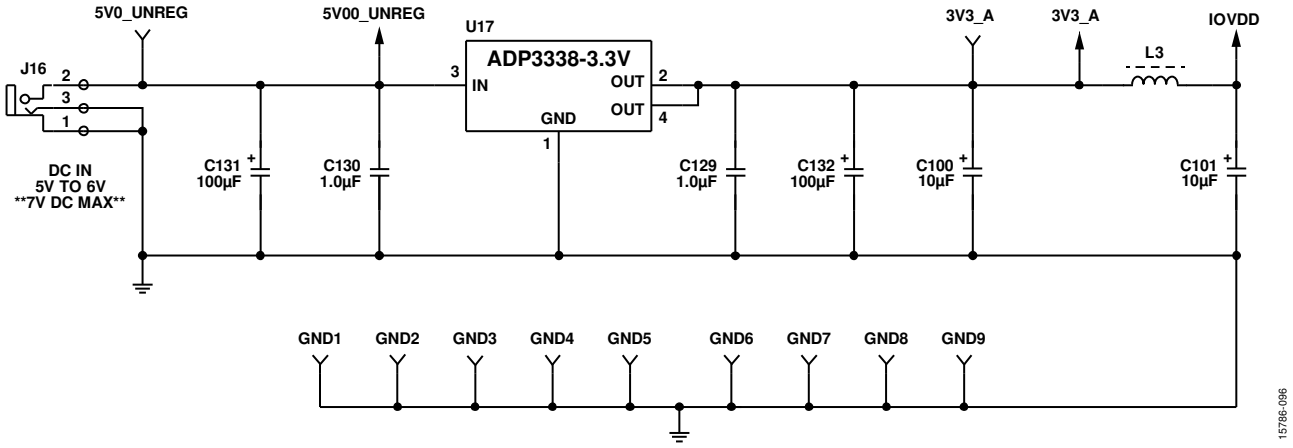


Figure 95. Power Supply Schematic

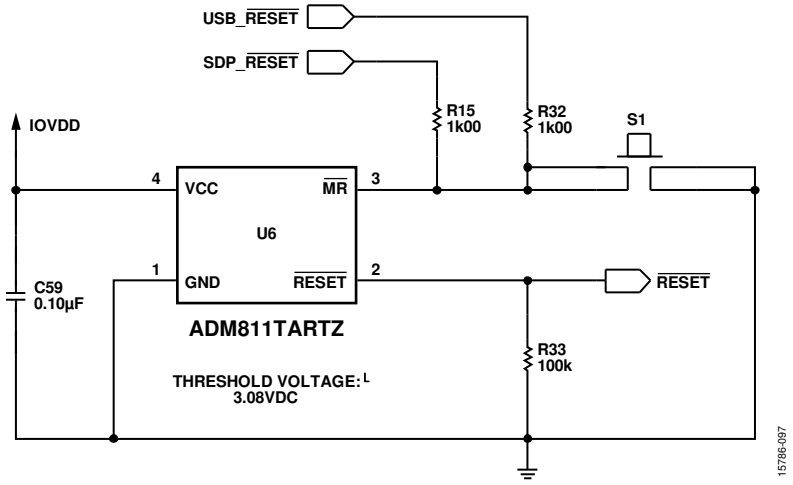


Figure 96. Reset Generator and Control Schematic

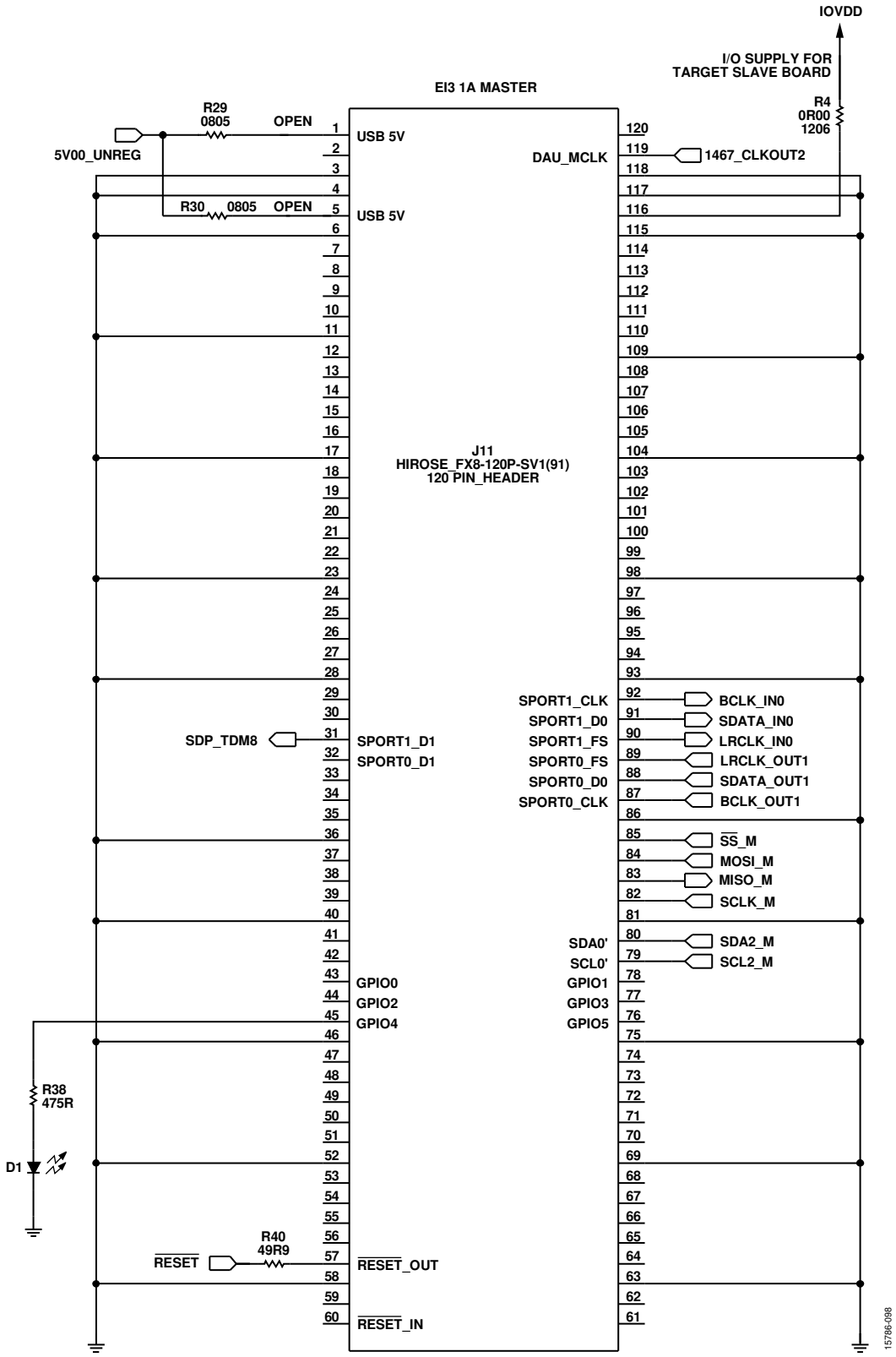


Figure 97. SDP-EI3 Connector—Master Output to a Target Slave Board Schematic

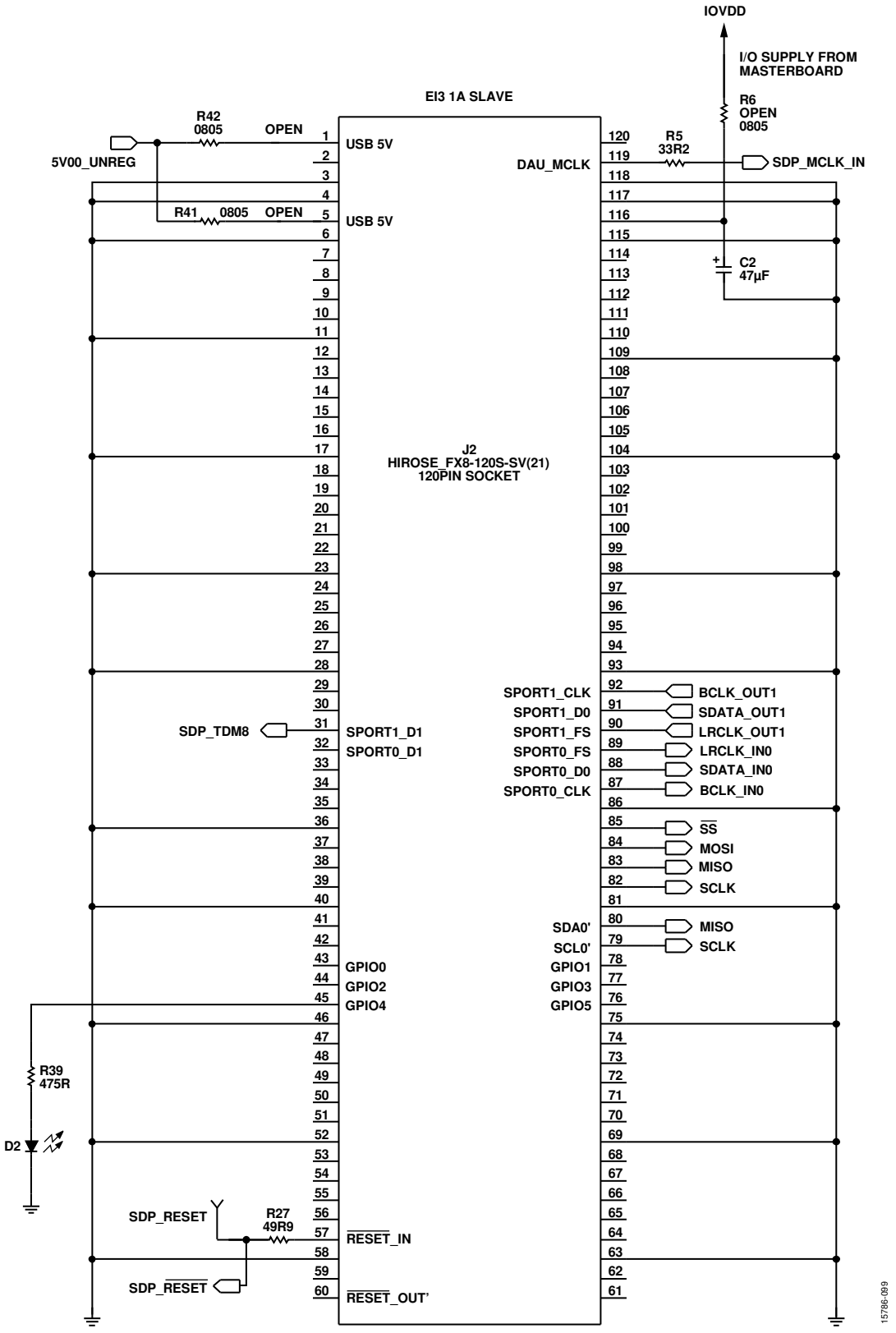


Figure 98. SDP-EI3 Connector—Slave Input from a Master Controller Board Schematic

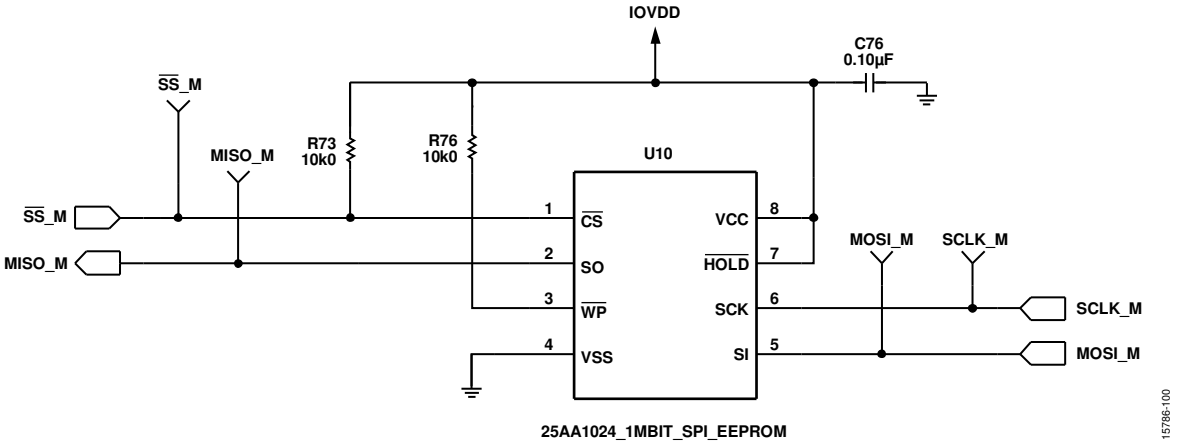


Figure 99. Self Boot SPI Memory Schematic

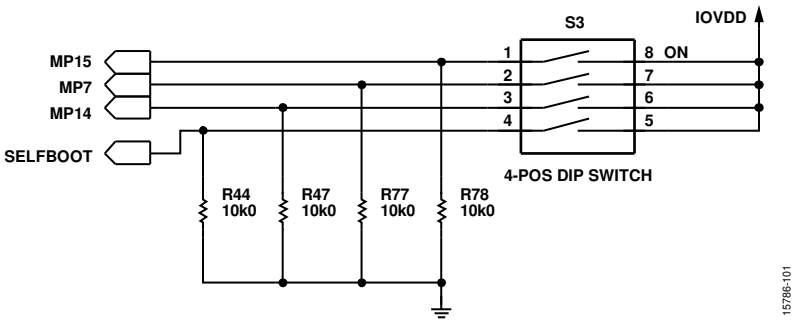


Figure 100. Self-Boot, MP15, MP7, and MP14 DIP Switch Schematic

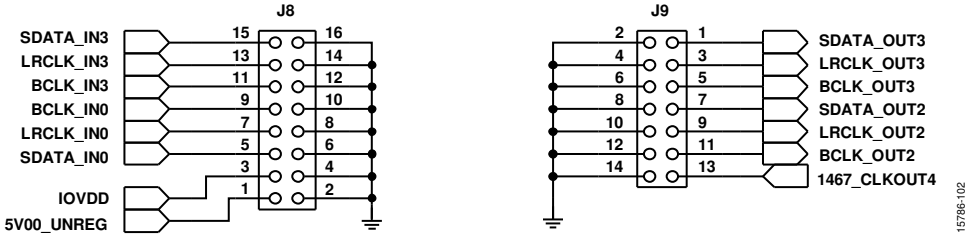


Figure 101. Serial Port Header Schematic

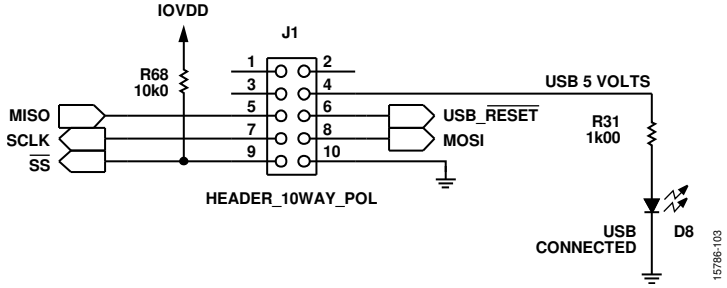


Figure 102. Slave Control Port Input Header (USBi) Schematic

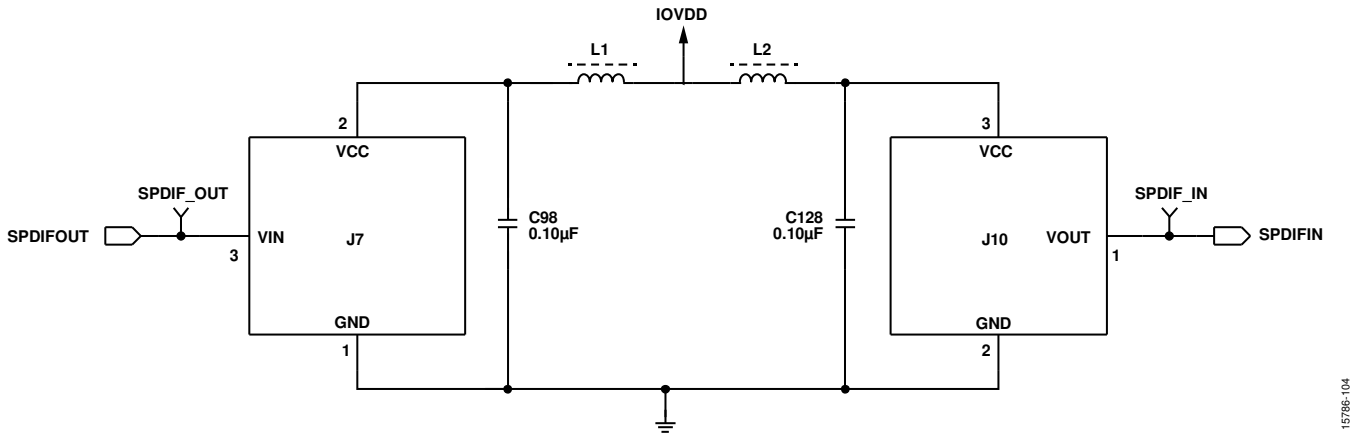


Figure 103. TOSLINK Optical Input/Output Connector Schematic

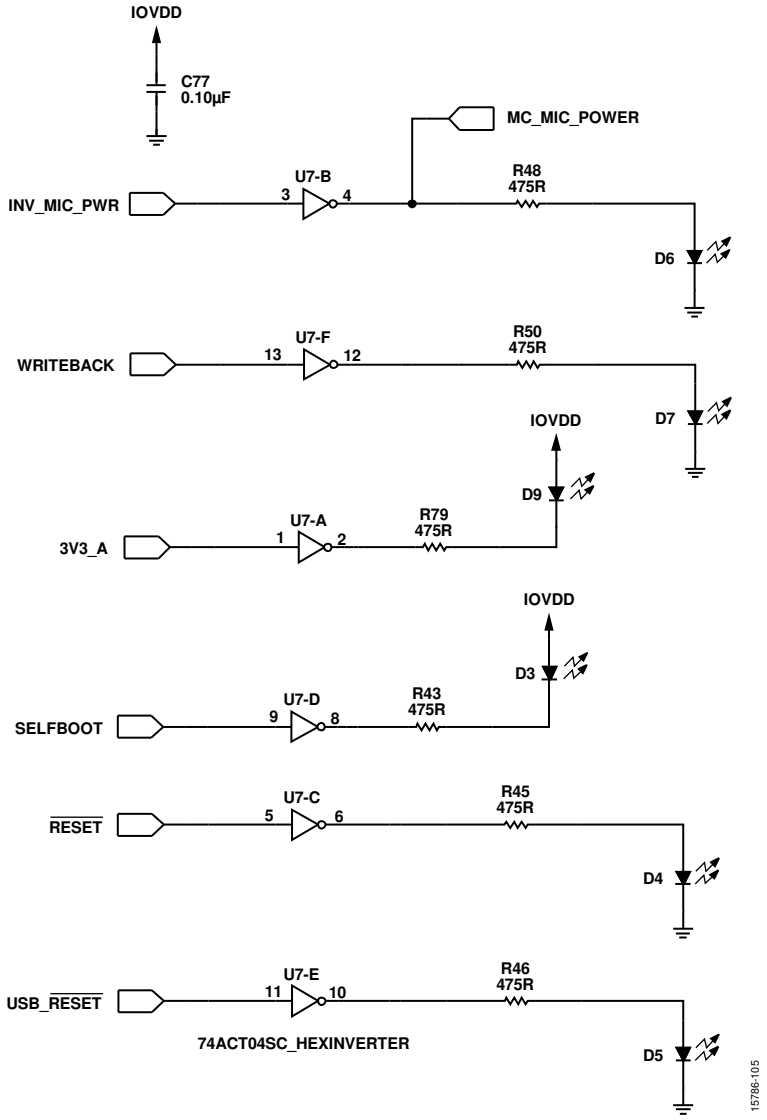


Figure 104. Status LEDs and Inverter Schematic

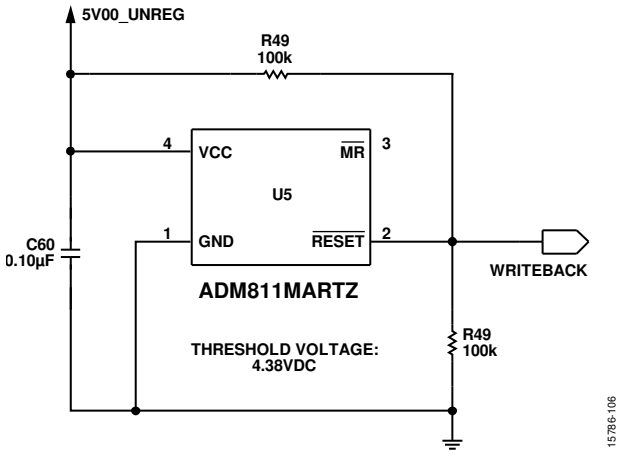


Figure 105. Write Back Trigger Schematic

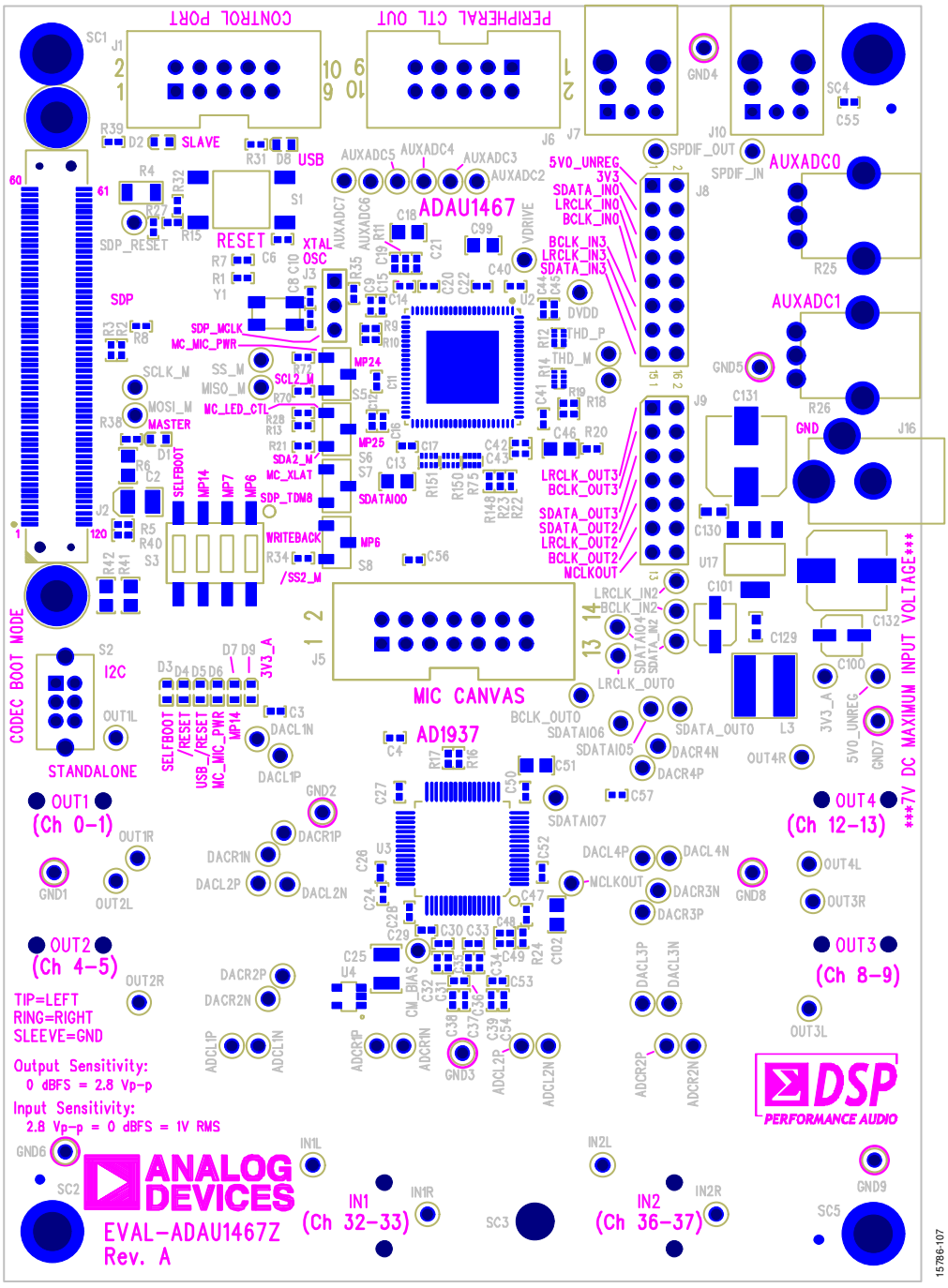


Figure 106. EVAL-ADAU1467Z Layout, Top Assembly and Silkscreen

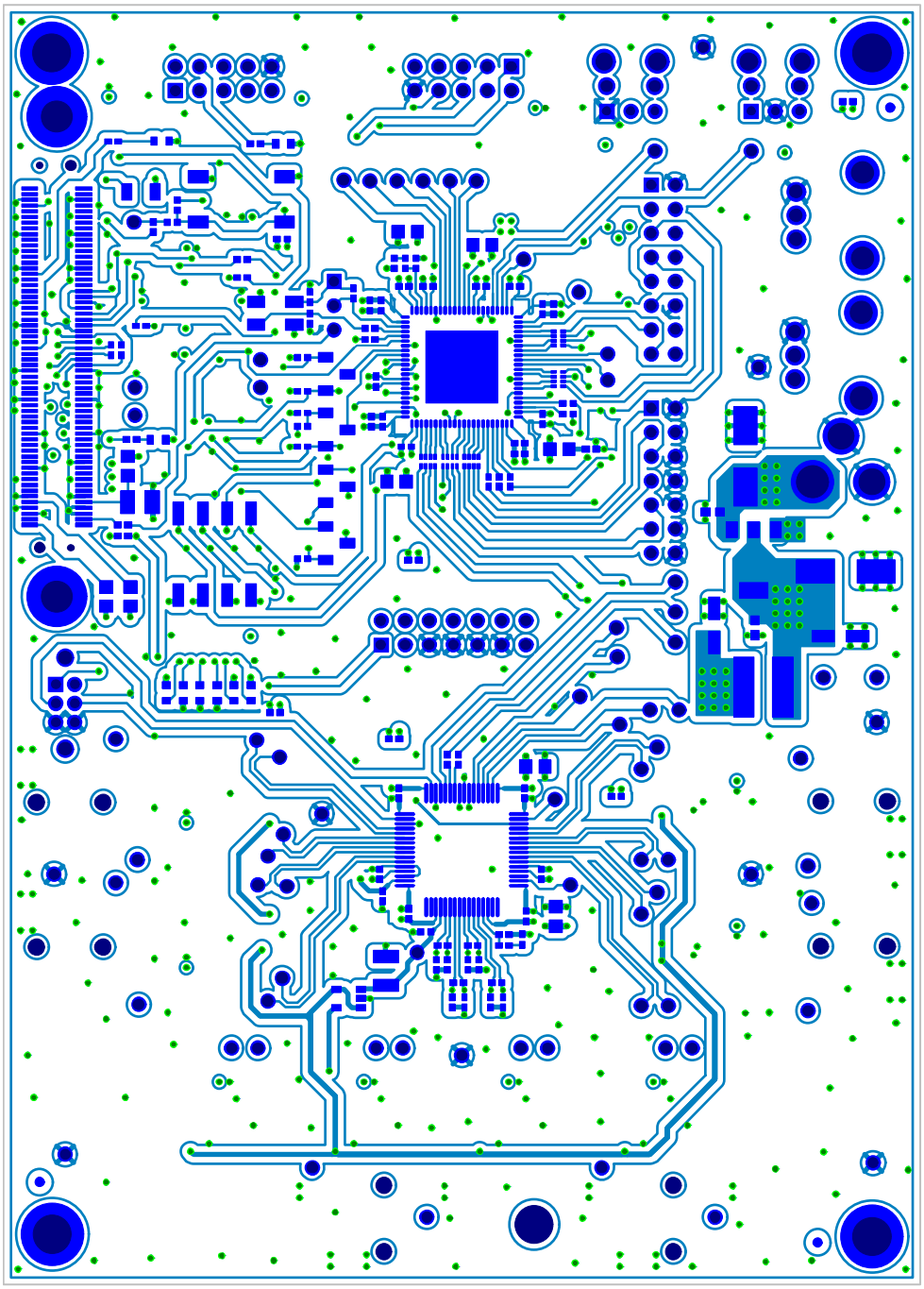


Figure 107. EVAL-ADAU1467ZLayout, Top Copper

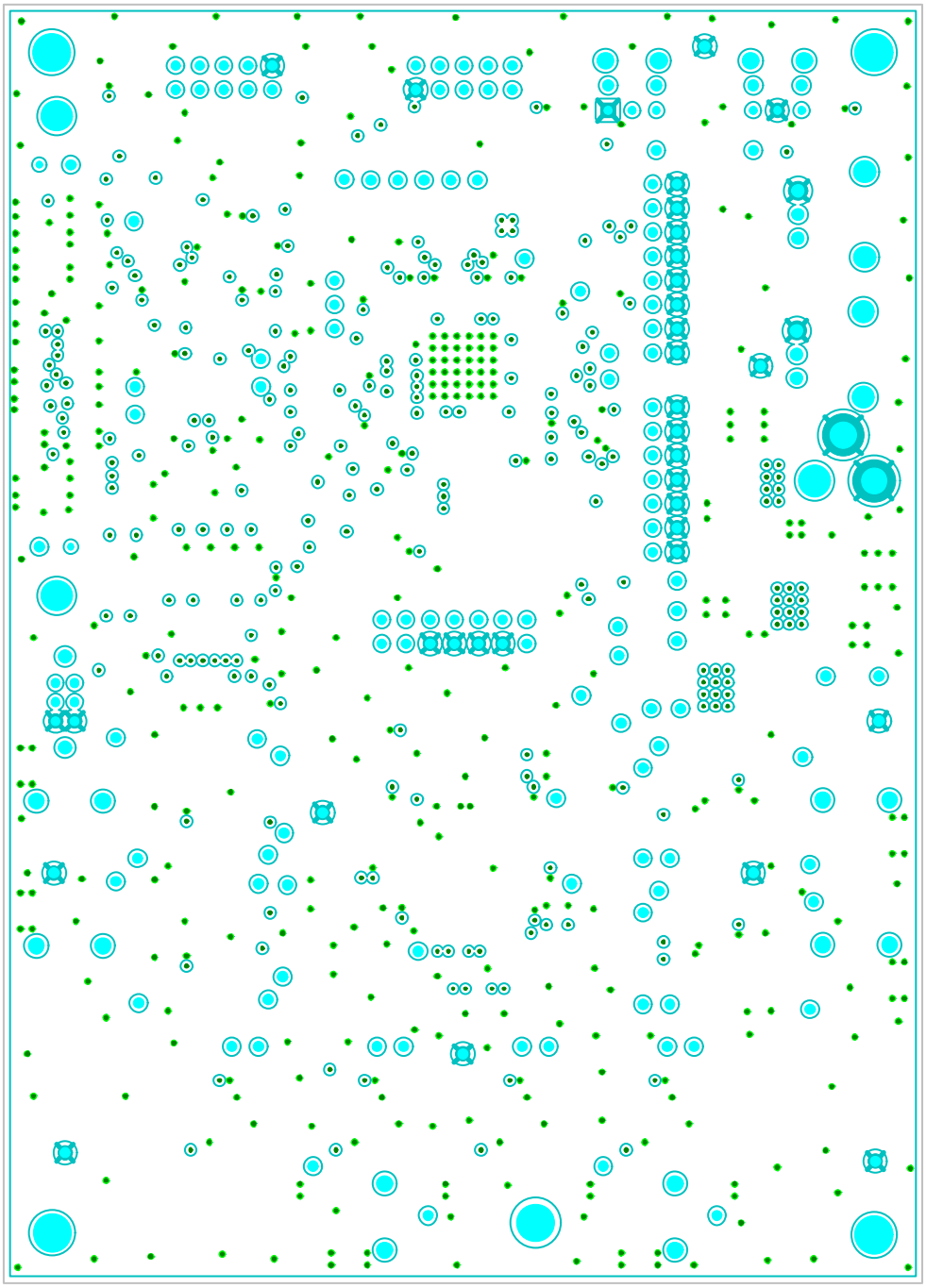


Figure 108. EVAL-ADAU1467Z Layout, Layer 2 (Ground)

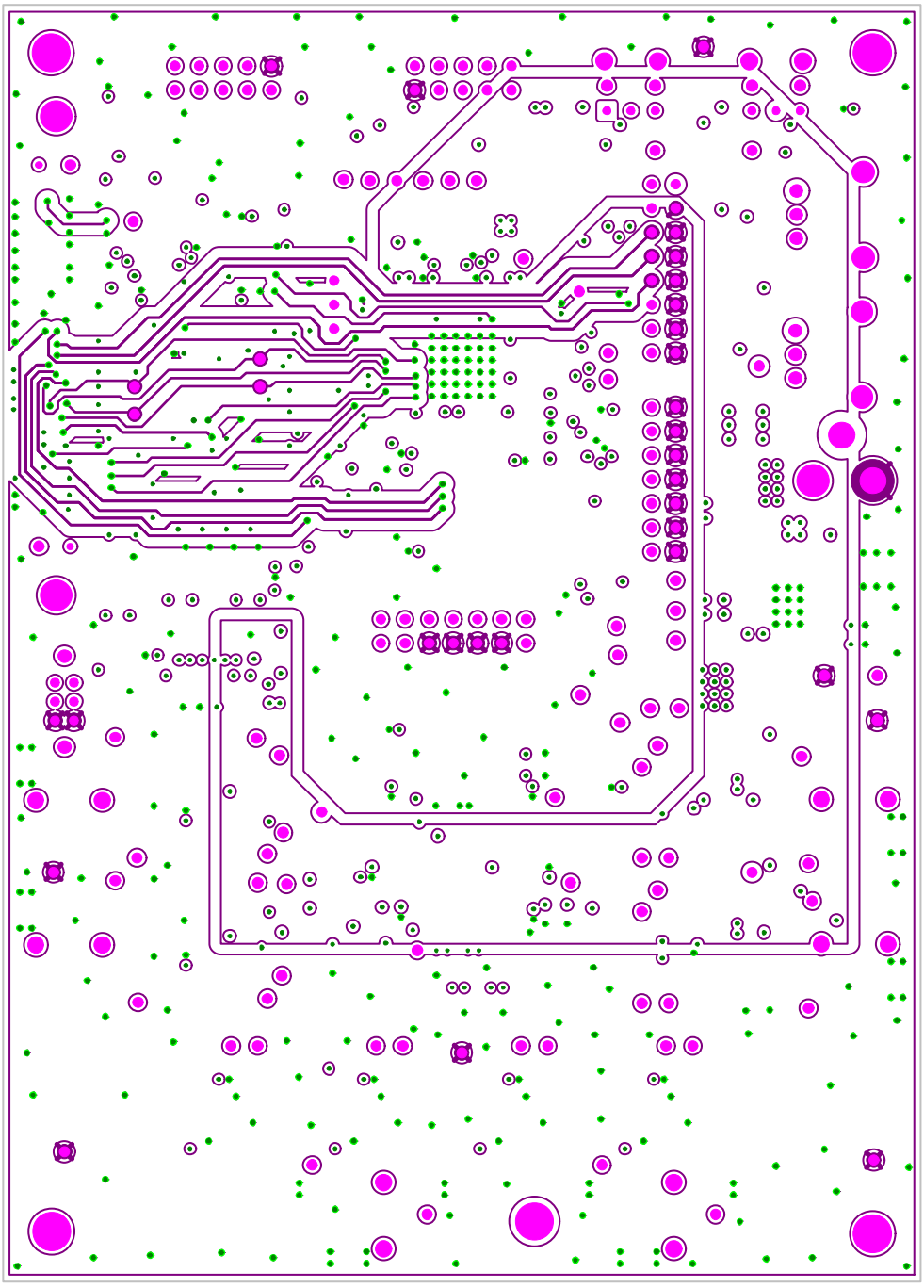


Figure 109. EVAL-ADAU1467Z Layout, Layer 3 (Signal/Power)

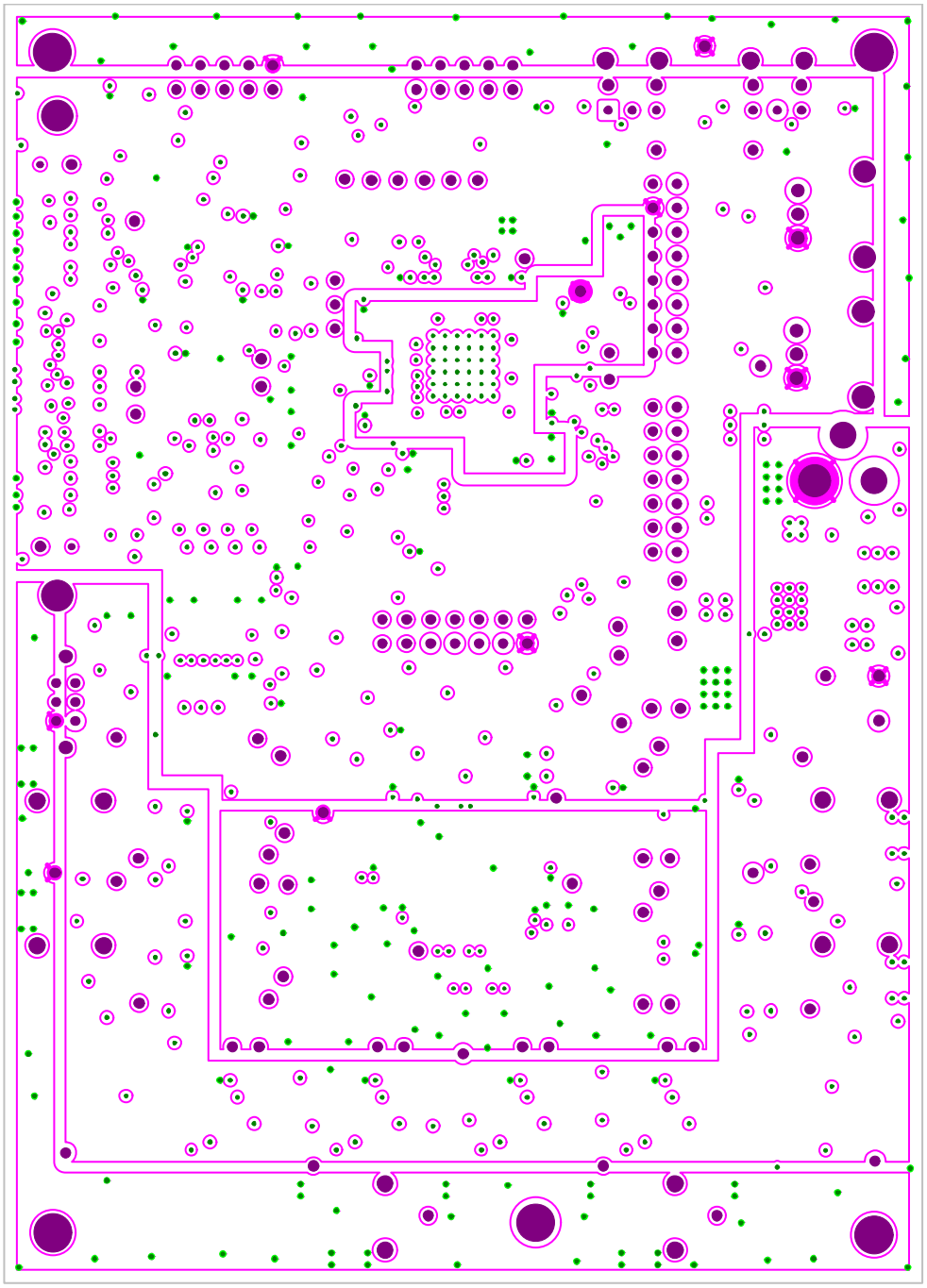


Figure 110. EVAL-ADAU1467Z Layout, Layer 4 (Power)

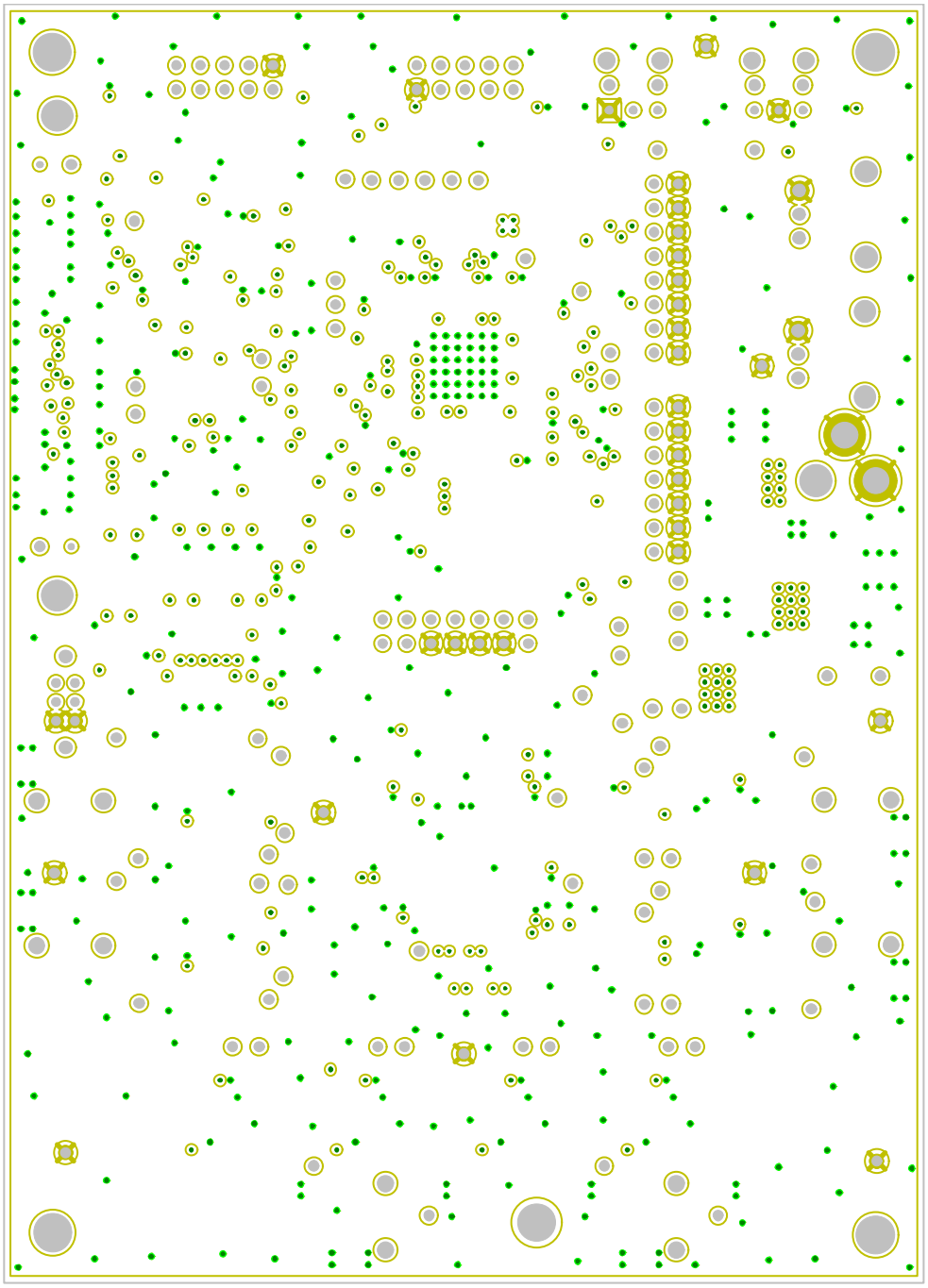


Figure 111. EVAL-ADAU1467Z Layout, Layer 5 (Ground)

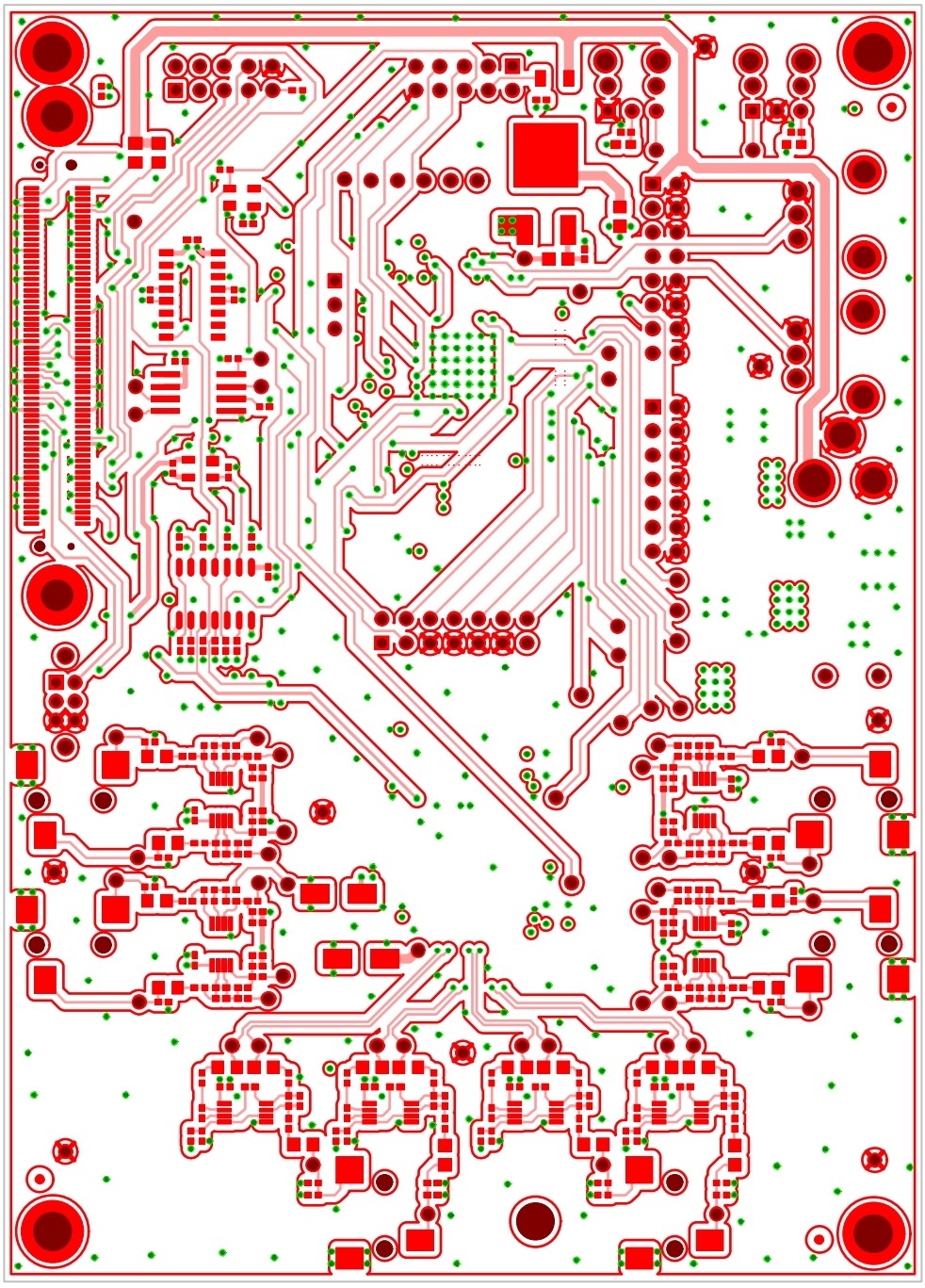


Figure 112. EVAL-ADAU1467Z Layout, Bottom Copper

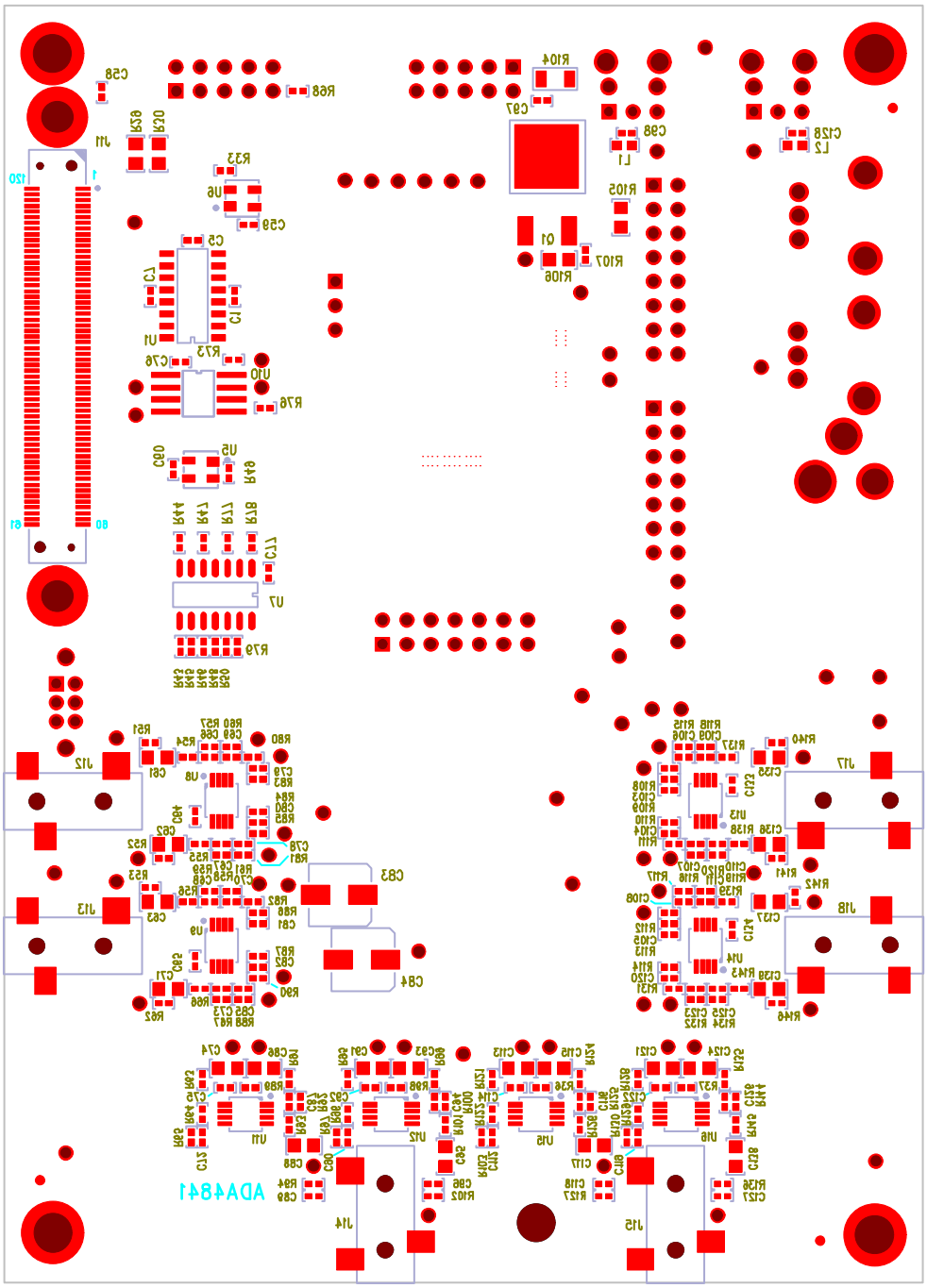


Figure 113. EVAL-ADAU1467Z Layout, Bottom Assembly (Viewed from Above)

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Qty	Reference Designator	Description	Manufacturer	Part Number
48	C1, C3 to C7, C9, C11, C12, C14, C17, C20, C22, C24, C26, C27 to C29, C40, C41, C43, C45, C47, C50, C52, C55 to C60, C64, C65, C72, C75 to C77, C90, C92, C97, C98, C112, C114, C119, C122, C128, C133, C134	Multilayer ceramic capacitors, 16 V, X7R (0402), 0.10 µF	Murata ENA	GRM155R71C104KA88D
2	C100, C101	Aluminum electrolytic capacitors, 105°C, SMD_B, 10 µF	Panasonic EC	EEE-FC1C100R
2	C129, C130	Multilayer ceramic capacitors, 16 V, X7R (0603), 1.0 µF	Murata ENA	GRM188R71C105KA12D
26	C13, C18, C46, C51, C61 to C63, C71, C74, C86, C88, C91, C93, C95, C99, C102, C113, C115, C117, C121, C124, C135 to C139	Multilayer ceramic capacitors, 10 V, X7R (0805), 10 µF	Murata ENA	GRM21BR71A106KE51L
2	C131, C132	Aluminum electrolytic capacitors, 105°C, 100 µF	Panasonic EC	EEE-FC1C101P
4	C15, C16, C42, C44	Multilayer ceramic capacitors, 25 V, X7R (0402), 10 nF	Murata	GRM155R71E103JA01J
2	C19, C49	Multilayer ceramic capacitors, 25 V, NP0 (0402), 5.6 nF	Murata	GRM155R71E562KA01D
1	C2	Tantalum capacitor, 105°C, 47 µF	Kemet	T520B476M010ATE035
1	C21	Multilayer ceramic capacitor, 50 V, NP0 (0402), 150 pF	Murata ENA	GRM1555C1H151JA01D
1	C25	Ceramic capacitor, 6.3 V, X7R, 1210, 47.0 µF	Murata	GCM32ER70J476KE19L
8	C30, C33, C36, C53, C89, C96, C118, C127	Multilayer ceramic capacitors, 50 V, NP0 (0402), 100 pF	Murata ENA	GRM1555C1H101JA01D
8	C31, C32, C34, C35, C37 to C39, C54	Multilayer ceramic capacitors, 50 V, NP0 (0402), 1.0 nF	Murata ENA	GRM1555C1H102JA01D
1	C48	Multilayer ceramic capacitor, 50 V, NP0 (0402), 390 pF	Murata ENA	GRM1555C1H391JA01D
16	C66 to C68, C73, C79, C80 to C82, C103 to C105, C109 to C111, C120, C125	Multilayer ceramic capacitors, 50 V, NP0 (0402), 33 pF	Murata ENA	GRM1555C1H330JA01D
8	C69, C70, C78, C85, C106 to C108, C123	Multilayer ceramic capacitors, 50 V, NP0 (0402), 82 pF	Murata ENA	GRM1555C1H820JA01D
2	C8, C10	Multilayer ceramic capacitors, 50 V, NP0 (0402), 22 pF	Murata ENC	GRM1555C1H220JA01D
2	C83, C84	Aluminum electrolytic capacitors, FC, 105°C, SMD_D, 47 µF	Panasonic EC	EEE-FC1C470P
4	C87, C94, C116, C126	Multilayer ceramic capacitors, 50 V, NP0 (0402), 330 pF	Murata ENA	GRM1555C1H331JA01D
9	D1 to D9	LED, 3 millicandela, 571 nm, 0603, green	Lite-On	LTST-C191KGKT
2	J1, J6	10-way shroud polarized headers, 2 × 5	3M	N2510-6002RB
1	J10	TOSLINK, 16 Mpbs, optical receiver, PLR135/T10	Everlight Americas	PLR135/T10
1	J11	120-pin header, 0.6 mm	Hirose Electric	FX8-120P-SV1(91)
6	J12 to J15, J17, J18	Stereo mini jacks, SMT, SJ-3523-SMT	CUI Inc.	SJ-3523-SMT
1	J16	Mini power jack, 0.08 inch	Switchcraft Inc.	RAPC722X
1	J2	120-pin socket, 0.6 mm	Hirose Electric	FX8-120S-SV(21)

Qty	Reference Designator	Description	Manufacturer	Part Number
1	J3	3-position session initiation protocol (SIP) header, 3-jumper	Sullins	PBC03SAAN or cut PBC36SAAN
1	J5	14-way shroud polarized header, 2 × 7	3M	N2514-6002RB
1	J7	TOSLINK, 16 Mpbs, optical transmitter	Everlight Americas	PLT133/T10W
1	J8	16-way unshrouded, 2 × 8	3M	PBC08DAAN, or cut PBC36DAAN
1	J9	14-way unshrouded header, 2 × 7	3M	PBC07DAAN, or cut PBC36DAAN
2	L1, L2	47 µH inductor	Taiyo Yuden	CBMF1608T470K
1	L3	Inductor surface mount technology (SMT), 9.0 µH	Wurth Electronics Inc.	744052009
1	Q1	PNP transistor, D-PAK,	STMicroelectronics	STD2805T4
12	R1, R5, R7, R8, R10, R16 to R19, R22, R23, R148	Chip resistors ,1%, 63 mW, thick film 0402, 33.2 Ω	Stackpole	RMCF0402FT33R2
2	R105, R106	Chip resistors, 5%, 125 mW, thick film, 0805, 0.00 Ω	Panasonic EC	ERJ-6GEY0R00V
1	R11	Chip resistor, 1%, 100 mW, thick film ,0402, 4.32 kΩ	Panasonic ECG	ERJ-2RKF4321X
5	R12, R14, R75, R150, R151	Resistor network isolated, 4 resistors, 33R0	CTS Corp.	741X083330JP
1	R13	Chip resistor, 1%, 63 mW, thick film, 0402, 47.0 kΩ	Yageo	RC0402FR-0747K0L
4	R15, R31, R32, R107	Chip resistors, 1%, 63 mW, thick film, 0402, 1.0 kΩ	Yageo	RC0402FR-071KL
7	R2, R3, R6, R29, R30, R41, R42	Not applicable	Not applicable	Not applicable
1	R20	Chip resistor, 1%, 167 mW, thick film, 0402, 0.47 Ω	Panasonic ERJ	ERJ-2BQFR47X
5	R21, R28, R34, R70, R72	Chip resistors, 1%, 63 mW, thick film, 0402, 2.43 kΩ	Vishay/Dale	CRCW04022K43FKED
1	R24	Chip resistor, 1%, 63 mW, thick film, 0402, 562 Ω	Stackpole	RMCF0402FT562R
2	R25, R26	10.0 kΩ potentiometers, 9 mm, vertical, 10.0 kΩ linear taper	Panasonic EC	EVU-F2MFL3B14
18	R27, R40, R54 to R56, R63, R66, R91, R95, R99, R121, R124, R128, R135, R137 to R139, R143	Chip resistors, 1%, 63 mW, thick film, 0402, 49.9 Ω	Yageo	RC0402FR-0749R9L
14	R33, R49, R51 to R53, R62, R94, R102, R127, R136, R140, R141, R142, R146	Chip resistors, 1%, 100 mW, thick film, 0402, 100 k	Panasonic ECG	ERJ-2RKF1003X
1	R35	Chip resistor, 5%, 100 mW, thick film, 0402, 0.00 Ω	Panasonic ECG	ERJ-2GE0R00X
32	R36, R37, R57 to R59, R64, R67, R83, R84, R86 to R89, R92, R93, R96, R98, R100, R101, R109, R110, R113, R114, R118 to R120, R122, R125, R126, R129, R134, R144, R145	Chip resistors, 1%, 63 mW, thick film, 0402, 4.99 kΩ	Stackpole	RMCF0402FT4K99
8	R38, R39, R43, R45, R46, R48, R50, R79	Chip resistors, 1%, 63 mW, thick film, 0402, 475 Ω	Stackpole	RMCF0402FT475R
2	R4, R104	Chip resistors, 5%, 250 mW, thick film, 1206, 0.00 Ω	Panasonic EC	ERJ-8GEY0R00V
23	R44, R47, R60, R61, R68, R73, R76 to R78, R80 to R82, R85, R88, R90, R108, R111, R112, R115 to R117, R131, R132	Chip resistors, 1%, 100 mW, thick film, 0402, 10.0 kΩ	Panasonic ECG	ERJ-2RKF1002X
5	R9, R65, R97, R103, R130	Chip resistors, 1%, 63 mW, thick film, 0402, 100 Ω	Yageo	RC0402FR-07100RL
1	S1	Tactile switch, 6 mm, gull wing, SPST-NO	Tyco/Alcoswitch	FSM6JSMA

Qty	Reference Designator	Description	Manufacturer	Part Number
1	S2	Double-pole, double-throw (DPDT) slide switch, DPDT slide	E-Switch	EG2207
1	S3	4 section SPST SMD switch raised act, 4× SPST	CTS Corp	219-4MST
4	S5 to S8	Single-pole, double-throw (SPDT) slide switches, SMD J hook, SPDT	Copal Electronics	CAS-120TA
1	U1	IC clock buffer 1:9, 16-lead SOIC	On Semiconductor	PCS2I2309NZG16SR
1	U10	SPI EEPROM, 128k × 8 (1 Mbit), 20 MHz	Microchip	25AA1024-I/SM
1	U17	High accuracy, low dropout, 3.3 V dc voltage regulator	Analog Devices	ADP3338AKCZ-3.3-R7
1	U2	300 MHz, SigmaDSP	Analog Devices	ADAU1467WBCPZ
1	U3	4 ADC/8 DAC with phase-locked loop (PLL), 192 kHz, 24-bit codec	Analog Devices	AD1937WBSTZ
1	U4	JFET input, single op amp, SOT-23,	Analog Devices	ADA4610-1ARJZ
1	U5	Microprocessor voltage supervisor, logic low reset output	Analog Devices	ADM811MARTZ-REEL7
1	U6	Microprocessor voltage supervisor, logic low reset output	Analog Devices	ADM811TARTZ-REEL7
1	U7	IC inverter HEX 14-SOIC, 74ACT04SC	Fairchild Semi	74ACT04SC
8	U8, U9, U11 to U16	Dual low power, low noise, and distortion rail-to-rail output amplifiers	Analog Devices	ADA4841-2YRMZ
1	Y1	Crystal, 12.288 MHz, 18 pF	Abracon Corp	ABM3B-12.288MHZ-10-1-U-T
48	C1, C3 to C7, C9, C11, C12, C14, C17, C20, C22, C24, C26 to C29, C40, C41, C43, C45, C47, C50, C52, C55 to C60, C64, C65, C72, C75 to C77, C90, C92, C97, C98, C112, C114, C119, C122, C128, C133, C134	Multilayer ceramic capacitors, 16 V, X7R (0402), 0.10 µF	Murata ENA	GRM155R71C104KA88D
2	C100, C101	Aluminum electrolytic capacitors, 105°C, SMD_B, 10 µF	Panasonic EC	EEE-FC1C100R
2	C129, C130	Multilayer ceramic capacitors, 16 V, X7R (0603), 1.0 µF	Murata ENA	GRM188R71C105KA12D
26	C13, C18, C46, C51, C61 to C63, C71, C74, C86, C88, C91, C93, C95, C99, C102, C113, C115, C117, C121, C124, C135 to C139	Multilayer ceramic capacitors, 10 V, X7R (0805), 10 µF	Murata ENA	GRM21BR71A106KE51L
2	C131, C132	Aluminum electrolytic capacitors, 105°C, 100 µF	Panasonic EC	EEE-FC1C101P
4	C15, C16, C42, C44	Multilayer ceramic, capacitors 25 V, X7R (0402), 10 nF	Murata	GRM155R71E103JA01J
2	C19, C49	Multilayer ceramic capacitors, 25 V, NP0 (0402), 5.6 nF	Murata	GRM155R71E562KA01D
1	C2	Tantalum capacitor, 105°C, 47 µF	Kemet	T520B476M010ATE035
1	C21	Multilayer ceramic, 50 V, NP0 (0402), 150 pF	Murata ENA	GRM1555C1H151JA01D
1	C25	Ceramic capacitor, 6.3 V, X7R 1210, 47.0 µF	Murata	GCM32ER70J476KE19L
8	C30, C33, C36, C53, C89, C96, C118, C127	Multilayer ceramic capacitors, 50 V, NP0 (0402), 100 pF	Murata ENA	GRM1555C1H101JA01D
8	C31, C32, C34, C35, C37 to C39, C54	Multilayer ceramic capacitors, 50 V, NP0 (0402), 1.0 nF	Murata ENA	GRM1555C1H102JA01D
1	C48	Multilayer ceramic capacitor, 50 V, NP0 (0402), 390 pF	Murata ENA	GRM1555C1H391JA01D
16	C66 to C68, C73, C79 to C82, C103 to C105, C109 to C111, C120, C125	Multilayer ceramic capacitors, 50 V, NP0 (0402), 33 pF	Murata ENA	GRM1555C1H330JA01D

Qty	Reference Designator	Description	Manufacturer	Part Number
8	C69, C70, C78, C85, C106 to C108, C123	Multilayer ceramic capacitors, 50 V, NP0 (0402), 82 pF	Murata ENA	GRM1555C1H820JA01D
2	C8, C10	Multilayer ceramic capacitors, 50 V, NP0 (0402), 22 pF	Murata ENC	GRM1555C1H220JA01D
2	C83, C84	Aluminum electrolytic capacitors, 105°C, SMD_D, 47 µF	Panasonic EC	EEE-FC1C470P
4	C87, C94, C116, C126	Multilayer ceramic capacitors, 50 V, NP0 (0402), 330 pF	Murata ENA	GRM1555C1H331JA01D
9	D1 to D9	LED, 3 millicandela, 571 nm, 0603, green	Lite-On	LTST-C191KGKT
9	GND1 to GND9	Test point, black	Keystone Electronics	5001
2	J1, J6	10-way shroud polarized headers, 2 × 5	3M	N2510-6002RB
1	J10	TOSLINK ,16 Mpbs, optical receiver	Everlight Americas	PLR135/T10
1	J11	120-pin header, 0.6 mm	Hirose Electric	FX8-120P-SV1(91)
6	J12 to J18	Stereo mini jacks, SMT	CUI Inc.	SJ-3523-SMT
9	GND1 to GND9	Test points, black	Keystone Electronics	5001
67	3V3_A, 5V0_UNREG, ADCL1N, ADCL2N ADCL1P, ADCL2P, ADCR1N, ADCR2N, ADCR1P, ADCR2P, AUXADC2 to AUXADC7, BCLK_IN2, BCLK_OUT0, CM_BIAS, DACL1N to DACL4N, DACL1P to DACL4P, DACR1N to DACR4N, DACR1P to DACR4P, DVDD, IN1L, IN1R, IN2L, IN2R, LRCLK_IN2, LRCLK_OUT0, MCLKOUT, MISO_M, MOSI_M, OUT1L to OUT4L, OUT1R to OUT4R, SCLK_M, SDATAIO4 to SDATAIO7, SDATA_IN2, SDATA_OUT0, SDP_RESET, SPDIF_IN, SPDIF_OUT, SS_M, THD_M, THD_P, VDRIVE	Test points, white	Keystone Electronics	5002

RELATED LINKS

Resource	Description
ADAU1467	ADAU1463/ADAU1467 data sheet
SigmaStudio	SigmaStudio Software

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG15786-0-10/17(0)

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