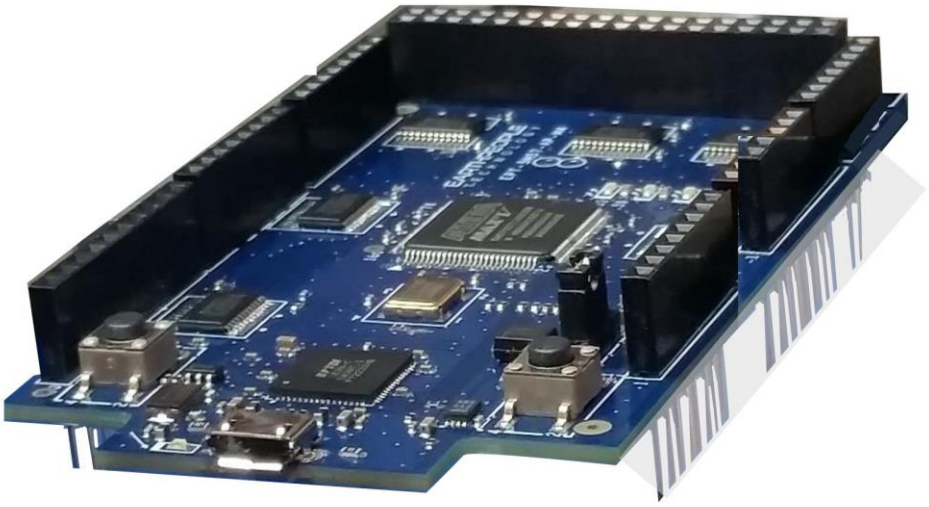
MEGAPROLOGIC

USB PLD DEVELOPMENT SYSTEM

Data Sheet



The MegaProLogic is a part of the EPT USB/PLD development system. It provides an innovative method of developing and debugging the users microcontroller code. It can also provide a high speed data transfer mechanism between microcontroller and Host PC.

The MegaProLogic board is equipped with an Altera 5M570 PLD; which is programmed using the Intel Quartus Prime software. The CPLD has 570 Logic Elements which is equivalent to 440 Macrocells. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 0.1 Mega Bytes per second. The EPT-Active-Transfer-Library provides control communication between the objective device and the CPLD. Data transfer

during the objective device checkout between the PC and the CPLD program is available via the Hyper Serial Port. The board also includes the following parts.

- Altera 5M570 in the TQFP 100 pin package
- 66 MHz oscillator for driving USB data transfers and users code
- Four 74LVC245 bidirectional voltage translator/bus transceiver
- 32 user Input/Outputs
- Four Green LED's accessible by the user
- Two PCB switches accessible by the user
- All connectors to stack into the Arduino Uno
- USB to Serial FT2232H Dual Channel Chip

1 Block Diagram

Figure 2 MegaProLogic Block Diagram

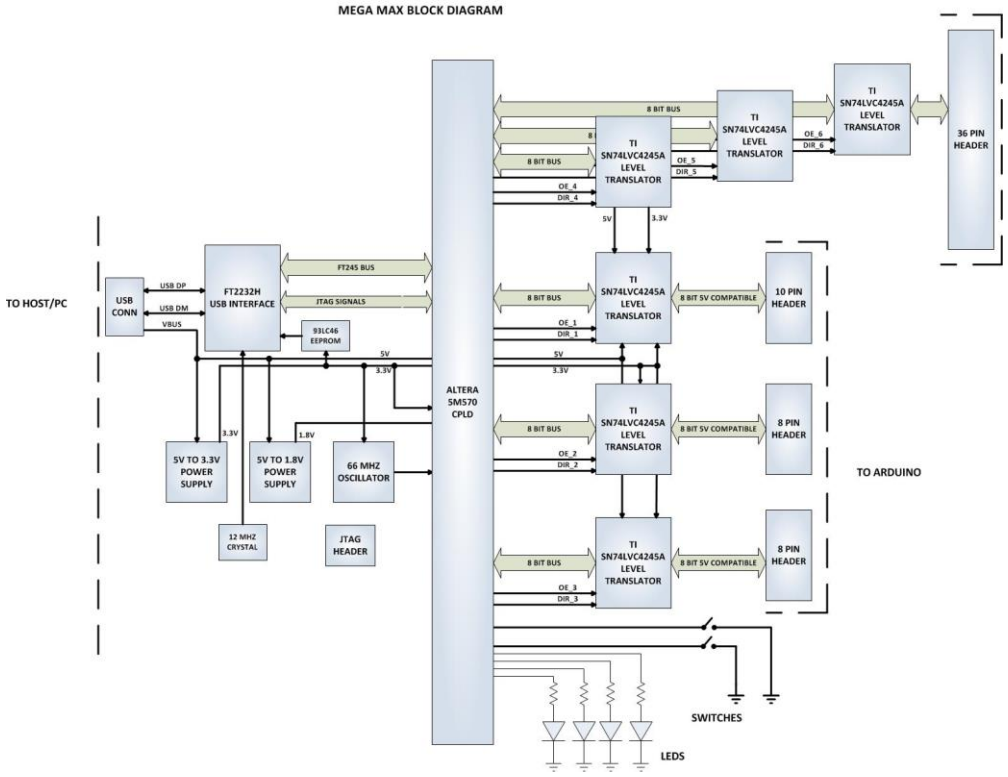
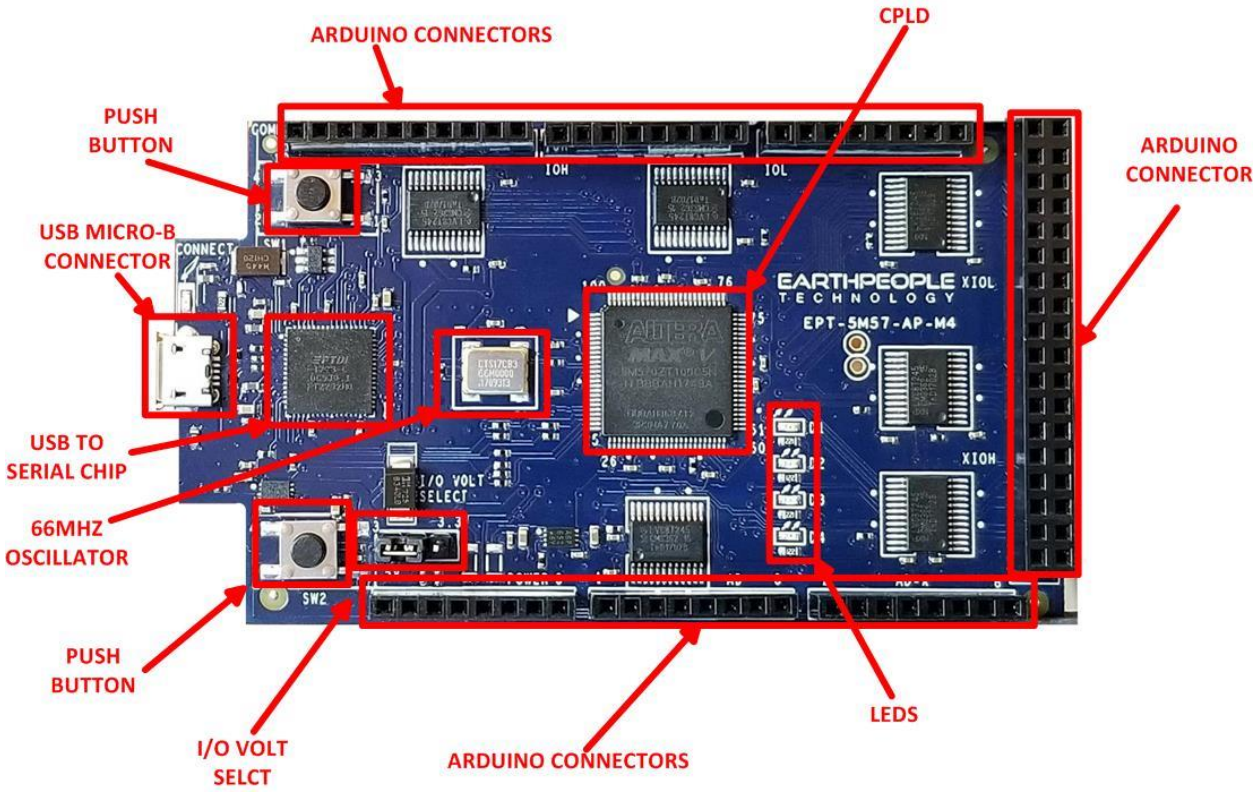
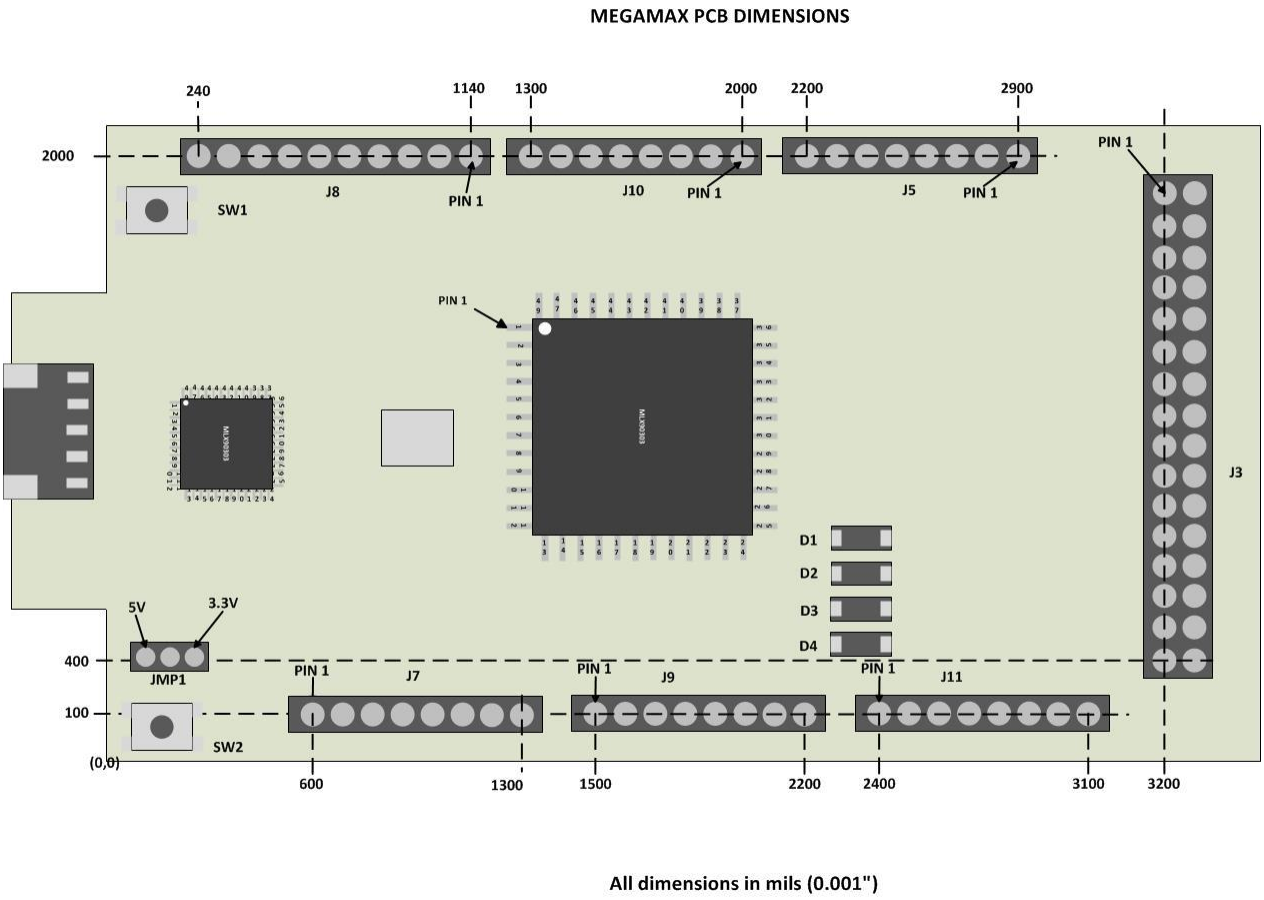


Figure 2 MegaProLogic Component Callouts



2 Mechanical Dimensions



3 Pin Mapping

Pin Mapping between Connectors, MAXV CPLD and User code

J10 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J10-1	LB0	87	LB_COMM[0]
J10-2	LB1	89	LB_COMM [1]

J10-3	LB2	91	LB_COMM [2]
J10-4	LB3	92	LB_COMM [3]
J10-5	LB4	96	LB_COMM [4]
J10-6	LB5	97	LB_COMM [5]
J10-7	LB6	98	LB_COMM[6]
J10-8	LB7	88	LB_COMM[7]
J10-9	NC	NC	NC
J10-10	NC	NC	NC

J8 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J8-1	LB8	33	LB_IO8 [0]
J8-2	LB9	34	LB_IO8 [1]
J8-3	LB10	35	LB_IO8 [2]
J8-4	LB11	36	LB_IO8 [3]
J8-5	LB12	38	LB_IO8 [4]
J8-6	LB13	40	LB_IO8 [5]
J8-7	LB14	41	LB_IO8[6]
J8-8	LB15	42	LB_IO8[7]

J9 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J9-1	LB16	81	LB_IO9 [0]
J9-2	LB17	82	LB_IO9 [1]
J9-3	LB18	83	LB_IO9 [2]
J9-4	LB19	84	LB_IO9 [3]
J9-5	LB20	78	LB_IO9 [4]
J9-6	LB21	77	LB_IO9 [5]
J9-7	LB22	76	LB_IO9[6]
J9-8	LB23	75	LB_IO9[7]

J16 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J16-1	NC	NC	NC
J16-2	NC	NC	NC
J16-3	LB38 & CIO_A_6	71	LB_IOHA 0]

J16-4	LB39 & CIO_A_7	72	LB_IOHA [1]
J16-5	LB36 & CIO_A_4	69	LB_IOHA [2]
J16-6	LB37 & CIO_A_5	70	LB_IOHA [3]
J16-7	LB34 & CIO_A_2	67	LB_IOHA[4]
J16-8	LB35 & CIO_A_3	68	LB_IOHA[5]
J16-9	LB32 & CIO_A_0	61	LB_IOHA[6]
J16-10	LB33 & CIO_A_1	66	LB_IOHA[7]
J16-11	NC	NC	

J16-12	NC	NC	
J16-13	NC	NC	
J16-14	NC	NC	
J16-15	NC	NC	
J16-16	NC	NC	
J16-17	NC	NC	
J16-18	NC	NC	
J16-19	LB46 & CIO_C_6	NC	TP1
J16-20	LB47 & CIO_C_7	NC	TP2
J16-21	SW_USER_1 & CIO_C_4	NC	SW1
J16-22	SW_USER_2 & CIO_C_5	NC	SW2
J16-23	LB42 & CIO_C_2	43	LB_IOHB[0]

J16-24	LB43 & CIO_C_3	44	LB_IOHB[1]
J16-25	LB40 & CIO_C_0	64	LB_IOHB[2]
J16-26	LB41 & CIO_C_1	62	LB_IOHB[3]
J16-27	LB31 & CIO_D_7	58	LB_IOL[0]
J16-28	LB30 & CIO_D_6	57	LB_IOL[1]
J16-29	LB29 & CIO_D_5	56	LB_IOL[2]
J16-30	LB28 & CIO_D_4	55	LB_IOL[3]

J16-31	LB27 & CIO_D_3	50	LB_IOL[4]
J16-32	LB26 & CIO_D_2	49	LB_IOL[5]
J16-33	LB25 & CIO_D_1	48	LB_IOL[6]
J16-34	LB24 & CIO_D_0	47	LB_IOL[7]
J16-35	GND	NC	
J16-36	GND	NC	

Net Name Mapping between components

Component	**Pin**	**Net Name**	**Pin on CPLD**	**Signal in EPT Project Pinout**
66MHz Oscillator	3	GCLK	12	CLK_66MHZ
Reset	2	NA	44	RST
U1	16	AD0	24	JTAG_TCK (Not In Project)

	17	AD1	23	JTAG_TDI (Not In Project)
	18	AD2	25	JTAG_TDO (Not In Project)
	19	AD3	22	JTAG_TMS (Not In Project)
	38	BD0	19	BD_INOUT0
	39	BD1	18	BD_INOUT1
	40	BD2	17	BD_INOUT2
	41	BD3	16	BD_INOUT3
	43	BD4	15	BD_INOUT4
	44	BD5	14	BD_INOUT5
	45	BD6	7	BD_INOUT6
	46	BD7	6	BD_INOUT7
	48	BC0	5	BC_IN1
	52	BC1	4	BC_IN0
	53	BC2	3	BC_OUT2
	54	BC3	2	BC_OUT1
	55	BC4	1	BC_OUT0
SW1	1	SW_USER_1	20	SW_USER_1
SW2	1	SW_USER_2	21	SW_USER_23
U7	2	TR_DIR_1	100	TR_DIR_1
U4	2	TR_DIR_2	29	TR_DIR_2

U5	2	TR_DIR_3	85	TR_DIR_3
U15	2	TR_DIR_4	30	TR_DIR_4
U13	2	TR_DIR_5	27	TR_DIR_5
U7	22	TR_OE_1	86	TR_OE_1
U4	22	TR_OE_2	28	TR_OE_2
U5	22	TR_OE_3	74	TR_OE_3
U15	22	TR_OE_4	73	TR_OE_4
U13	22	TR_OE_5	26	TR_OE_5
D1	1	LED_GR_1_N	54	LED0
D2	1	LED_GR_2_N	53	LED1
D3	1	LED_GR_3_N	52	LED2
D4	1	LED_GR_4_N	51	LED3
U7	21	LB0	87	LB_COMMS0
	20	LB1	89	LB_COMMS 1
	19	LB2	91	LB_COMMS 2
	18	LB3	92	LB_COMMS 3
	17	LB4	96	LB_COMMS 4
	16	LB5	97	LB_COMMS 5
	15	LB6	98	LB_COMMS 6
	14	LB7	99	LB_COMMS 7
U4	21	LB8	42	LB_AD0
	20	LB9	41	LB_AD1

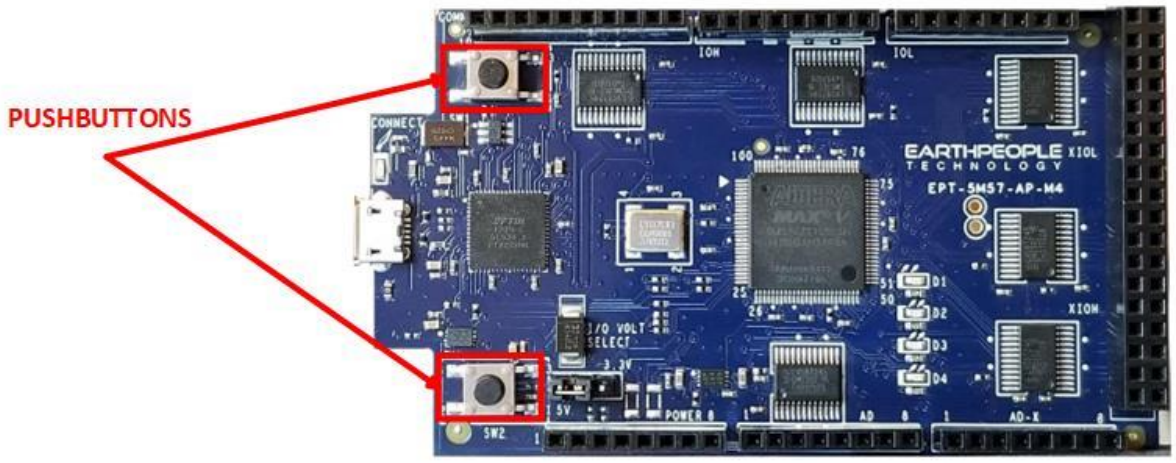
	19	LB10	40	LB_AD2
	18	LB11	38	LB_AD3
	17	LB12	36	LB_AD4
	16	LB13	35	LB_AD5
	15	LB14	34	LB_AD6
	14	LB15	33	LB_AD7
U5	21	LB16	81	LB_IOH0
	20	LB17	82	LB_IOH1
	19	LB18	83	LB_IOH2
	18	LB19	84	LB_IOH3
	17	LB20	78	LB_IOH4
	16	LB21	77	LB_IOH5
	15	LB22	76	LB_IOH6
	14	LB23	75	LB_IOH7
U13	21	LB24	47	CIO_D_0
	20	LB25	48	CIO_D_1
	19	LB26	49	CIO_D_2
	18	LB27	50	CIO_D_3
	17	LB28	55	CIO_D_4
	16	LB29	56	CIO_D_5
	15	LB30	57	CIO_D_6
	14	LB31	58	CIO_D_7

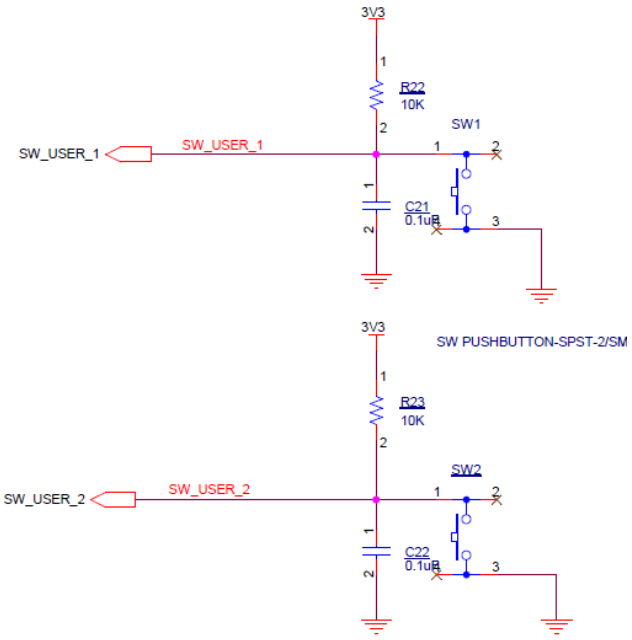
U15	21	LB32	61	CIO_A_0
	20	LB33	66	CIO_A_1
	19	LB34	67	CIO_A_2
	18	LB35	68	CIO_A_3
	17	LB36	69	CIO_A_4
	16	LB37	70	CIO_A_5
	15	LB38	71	CIO_A_6
	14	LB39	72	CIO_A_7
U14	21	LB40	62	CIO_C_0
	20	LB41	64	CIO_C_1
	19	LB42	43	CIO_C_2
	18	LB43	44	CIO_C_3

4 Pushbutton switches

There are two pushbutton switches on the MegaProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	**Net Name**	**Pin on CPLD**	**Signal in EPT Project Pinout**
SW1	SW_USER_1	20	SW_USER_1
SW2	SW_USER_2	21	SW_USER_23



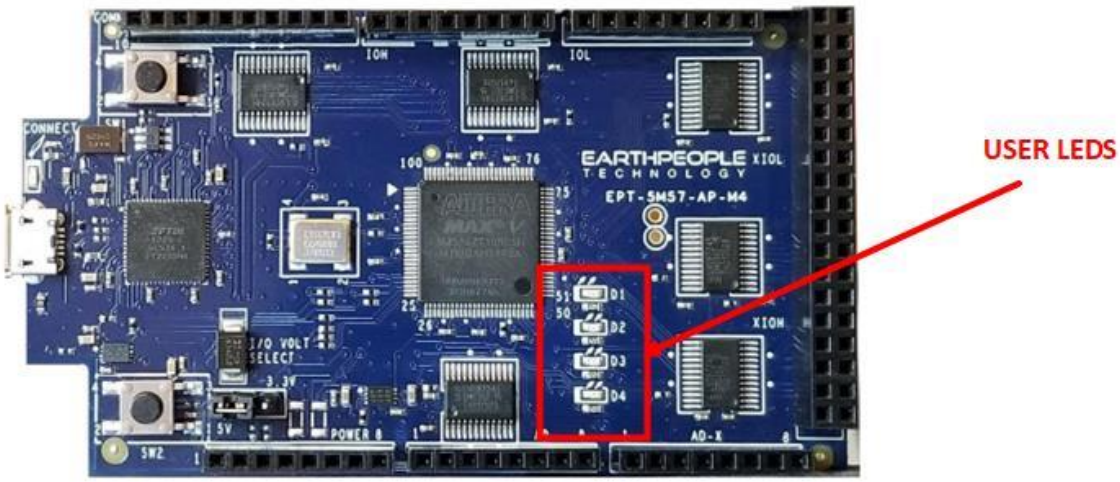


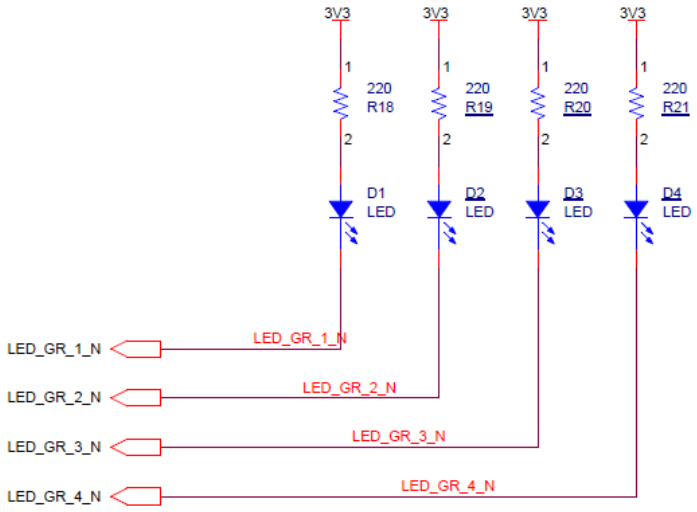
5 LEDs

The MegaProLogic includes four Green LEDs. The LEDs are connected to the CPLD in a

"Current Sink" configuration. This means the LEDs Anodes are permanently connected to +3.3V. Each Cathode side of the LEDs are connected to an individual I/O of the CPLD. In order to turn on the LED, the CPLD I/O must apply a low signal. This will complete the LED drive circuit and current will flow through the LED. To turn the LED off, the CPLD I/O must either "float" or drive a high onto the pin.

Component	**Net Name**	**Pin on CPLD**	**Signal in EPT Project Pinout**
LED1	LED[1]	50	LED[0]
LED2	LED[2]	51	LED[1]
LED3	LED[3]	52	LED[2]
LED4	LED[4]	53	LED[3]

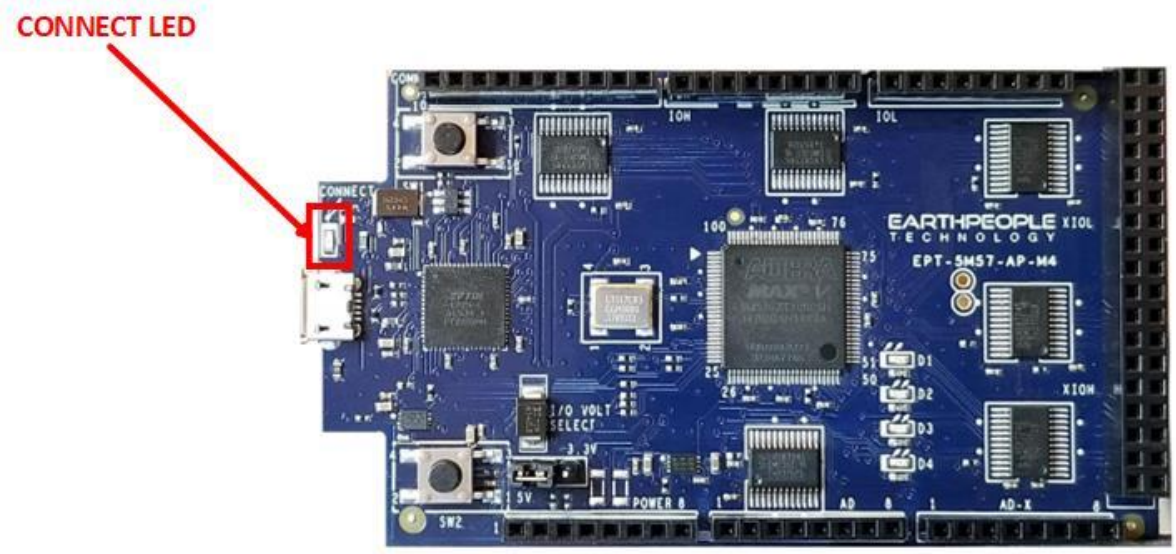




6 Host PC Connection

The MegaProLogic includes an LED that signifies the connection of the board with the Host PC. The connect LED has the word “CONNECT” in silkscreen next to the LED. This LED will only light up once the Host PC has correctly enumerated the USB device (FT2232HQ chip). When this LED is lit up it can tell the user three things:

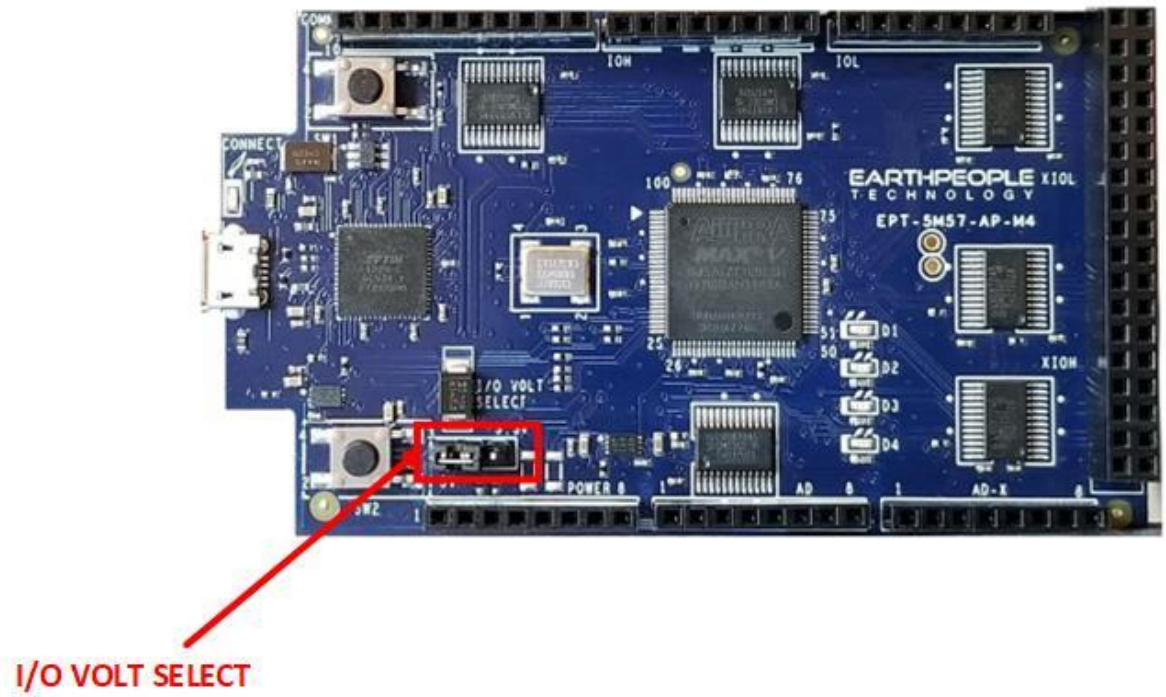
- Power has been applied to the MegaProLogic via USB
- The FT2232HQ chip is working properly
- The Host PC has found the appropriate driver and will communicate with the MegaProLogic



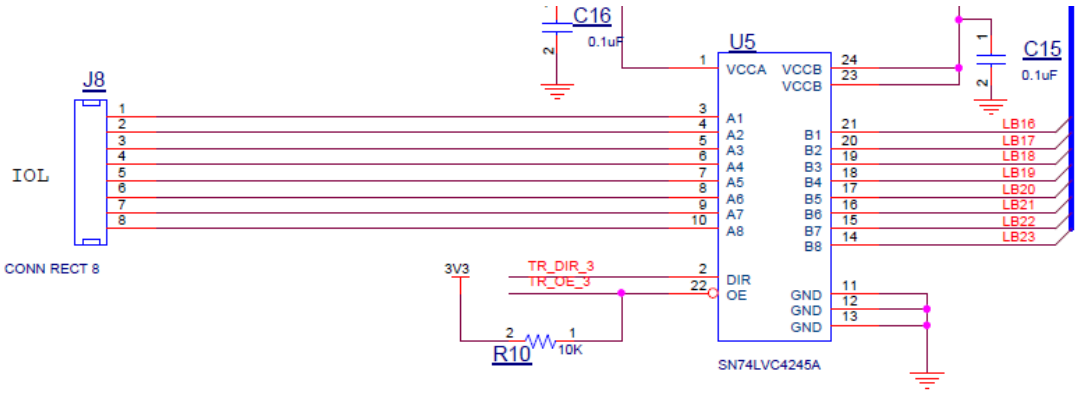
7 Inputs/Outputs

The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin.

There are 24 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to select which voltage the 24 Inputs/Outputs are set to.



The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will "float".



This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has VCCB, which is set at 3.3 V, and A port has VCCA, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, OE) is powered by VCCA.

7.1 Electrical Characteristics

for V_{CCA} = 4.5 V to 5.5 V(1)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Tim

for V_{CCB} = 2.7 V to 3.6 V(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		–12	mA
		V_{CCB} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.2 Timing Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

7.3 Description

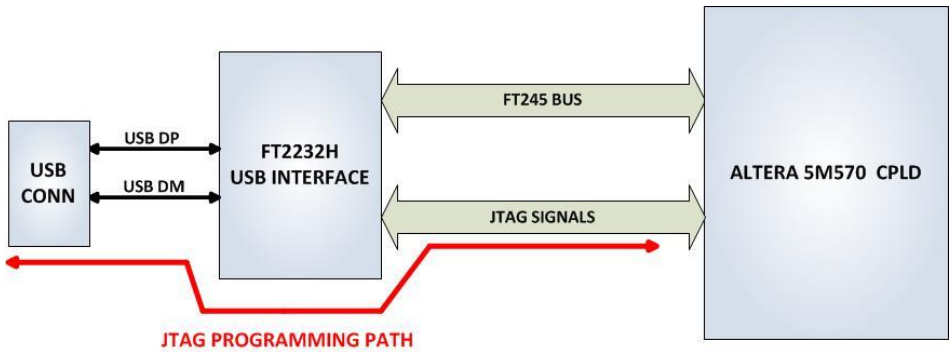
24 mA drive at 3-V supply
– Good for heavier loads and longer traces
Low VIH
– Allows 3.3-V to 5-V translation

Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

8 MAXV Programming

The UnoMax uses the second channel of the FT2232H chip as a dedicated CPLD programming port. The CPLD must be programmed via JTAG signals and the FT2232H has built in JTAG signals.



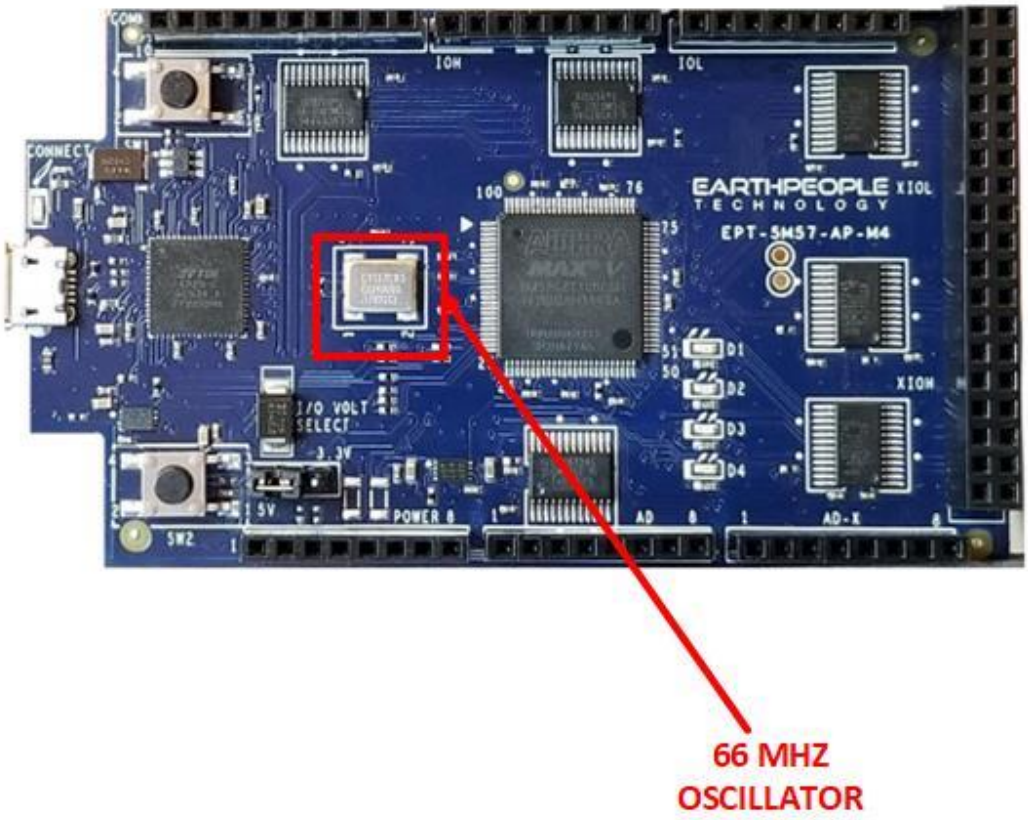
9 Oscillator

There is a 66MHz oscillator on the MegaProLogic, This oscillator has the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I

This oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling the net connected to the FPGA pin.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	CLK_66MHZ	



XLH536066.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz

Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	25 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

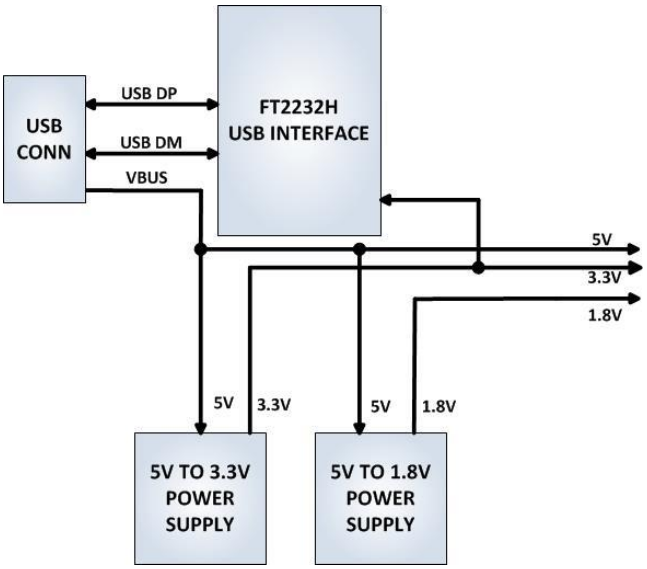
10 USB to Serial

The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is+5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.

11 MegaProLogic Power

The MegaProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the MegaProLogic must share this power with the user code that will run inside the CPLD along with any external power use.



11.1 Core Board Power Budget

Device	Part Number	+1.8V Power	+3.3V Power

CPLD	5M570	??? Defined by user code. EPT-Transfer-Demo code: 50mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Bus Transceivers	74LVC8245		15mA (All eight I/O's active)
USB Chip	FT2232H		60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56		2 mA (write current) 1 mA (read current)
66MHz Oscillator	CB3LV-3I-66M0		10 mA
Op-Amp driver	MCP6L04		0.5 mA (all four amps active)
Schmitt Buffer	74LVC1G17SE		1mA
User LEDs			20 mA
Total		**50mA**	**175.5mA**

*Theoritical Values only. This data needs to be validated

11.2 Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.8V Power Supply	MCP1725-1802E	70mA		
+3.3V Power Supply	MCP1725-3302E	215mA		
Total		**285mA**		

* Theoritical Values only. This data needs to be validated