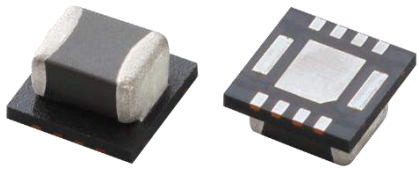
“PicoBK™” MYRGC series

0.5A Inductor Built-in Step-down DC/DC Converter

■GENERAL DESCRIPTION



The MYRGC series is a 18V operation synchronous step-down DC/DC converter ICs with a built-in high-side / low-sidedriver transistor. The MYRGC series has operating voltage range of 3.0V～18.0V and it can support 0.5A as an outputcurrent with high-efficiency. Compatible with Low ESR capacitors such as ceramic capacitors for the load capacitor (CL).
0.75V reference voltage source is incorporated in the IC, and the output voltage can be set to a value from 1.0V to 15.0V using external resistors (RFB1, RFB2).
1.2MHz can be selected for the switching frequency. In PWM/PFM automatic switchover control, IC can change the control method between PWM and PFM based on the output current requirement and as a result IC can achieve high efficiency over the full load range.
MYRGC has a fixed internal soft start time which is 1.0ms (TYP.), additionally the time can be extended by using an external resistor and capacitor.

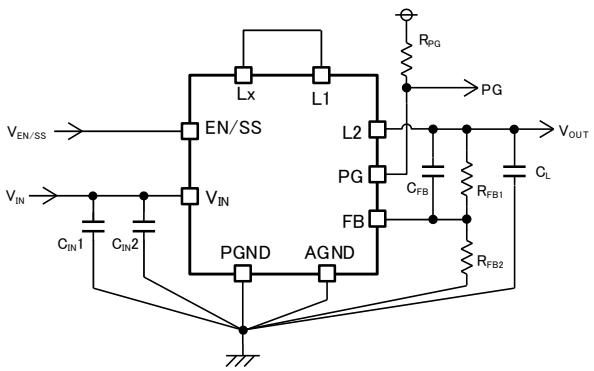
■APPLICATIONS

- ●Hot water supply system
- ●Recorders, Camcorders
- ●Refrigerators, Air-conditioners
- ●Low Power Systems

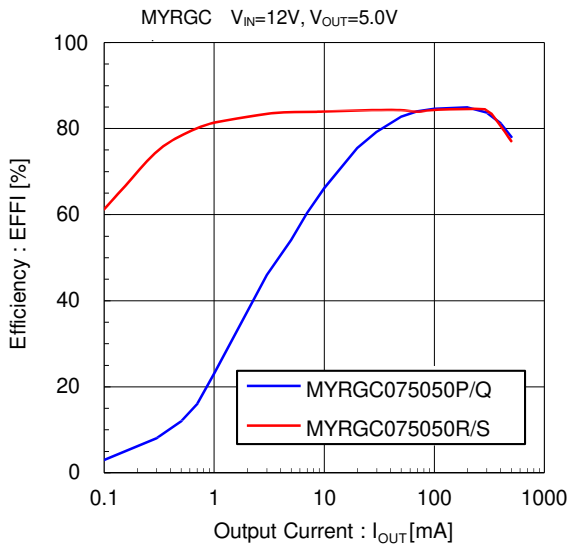
■FEATURES

Input Voltage Range	:	3.0～18V（Absolute Max 20V）
Output Voltage Range	:	1.0～15.0V (FB Voltage=0.75V±1.5%)
Switching Frequency	:	1.2MHz
Output Current	:	0.5A
Control Methods	:	PWM control (MYRGC075050P/Q)
		PWM/PFM Automatic (MYRGC075050R/S)
		Efficiency 85%@12V→5V, 1mA
Soft-start Time	:	Adjustable by RC
Protection Circuits	:	Over Current Protection
		Integral Latch Method (MYRGC075050P/R)
		Automatic Recovery (MYRGC075050Q/S)
		Thermal Shutdown
Environmentally Friendly	:	EU RoHS Compliant, Pb Free
		Halogen Free

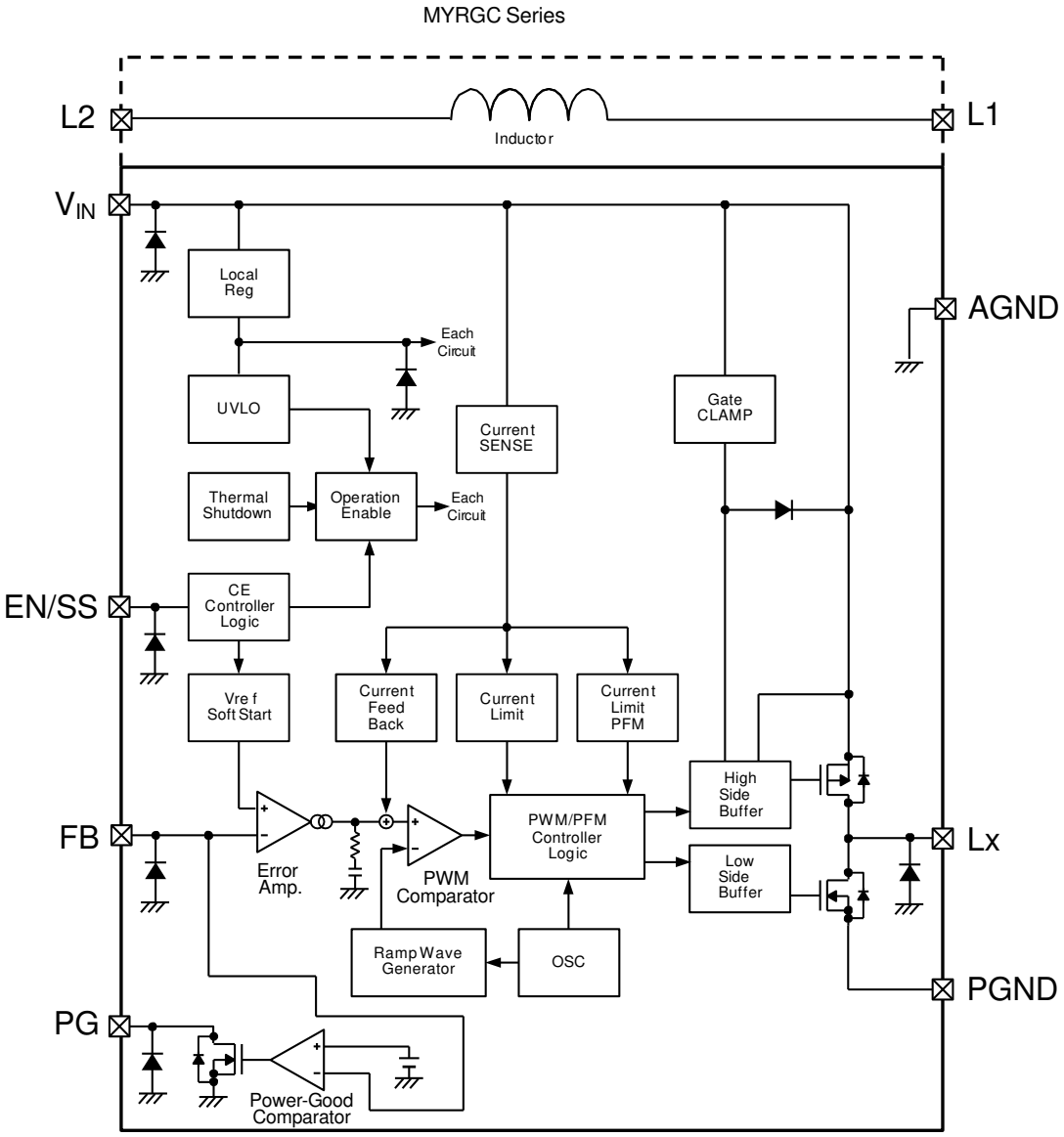
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS

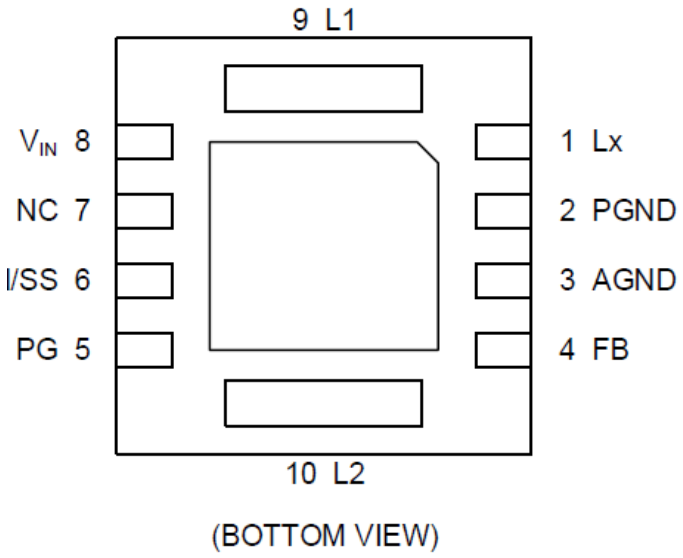


■BLOCK DIAGRAM



The MYRGC075050P/Q series is fixed to PWM control.
The MYRGC075050R/S series is PWM / PFM automatic switching control.
Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

■PIN CONFIGURATION



(BOTTOM VIEW)

* The dissipation pad for this package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2 and No.3) pin.

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
1	Lx	Switching Output
2	PGND	Power Ground
3	AGND	Analog Ground
4	FB	Output Voltage Sense
5	PG	Power-good Output
6	EN/SS	Enable Soft-start
7	NC	No Connection
8	V_{IN}	Power Input
9	L1	Inductor Electrodes
10	L2	Inductor Electrodes

* This 7-pin NC terminal is not connected to an IC chip.

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State(*1)

(*1) Please do not leave the EN/SS pin open. Each should have a certain voltage

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER	SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage	V_{IN}	-0.3 ～ +20	V
EN/SS Pin Voltage	$V_{EN/SS}$	-0.3 ～ +20	V
FB Pin Voltage	V_{FB}	-0.3 ～ +6.2	V
PG Pin Voltage	V_{PG}	-0.3 ～ +6.2	V
PG Pin Current	I_{PG}	8	mA
Lx Pin Voltage	V_{Lx}	-0.3 ～ V_{IN}+0.3 or +20 (*1)	V
Lx Pin Current	I_{Lx}	1800	mA
Power Dissipation	Pd	1950(JEDEC board)(*2)	mW
Operating Ambient Temperature	Topr	-40 ～ +105	℃
Storage Temperature	Tstg	-55 ～ +125	℃

* All voltages are described based on the GND (AGND、PGND) pin.

(*1) The maximum value should be either V_{IN}+0.3 or 20 in the lowest.

(*2) The power dissipation figure shown is PCB mounted and is for reference only.
Please see the power dissipation page for the mounting condition.

■ELECTRICAL CHARACTERISTICS

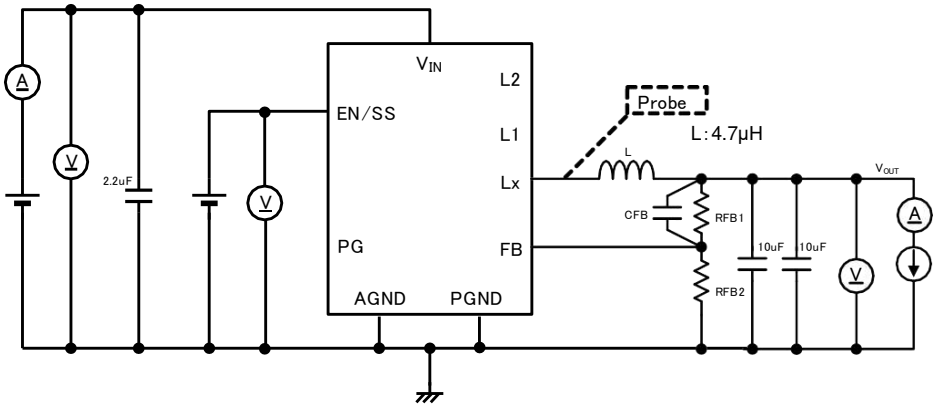
MYRGC Series Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V_{FB}	V_{FB}=0.739V→0.761V, V_{FB} Voltage when Lx pin oscillates	0.739	0.750	0.761	V	②
Output Voltage Setting Range(*1)	V_{OUTSET}	-	1	-	15	V	–
Operating Voltage Range	V_{IN}	-	3	-	18	V	–
UVLO Detect Voltage	V_{UVLO1}	V_{IN}:2.8V→2.6V, V_{FB}=0.675V, V_{IN} Voltage when Lx pin voltage changes from "H" level to "L" level	2.60	2.70	2.80	V	②
UVLO Release Voltage	V_{UVLO2}	V_{IN}:2.7V→2.9V、V_{FB}=0.675V, V_{IN} Voltage when Lx pin voltage changes from "L" level to "H" level	2.70	2.80	2.90	V	②
Quiescent Current	I_q	V_{FB}=0.825V	-	12.5	17.5	μA	④
Stand-by Current	I_{STB}	$V_{EN/SS}$=0V	-	1.65	2.5	μA	⑤
Oscillation Frequency	f_{OSC}	Connected to external components, I_{OUT}=100mA	1098	1200	1302	kHz	①
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V	-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V	100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.675V, I_{LX}=200mA	-	0.99	1.14	Ω	②
Lx SW "L" On Resistance	R_{LxL}	V_{FB}=0.825V, I_{LX}=200mA	-	0.73(*2)	-	Ω	②
PFM Switch Current	I_{PFM}	Connected to external components, I_{OUT}=1mA	-	320	-	mA	①
High side Current Limit (*3)	I_{LIMH}	V_{FB}=0.675V	920	1100	-	mA	②
Latch Time	t_{LAT}	Type A only, Connected to external components, V_{FB}=0V	0.5	1.0	1.7	ms	⑥
Internal Soft-Start Time	t_{SS1}	$V_{EN/SS}$=0V→12V, V_{FB}=0.675V, Time until Lx pin oscillates	0.5	1.0	1.7	ms	②
External Soft-Start Time	t_{SS2}	$V_{EN/SS}$=0V→12V, V_{FB}=0.675V, R_{SS}=430KΩ, C_{SS}=0.47μF Time until Lx pin oscillates	17	26	35	ms	③
PG Detect Voltage	V_{PGDET}	V_{FB}=0.712V→0.638V, R_{PG}:100kΩ pull-up to 5V, V_{FB} Voltage when PG pin voltage changes from "H" level to "L" level	0.638	0.675	0.712	V	②
PG Output Voltage	V_{PG}	V_{FB}=0.6V, I_{PG}=1mA	AGND	-	0.3	V	②
Efficiency (*4)	EFFI	Connected to external components, V_{OUT}=5V, I_{OUT}=1mA	-	82(2)	-	%	①
FB Voltage Temperature Characteristics	ΔV_{FB}/ (ΔTopr・V_{FB})	-40℃≦Topr≦105℃	-	±100	-	ppm /℃	②
FB 'H' Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=3.0V	-0.1	-	0.1	μA	④
FB 'L' Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=0V	-0.1	-	0.1	μA	④
EN/SS 'H' Current	$I_{EN/SSH}$	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=0.825V	-	0.1	0.3	μA	④
EN/SS 'L' Current	$I_{EN/SSL}$	V_{IN}=18V、$V_{EN/SS}$=0V、V_{FB}=0.825V	-0.1	-	0.1	μA	④
EN/SS 'H' Voltage	$V_{EN/SSH}$	$V_{EN/SS}$=0.3V→2.5V、V_{FB}=0.71V, $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" level to "H"	2.5	-	18.0	V	②
EN/SS 'L' Voltage	$V_{EN/SSL}$	$V_{EN/SS}$=2.5V→0.3V, V_{FB}=0.71V, $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" level to "L"	AGND	-	0.3	V	②
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature	-	150	-	℃	-
Hysteresis Width	T_{HYS}	Junction Temperature	-	25	-	℃	-
Inductance	L	Test Freq.=1MHz	-	4.3	-	μH	-
Inductor Rated Current	I_{DC}	ΔT=+40℃	-	1200	-	mA	-

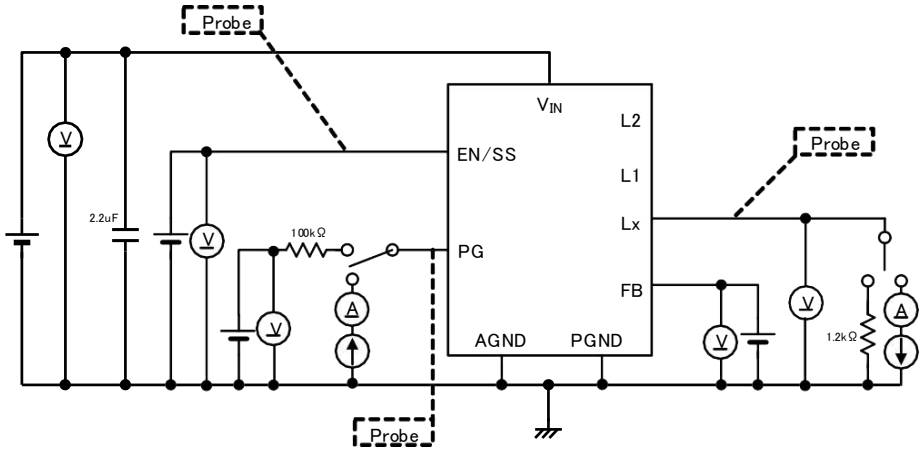
Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V
(*1): Please use within the range of V_{OUT}/V_{IN}≧0.14
(*2): Design reference value. This parameter is provided only for reference.
(*3): Current limit denotes the level of detection at peak of coil current.
(*4): EFFI = {(output voltage) x (output current)} / {(input voltage) x (input current)} x 100

■TEST CIRCUITS

Circuit No.①



Circuit No.②



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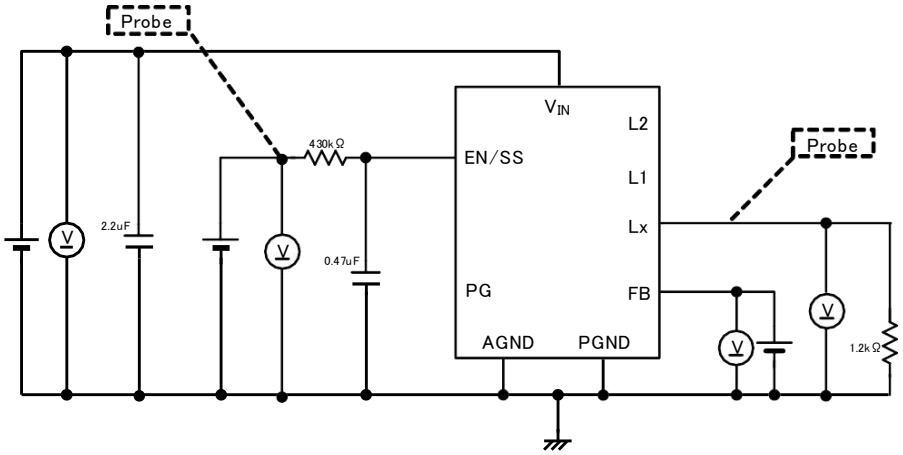
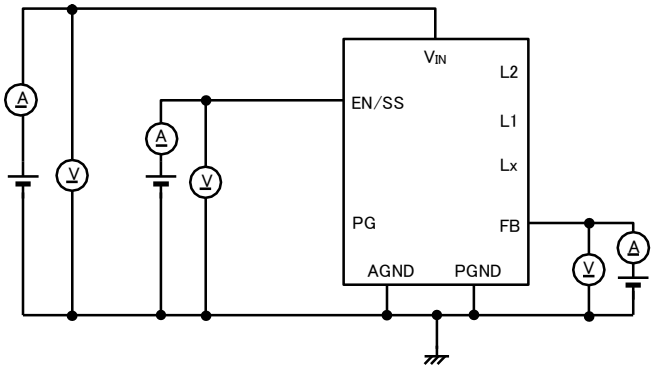


■TEST CIRCUITS

Circuit No.④



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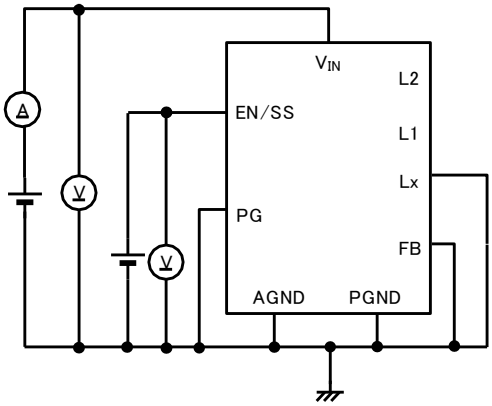

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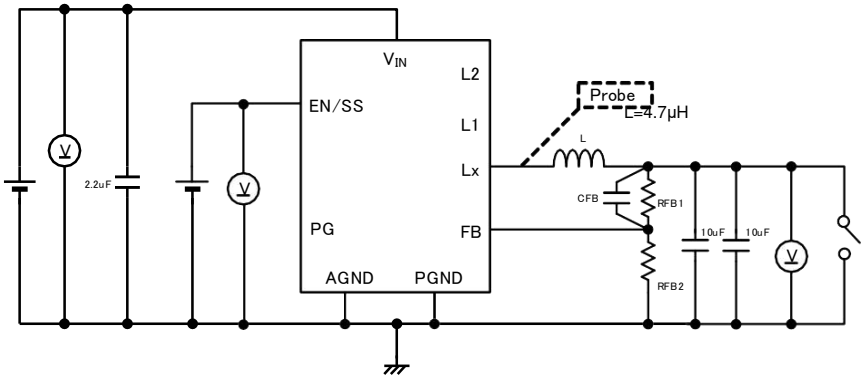
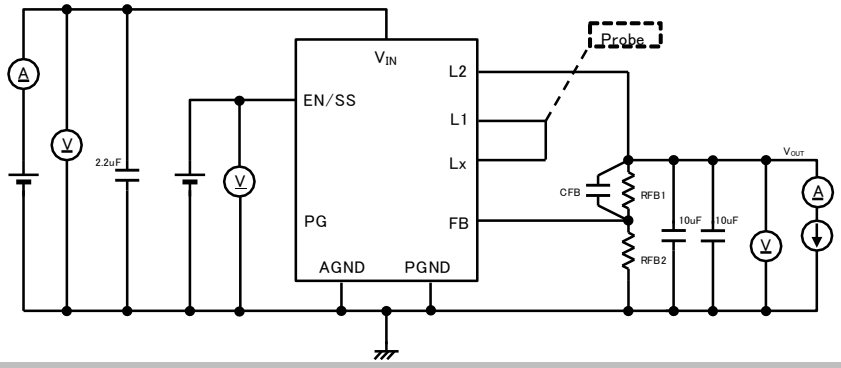
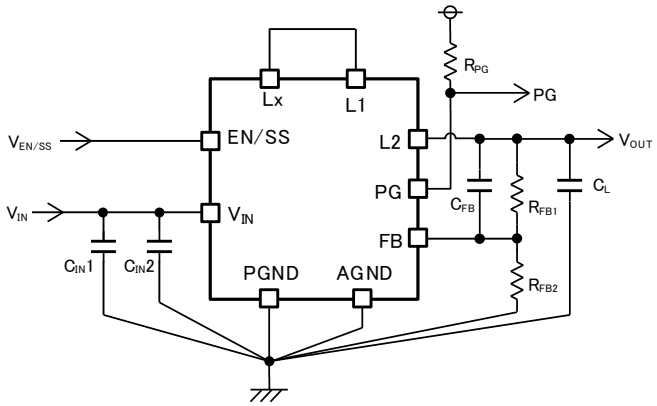


Circuit No.⑦



■TYPICAL APPLICATION CIRCUIT



*Coil is dedicated to this product. Please do not use it for purposes other than this product.

【Typical example】

	VALUE
C_{IN1}	25V/4.7μF
C_{IN2}	25V/0.1μF
	50V/0.1μF
C_L	10V/10μF
	25V/10μF
	10V/22μF
	25V/22μF

*When under the condition of the voltage difference between input voltage and output voltage is low, please use 125℃ product, which has small capacity drop.

【Typical example】

V_{OUT}	R_{FB1}	R_{FB2}	C_{FB} (C_L=20μF)	C_{FB} (C_L=10μF)
1.2V	180kΩ	300kΩ	56pF	39pF
1.5V	220kΩ	220kΩ	47pF	33pF
1.8V	180kΩ	130kΩ	56pF	39pF
2.5V	560kΩ	240kΩ	15pF	12pF
3.0V	390kΩ	130kΩ	27pF	18pF
3.3V	510kΩ	150kΩ	22pF	15pF
5.0V	680kΩ	120kΩ	18pF	10pF
7.5V	270kΩ	30kΩ	39pF	27pF
10.0V	160kΩ	13kΩ	68pF	47pF
12.0V	360kΩ	24kΩ	33pF	22pF

・About R_{PG}
The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin.
When not using power good function connect the PG pin to GND or open it for use.

■TYPICAL APPLICATION CIRCUIT(Continued)

<Output voltage setting>
The output voltage can be set by adding an external dividing resistor.
The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUT}=V_{FB}\times (R_{FB1}+R_{FB2})/R_{FB2}$$
With $R_{FB1}+R_{FB2} \leqq 1M\Omega$

<C_{FB} setting>
Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB}=\frac{1}{2\pi\times fzfb\times R_{FB1}}$$

A target value for fzfb of optimum is below.

$$fzfb=\frac{1}{2\pi\sqrt{C_L\times L}}$$

【Setting Example】

When C_L is 10μF, fzfb=24kHz
When C_L is 20μF, fzfb=17kHz

【Setting Example】

To set output voltage to 5V with fosc=1.2MHz, C_L=20μF, L=4.3μH

When R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUT}=0.75V× (680kΩ+120kΩ) / 120kΩ=5.0V
And fzfb is set to a target of 17kHz using the above equation,
C_{FB}=1/(2× π ×17kHz×680kΩ)=13.8pF

* The setting range for the output voltage is 1.0V to 15.0V.
The condition $V_{OUT}/V_{IN} \geqq$ 0.14 must be satisfied.

<Soft-start Time Setting>

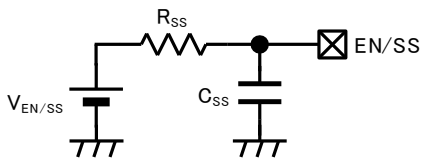
The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.
Soft-start time (t_{ss2}) is approximated by the equation below according to values of $V_{EN/SS}$, R_{SS}, and C_{SS}.

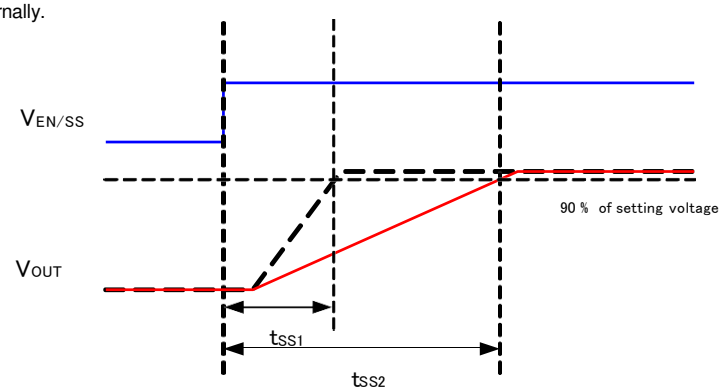
$$t_{ss2}=C_{ss}\times R_{ss}\times (-\ln ((V_{EN/SS}-1.45)/V_{EN/SS}))$$

【Setting Example】

When C_{SS}=0.47μF, R_{SS}=430kΩ and $V_{EN/SS}$=12V, $t_{SS2}=0.47\times10^{-6}\times 430\times 10^{3}\times(-\ln((12-1.45)/12))$ =26ms (Approx.)

*The soft-start time is the time from the start of $V_{EN/SS}$ until the output voltage reaches 90% of the set voltage. If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{ss1}=1.0ms (TYP.) which is fixed internally.





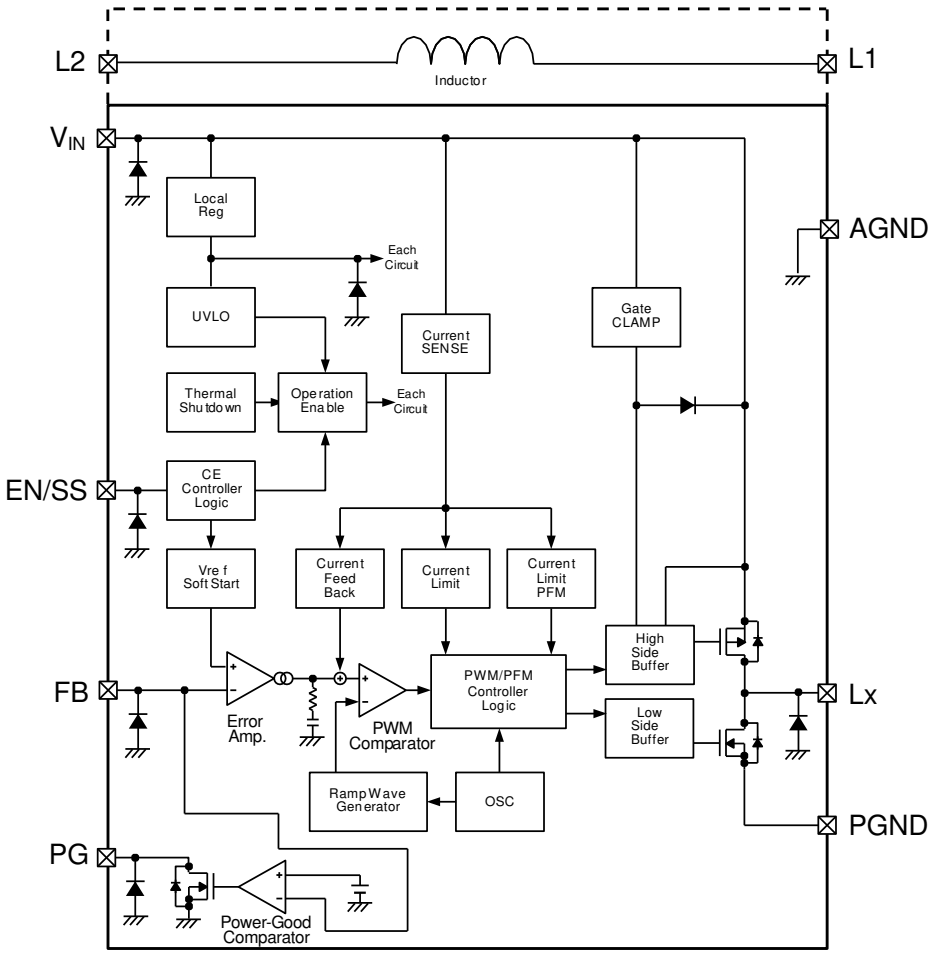
■OPERATIONAL EXPLANATION (Continued)

The MYRGC series consists internally of a reference voltage supply with soft-start function, error amp, PWM comparator, ramp wave circuit, oscillator (OSC) circuit, phase compensation (Current feedback) circuit, current limiting circuit, current limit PFM circuit, High-side driver Tr., Low-side driver Tr., buffer drive circuit, internal power supply (LocalReg) circuit, under-voltage lockout (UVLO) circuit, gate clamp (CLAMP) circuit, thermal shutdown (TSD) circuit, power good comparator, control block and other elements.

The voltage feedback from the FB pin is compared to the internal reference voltage by the error amp, the output from the error amp is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation. The output signal from the error amp is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the Lx pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The driver transistor current is monitored at each switching by the phase compensation (Current feedback) circuit, and the output signal from the error amp is modulated as a multi-feedback signal. This allows a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.

MYRGC Series



*Diodes inside the circuit are an ESD protection diodes and a parasitic.

■OPERATIONAL EXPLANATION (Continued)

<Reference voltage source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Oscillator circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally 1.2MHz.
Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation.

<Error amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal voltage divider, R_{FB1} and R_{FB2}. When a voltage is lower than the reference voltage, then the voltage is fed back, the output voltage of the error amplifier increases. The error amplifier output is fixed internally to deliver an optimized signal to the mixer.

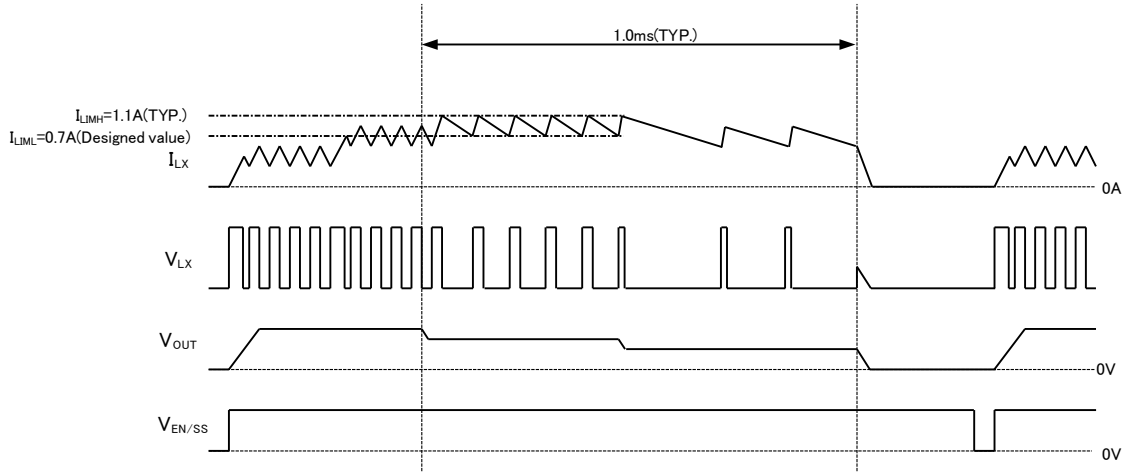
<Current limiting>
The current limiting circuit of the MYRGC series monitors the current that flows through the High-side driver transistor and Low-side driver transistor, and when over-current is detected, the current limiting function activates.

① Low-side driver Tr. current limiting
The current in the Low-side driver Tr. is detected to equivalently monitor the bottom value of the coil current. The Low-side driver Tr. current limiting function prohibits the High-side driver Tr. from turning on in an over-current state where the bottom value of the coil current is higher than the Low-side driver Tr. current limit value I_{LIML}. Control to lower the switching frequency f_{OSC} is also performed. When the over-current state is released, normal operation resumes.

② High-side driver Tr. current limiting
The current in the High-side driver Tr. is detected to equivalently monitor the peak value of the coil current. The High-side driver Tr. current limiting function forcibly turns off the High-side driver Tr. when the peak value of the coil current reaches the High-side driver current limit value I_{LIMH}. $I_{LIML} < I_{LIMH}$ is set inside the IC, and therefore the Low-side driver Tr. current limiting function of ① above also detects the over-current state at this time. When the over-current state is released, normal operation resumes.

③ Over-current latch (Type P / Type R)
Type P / Type R turns off the High-side and Low-side driver Tr. when state ① or ② continues for 1.0ms (TYP.). The Lx pin is latch-stopped at the GND level (0V).
The latch-stopped state only stops the pulse output from the Lx pin; the internal circuitry of the IC continues to operate. To restart after latch-stopping, L level and then H level must be input into the EN/SS pin, or V_{IN} pin re-input must be performed (after lowering the voltage below the UVLO detection voltage) to resume operation by soft start.
The over-current latch function may occasionally be released from the current limit detection state by the effects of ambient noise, and it may also happen that the latch time becomes longer or latching does not take place due to board conditions. For this reason, place the input capacitor as close as possible to the IC.
Type Q / Type S is an automatic recovery type that performs the operation of ① or ② until the over-current state is released.

Low side driver Tr. current limit value I_{LIML}=0.7A (Designed value)
High-side driver Tr. current limit value I_{LIMH}=1.1A (TYP.)



< Current limiting timing chart >

■OPERATIONAL EXPLANATION (Continued)

<Soft-start function>

The reference voltage applied to the error amplifier is restricted by the start-up voltage of the EN/SS pin. This ensures that the error amplifier operates with its two inputs in balance, thereby preventing ON-time signal from becoming longer than necessary. Therefore, start-up time of the EN/SS pin becomes the set-time of soft-start. The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.

If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{ss1}=1.0ms (TYP.) which is fixed internally.

The soft-start function operates when the voltage at the EN/SS pin is between 0.3V to 2.5V. If the voltage at the EN/SS pin does not start from 0V but from a middle level voltage when the power is switched on, the soft-start function will become ineffective and the possibilities of large inrush currents and ripple voltages occurring will be increased.

<Thermal shutdown>

The thermal shutdown (TSD) as an over current limit is built in the MYRGC series.
When the junction temperature reaches the detection temperature, the driver transistor is forcibly turned off. When the junction temperature falls to the release temperature while in the output stop state, restart takes place by soft-start.

<UVLO>

When the V_{IN} pin voltage falls below 2.7V (TYP.), the driver transistor is forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above 2.8V (TYP.), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

<Power good>

The output state can be monitored using the power good function.
When the FB voltage drops below 90% (TYP.), the PG pin outputs an "L" signal.
The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin.
When not using power good function connect the PG pin to GND or open it for use.

■NOTE ON USE(Continued)

1)For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.

2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

3)The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select. Be especially careful of the capacitor characteristics and use B characteristics (JIS standard) or X7R, X5R (EIA standard) ceramic capacitors.
The capacitance decrease caused by the bias voltage may become remarkable depending on the external size of the capacitor.

4) If there is a large dropout voltage, then there might be pulse-skip during light loads even with PWM control.

5)The DC/DC converter of this IC uses a current-limiting circuit to monitor the coil peak current. If the potential dropout voltage is large or the load current is large, the peak current will increase, which makes it easier for current limitation to be applied which in turn could cause the operation to become unstable.

6) If there is a large dropout voltage, a circuit delay could create the ramp-up of coil current with staircase waveform exceeding the current limit.

7)The ripple voltage could be increased when switching from discontinuous conduction mode to Continuous conduction mode. Please evaluate IC well on customer's PCB.

8) The operation of becomes unstable below the minimum operating voltage.

9) If the voltage at the EN/SS Pin does not start from 0V but it is at the midpoint potential when the power is switched on, the soft start function may not work properly and it may cause the larger inrush current and bigger ripple voltages.

10)The effects of ambient noise and the state of the circuit board may cause release from the current limiting state, and The latch time may lengthen or latch operation may not take place. Please evaluate IC well on customer's PCB.

■NOTE ON USE

11) Instructions of pattern layouts

(1) The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(CIN) and the output capacitor (CL) as close to the IC as possible.

(2) In order to stabilize VIN voltage level, we recommend that a by-pass capacitor (CIN) be connected as close as possible to the VIN and PGND pins.

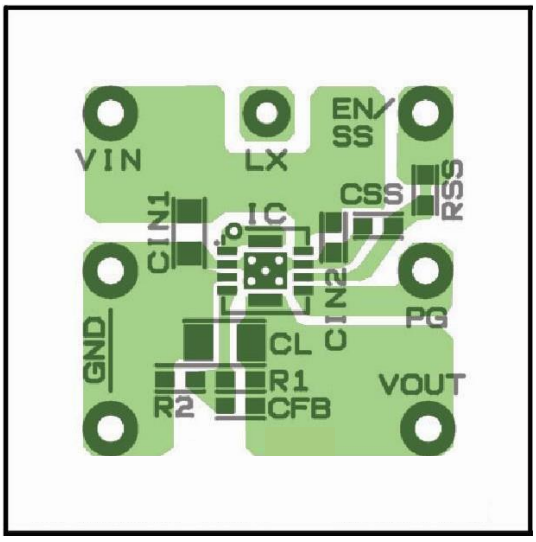
(3) Please mount each external component as close to the IC as possible.

(4) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

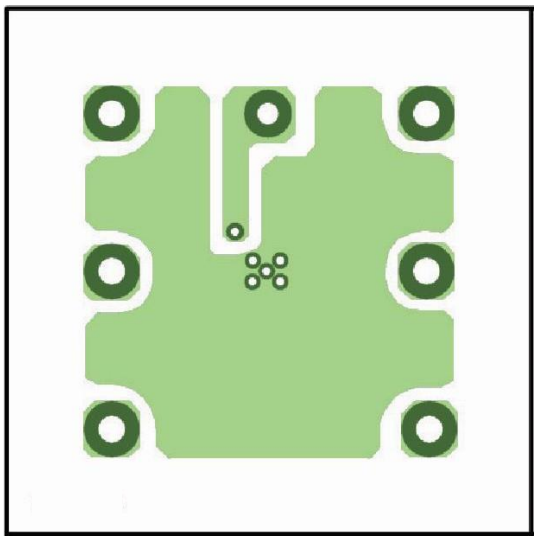
(5) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

(6) Please note that internal driver transistors bring on heat because of the load current and ON resistance of High-side driver transistor,Low-side driver transistor.

< Reference Pattern Layout >



< Top view>



< Bottom side top view >

12) MURATA places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using MURATA products in their systems.

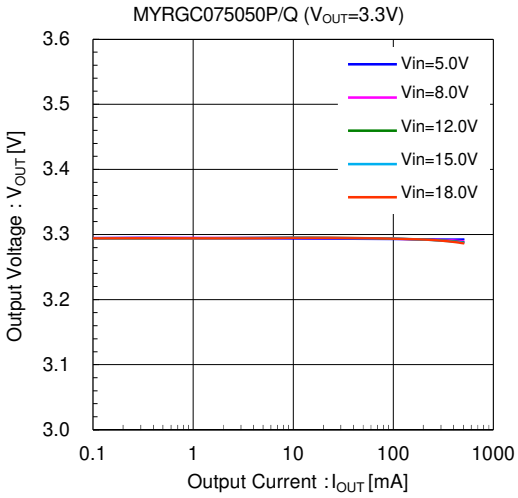
■About the appearance (coil part)

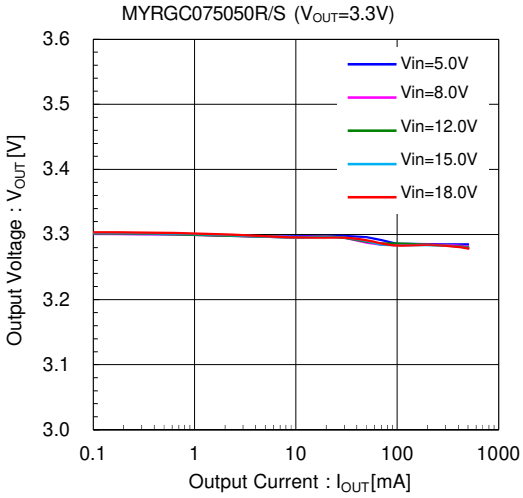
(1) Coils are compliant with general surface mount type chip coil (inductor) specifications and may have scratches, flux contamination and the like.

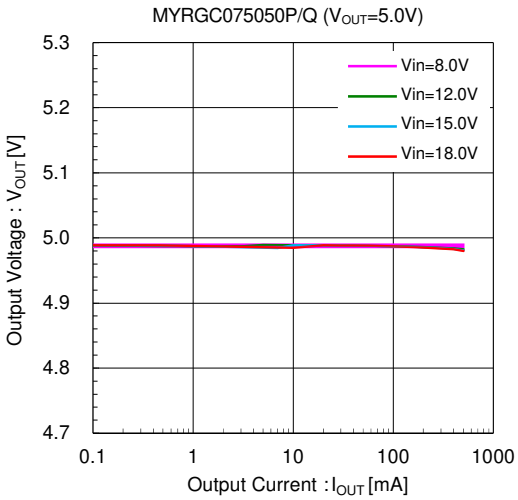
(2) This product has a coil which is soldered on top of the package. There is no problem with normal board mounting reflow. If the excessive shock is provided during reflow, there is a possibility to cause the coil misaligned or have the coil fell off. Please be careful not to provide excessive shock to the PCB during the board mounting reflow.

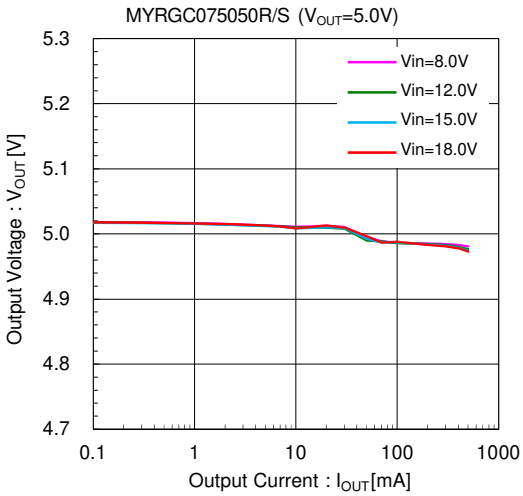
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs. Output Current



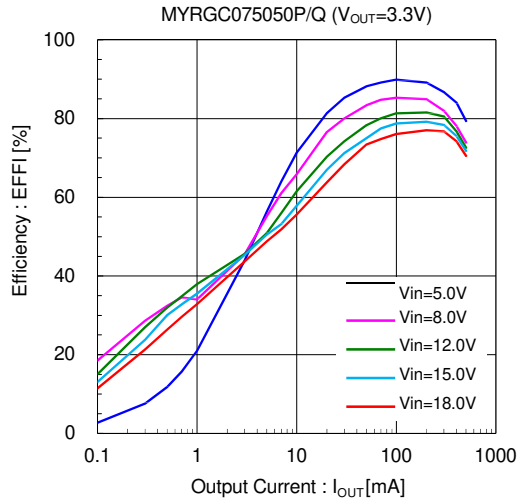


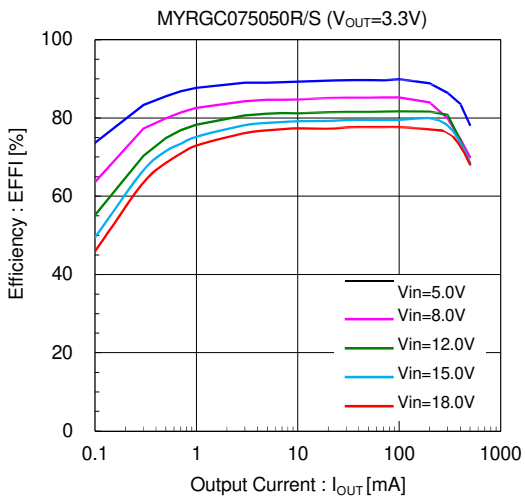


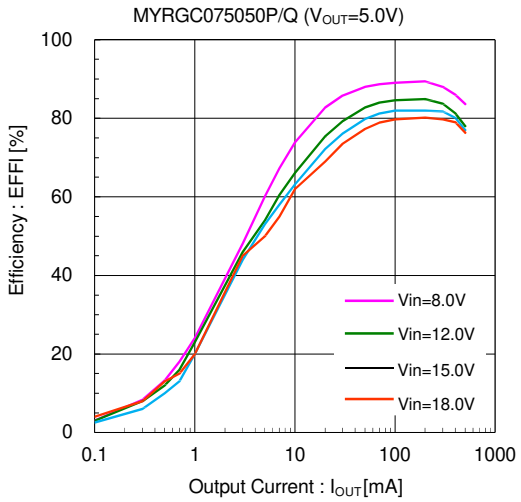


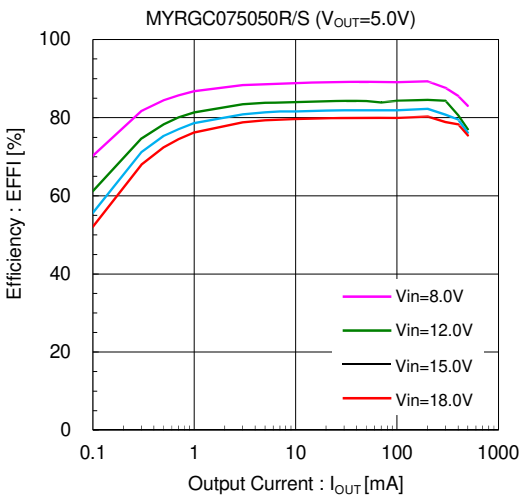
■TYPICAL PERFORMANCE CHARACTERISTICS

(2) Efficiency vs. Output Current



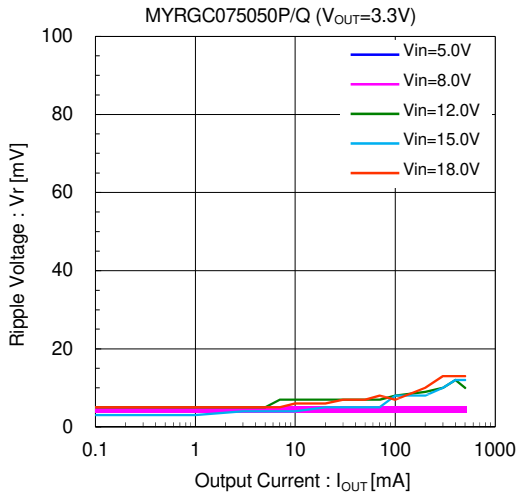


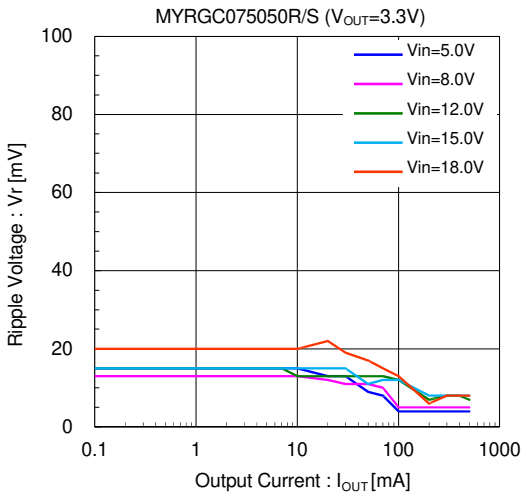


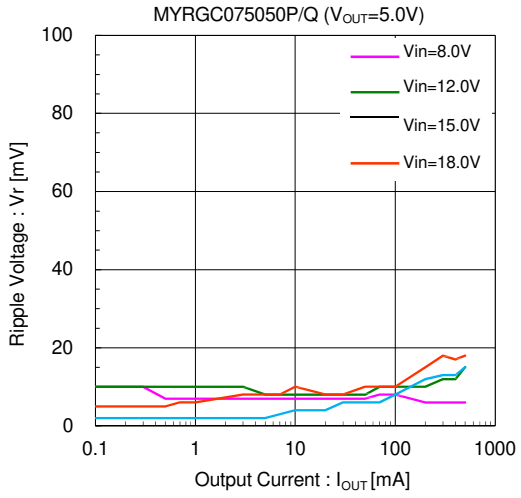


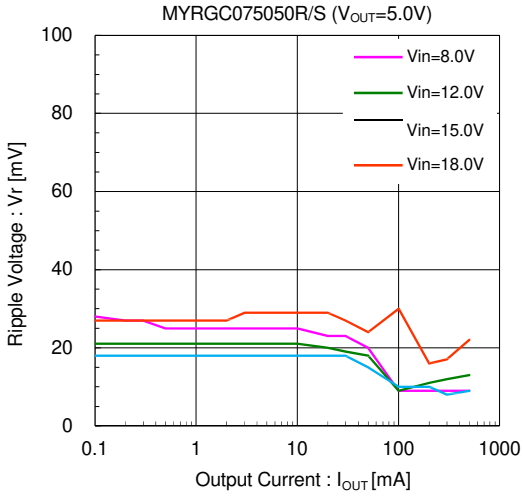
■TYPICAL PERFORMANCE CHARACTERISTICS

(3) Ripple Voltage vs. Output Current





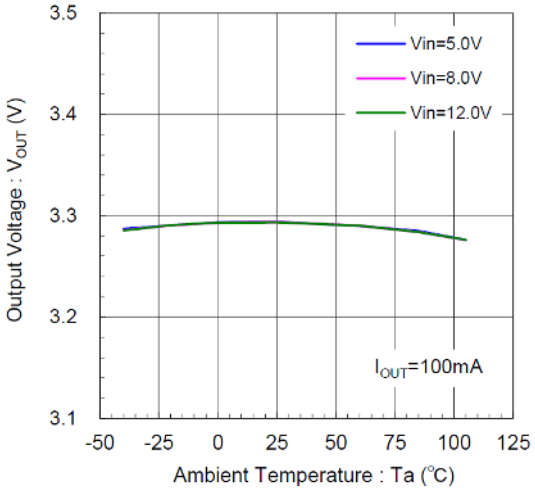




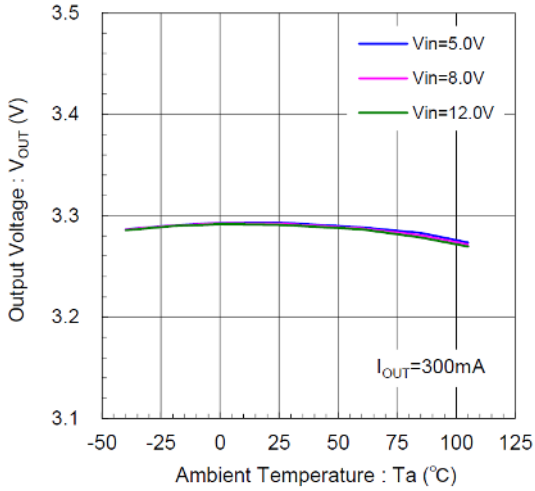
■TYPICAL PERFORMANCE CHARACTERISTICS

(4) Output Voltage vs. Ambient Temperature

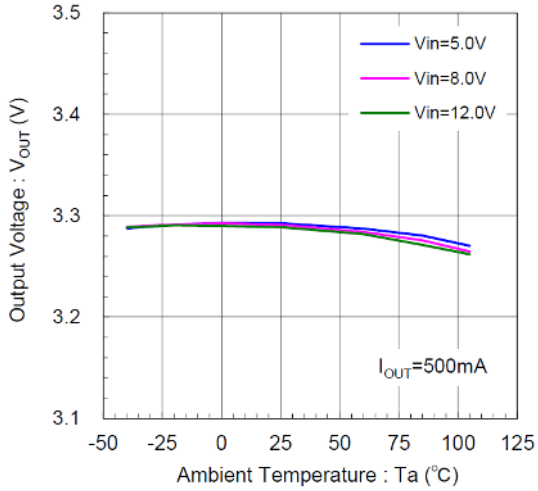
MYRGC075050P/Q (V_{OUT}=3.3V, I_{OUT}=100mA)



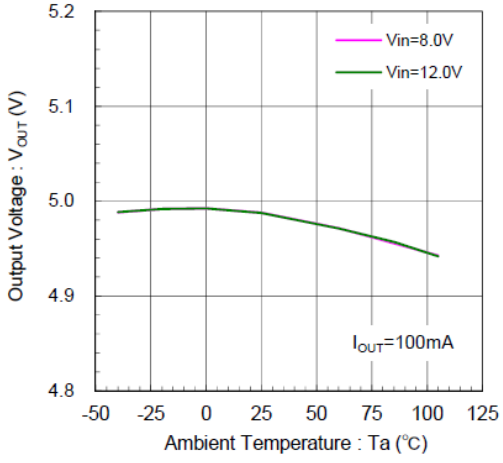
MYRGC075050P/Q (V_{OUT}=3.3V, I_{OUT}=300mA)



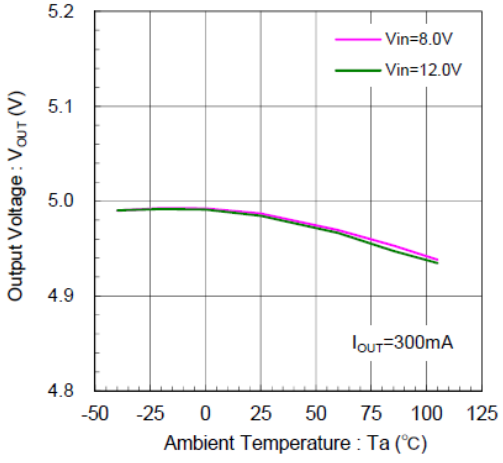
MYRGC075050P/Q (V_{OUT}=3.3V, I_{OUT}=500mA)



MYRGC075050P/Q (V_{OUT}=5.0V, I_{OUT}=100mA)

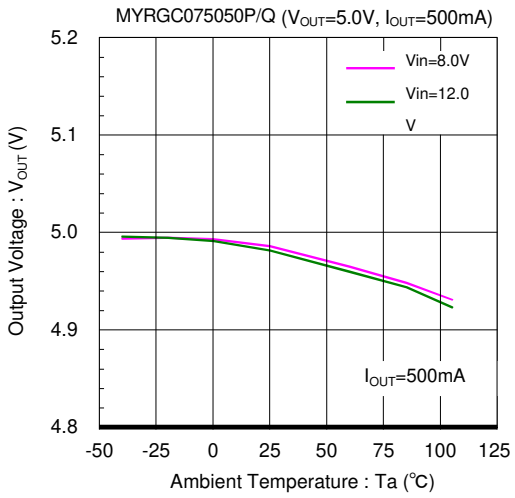


MYRGC075050P/Q (V_{OUT}=5.0V, I_{OUT}=300mA)

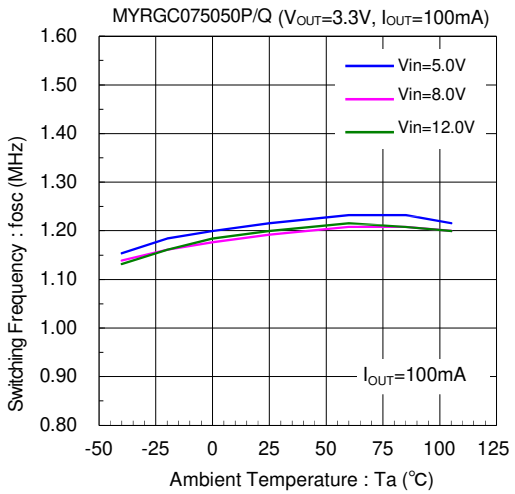


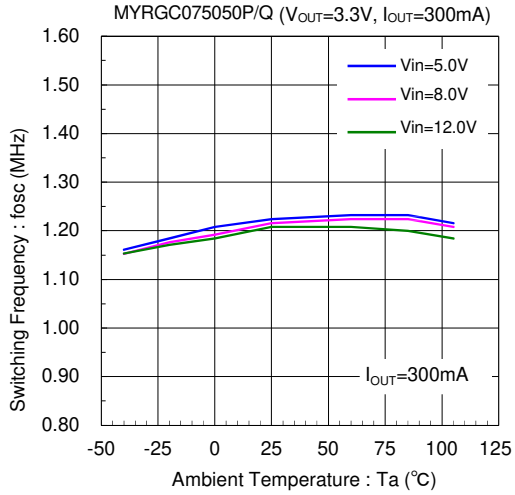
■TYPICAL PERFORMANCE CHARACTERISTICS

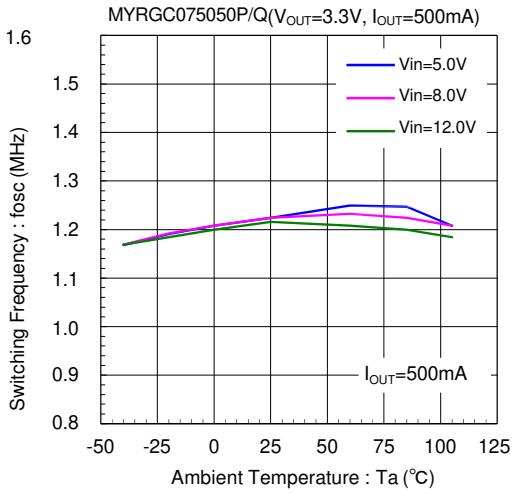
(4) Output Voltage vs. Ambient Temperature



(5) Switching Frequency vs. Ambient Temperature

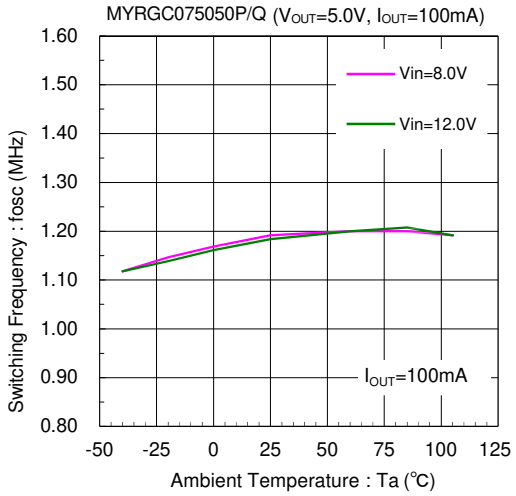


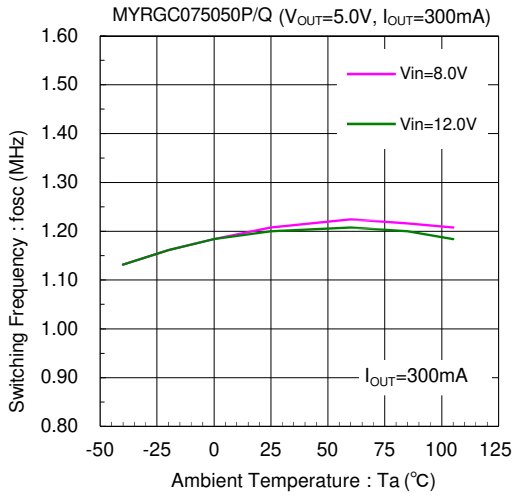


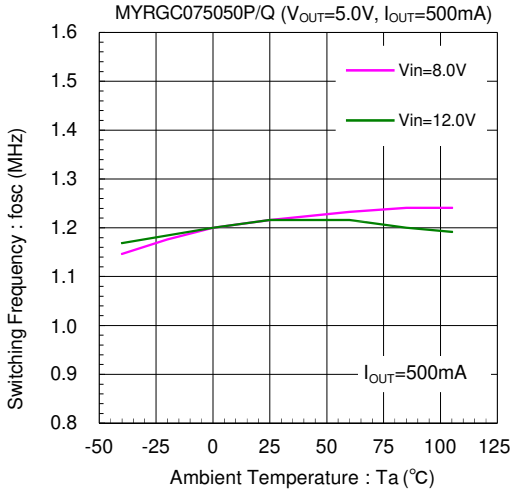


■TYPICAL PERFORMANCE CHARACTERISTICS

(5) Switching Frequency vs. Ambient Temperature

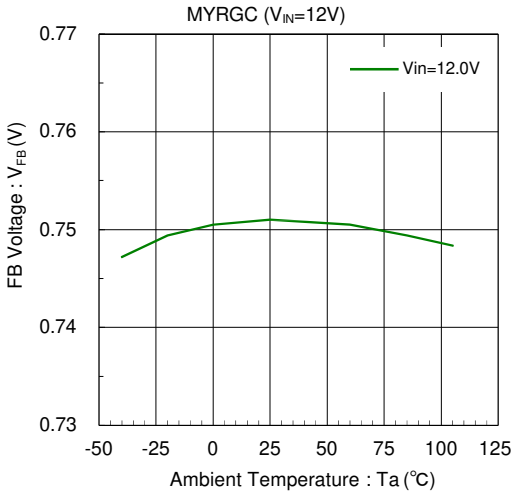




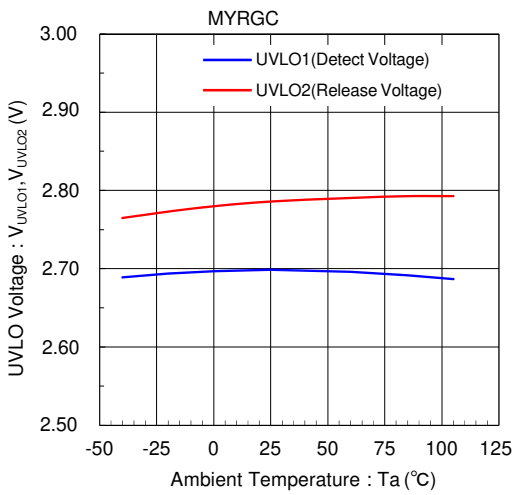


■TYPICAL PERFORMANCE CHARACTERISTICS

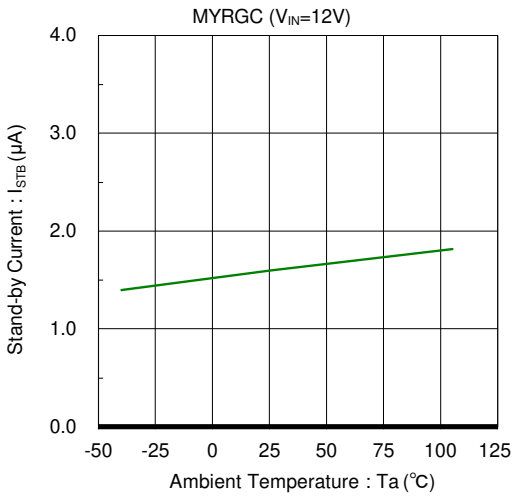
(6) FB Voltage vs. Ambient Temperature



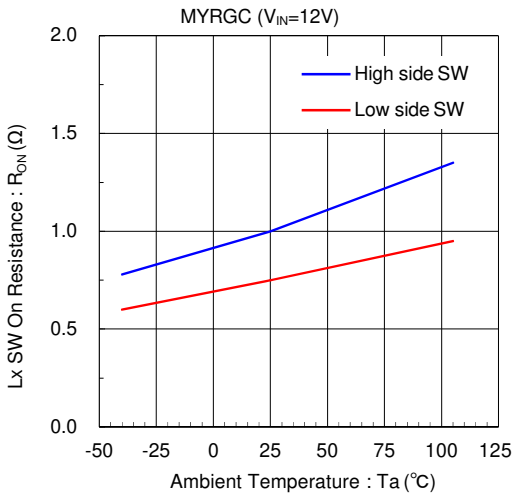
(7) UVLO Voltage vs. Ambient Temperature



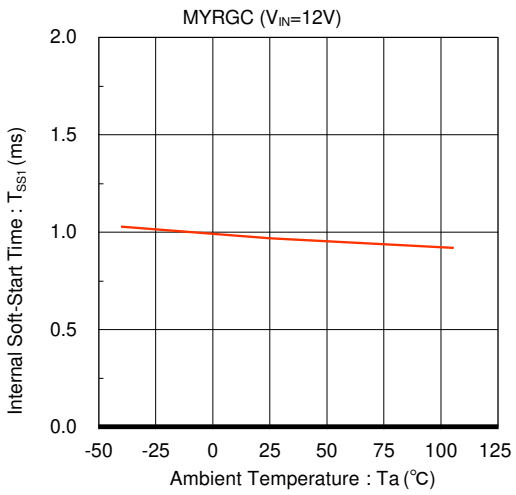
(8) Stand-by Current vs. Ambient Temperature



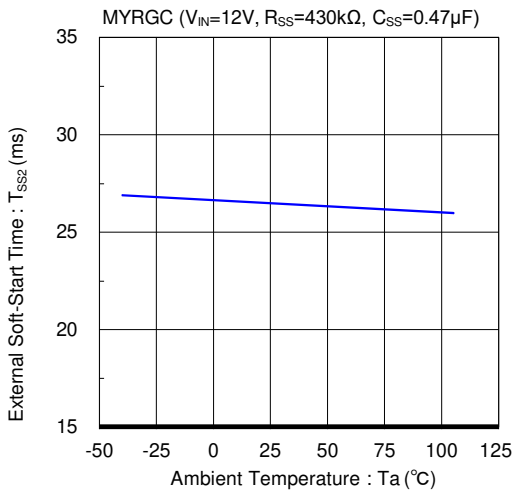
(9) Lx SW On Resistance vs. Ambient Temperature



(10) Internal Soft-Start Time vs. Ambient Temperature

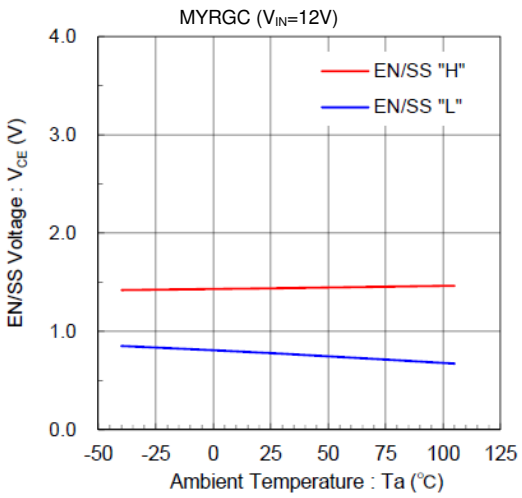


(11) External Soft-Start Time vs. Ambient Temperature

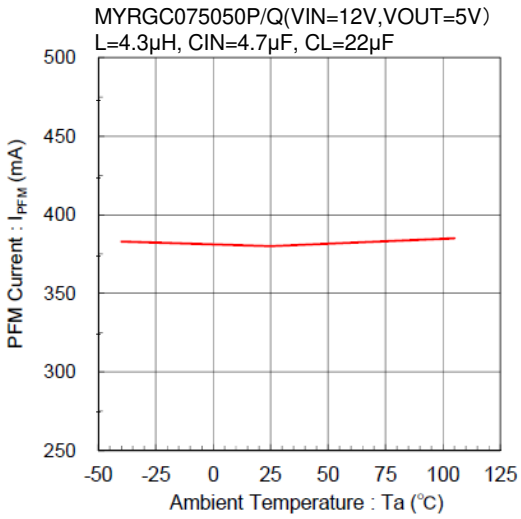


■TYPICAL PERFORMANCE CHARACTERISTICS

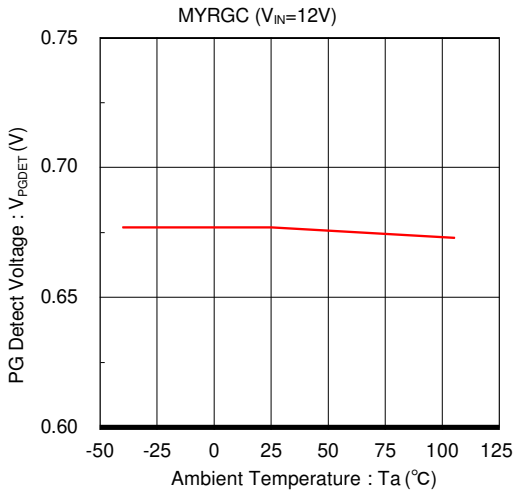
(12) EN/SS Voltage vs. Ambient Temperature



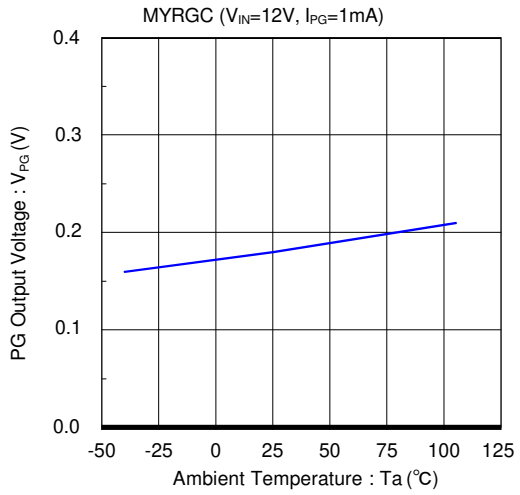
(13) PFM Current vs. Ambient Temperature



(14) PG Detect Voltage vs. Ambient Temperature



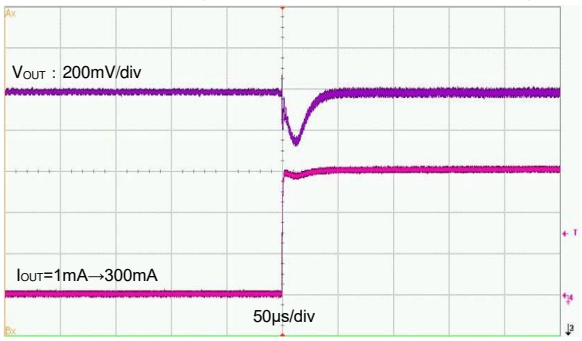
(15) PG Output Voltage vs. Ambient Temperature



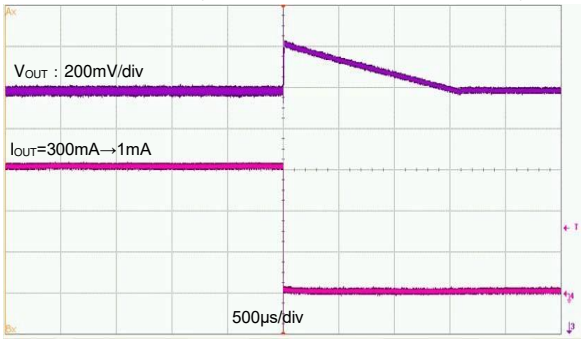
■TYPICAL PERFORMANCE CHARACTERISTICS

(16) Load Transient Response

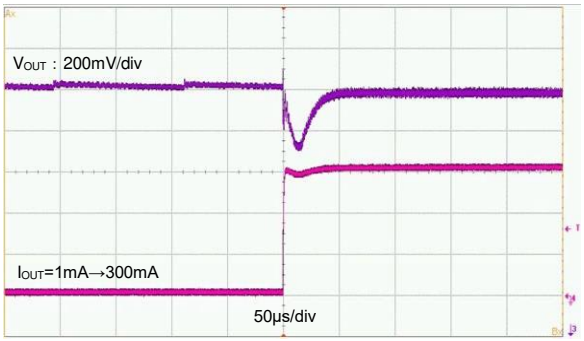
MYRGC075050P/Q (V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1mA→300mA)



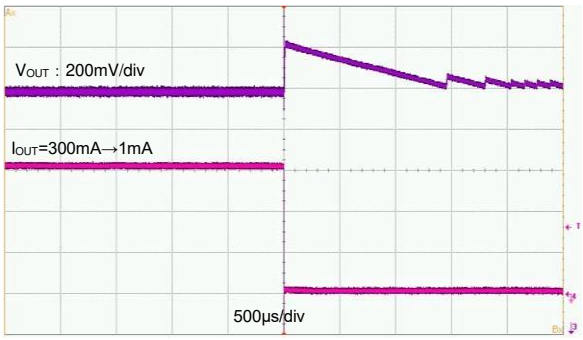
MYRGC075050P/Q (V_{IN}=12V, V_{OUT}=5V,I_{OUT}=300mA→1mA)



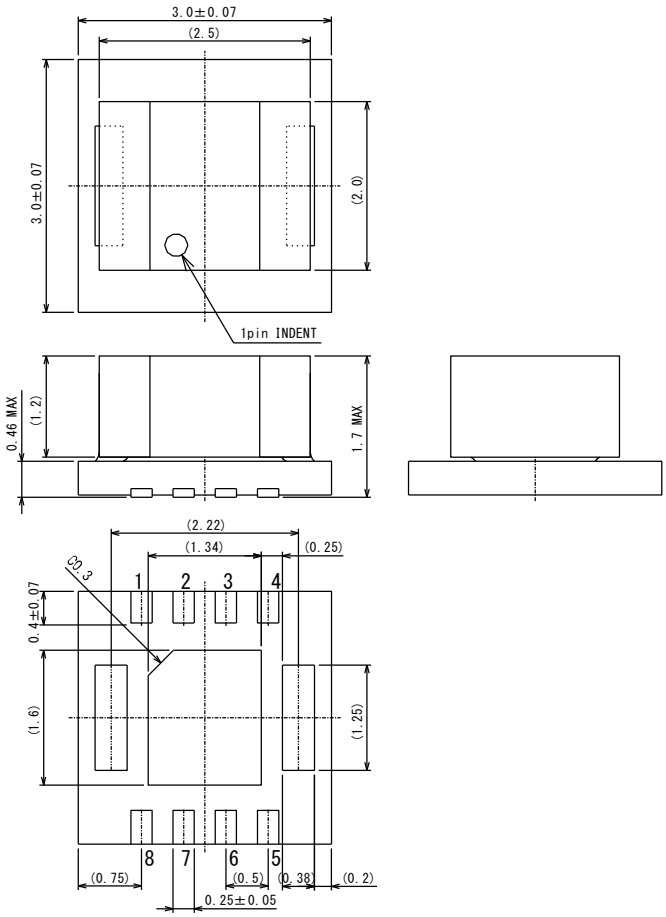
MYRGC075050R/S (V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1mA→300mA)



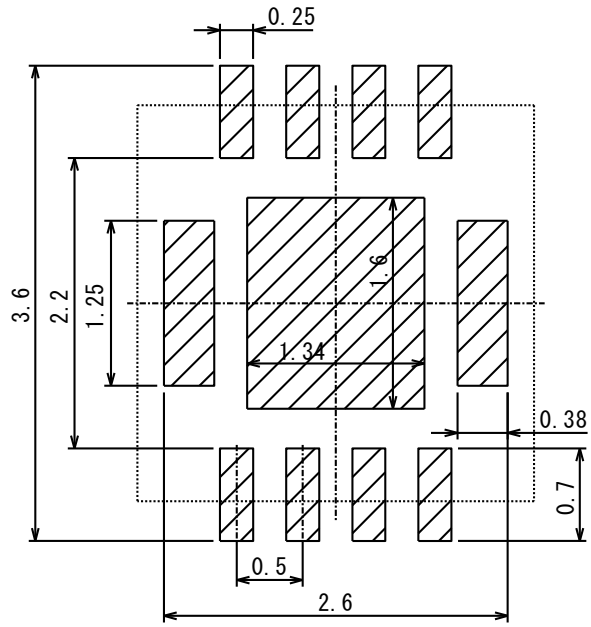
MYRGC075050R/S (V_{IN}=12V, V_{OUT}=5V, I_{OUT}=300mA→1mA)



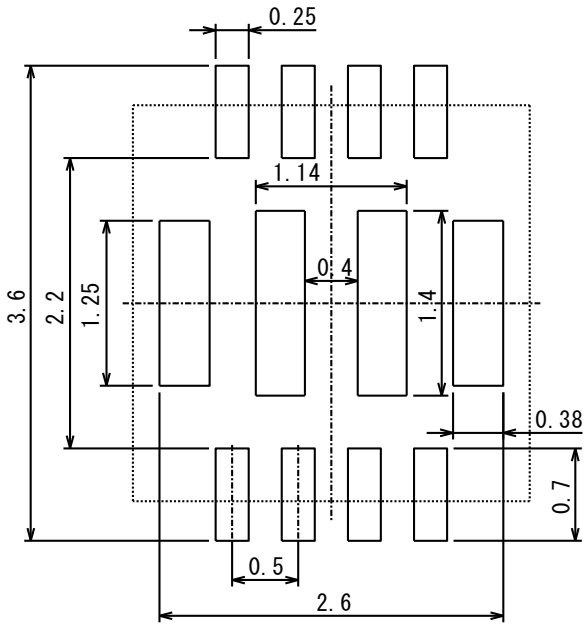
■PACKAGING INFORMATION



●Reference Pattern Layout (unit:mm)



●Reference Metal Mask Design (unit:mm)

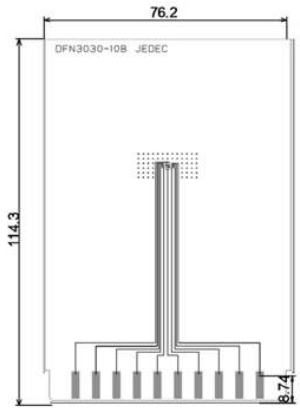


■PACKAGING INFORMATION

1.Power Dissipation (JEDEC board)

Power dissipation data for this packaging is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1.Measurement Condition (Reference data)
Condition : Mount on a board
Ambient : Natural convection
Soldering : Lead (Pb) free
Board : The board using 4 copper layer.
(76.2mm x 114.3mm・・・Area: about 8700mm^2)
1st layer : No copper foil (Signal layer)
2nd layer : 70mm x 70mm_Conected to heat-sink.
3rd layer : 70mm x 70mm_Conected to heat-sink.
4th layer : No copper foil (Signal layer)
Material : Glass Epoxy(FR-4)
Thickness : 1.6mm
Through-hole : 0.2mm x 60pcs

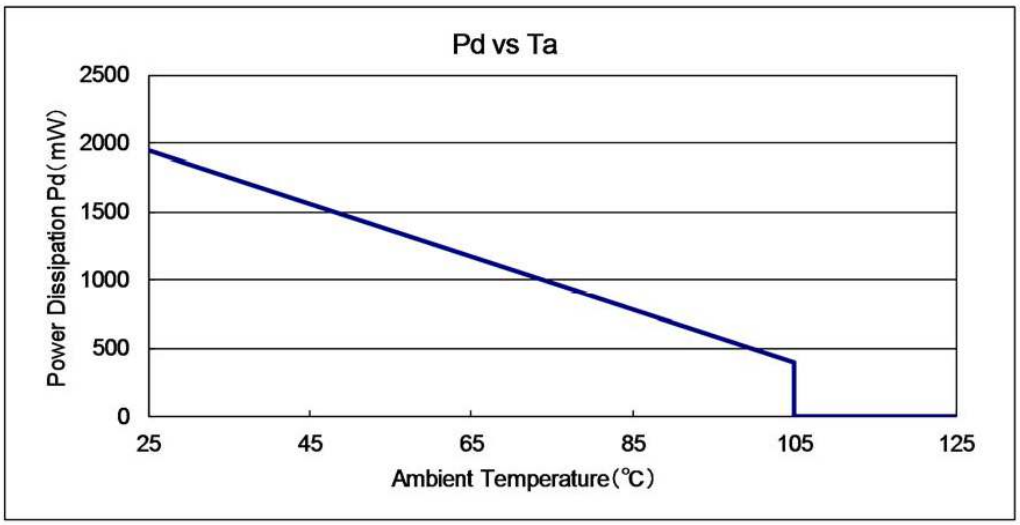


Evaluation Board (Unit: mm)

2.Power Dissipation vs. Ambient Temperature

Board Mount (Tj max = 125℃)

Ambient Temperature(℃)	Power Dissipation Pd(mW)	Thermal Resistance (℃/W)
25	1950	51.28
105	390	



■MARKING RULE

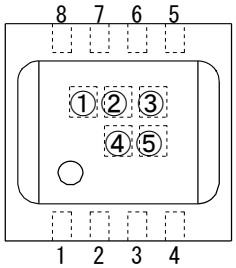
①,②,③ represents products series

SYMBOL			Switching Frequency	PRODUCT
①	②	③		
1	1	B	1	MYRGC075050P31RA
1	1	E	1	MYRGC075050Q31RA
1	1	K	1	MYRGC075050R31RA
1	1	N	1	MYRGC075050S31RA

④,⑤ represents production lot number

01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order. (G, I, J, O, Q, W excluded)

* No character inversion used.



1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

Murata Manufacturing Co., Ltd.