# BLA6H0912L-1000; BLA6H0912LS-1000

LDMOS avionics power transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

1000W LDMOS pulsed power transistor intended for avionics transmitter applications in the 960 MHz to 1215 MHz frequency range such as Mode-S, TCAS, JTIDS, DME and TACAN.

**Table 1. Application information**

*Typical RF performance at $T_{case}$ = 25 °C; $t_p$ = 50 μs; $\delta$ = 2 %; $I_{Dq}$ = 200 mA; in a class-AB application circuit.*

| Test signal | f | $V_{DS}$ | $P_L$ | $G_p$ | $\eta_D$ | $t_r$ | $t_f$ |
|---|---|---|---|---|---|---|---|
| | (MHz) | (V) | (W) | (dB) | (%) | (ns) | (ns) |
| pulsed RF | 1030 | 50 | 1000 | 16 | 52 | 11 | 5 |

### 1.2 Features and benefits

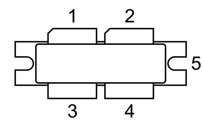
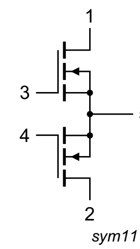
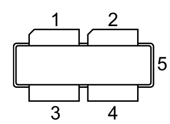
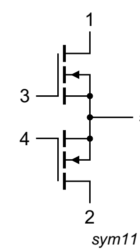
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (960 MHz to 1215 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- 1000 W LDMOS pulsed power transistor intended for Mode-S, TCAS, JTIDS, DME and TACAN applications in the 960 MHz to 1215 MHz frequency range

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| **BLA6H0912L-1000 (SOT539A)** | | | |
| 1 | drain1 |  |  |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source [1] | | |
| **BLA6H0912LS-1000 (SOT539B)** | | | |
| 1 | drain1 |  |  |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source [1] | | |

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BLA6H0912L-1000 | - | flanged balanced ceramic package; 2 mounting holes; 4 leads | SOT539A |
| BLA6H0912LS-1000 | - | earless flanged balanced ceramic package; 4 leads | SOT539B |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | - | 100 | V |
| $V_{GS}$ | gate-source voltage | | –0.5 | +13 | V |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | [1] | - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

# 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $Z_{th(j-c)}$ | transient thermal impedance from junction to case | $T_{case}$ = 80 °C; $P_L$ = 1000 W | | |
| | | $t_p$ = 50 μs; δ = 2 % | 0.011 | K/W |
| | | $t_p$ = 100 μs; δ = 10 % | 0.021 | K/W |
| | | $t_p$ = 200 μs; δ = 10 % | 0.025 | K/W |
| | | $t_p$ = 300 μs; δ = 10 % | 0.027 | K/W |
| | | $t_p$ = 2.4 ms; δ = 6.4 % | 0.041 | K/W |

# 6. Characteristics

**Table 6. DC characteristics**

*$T_j$ = 25 °C; per section unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 4 mA | 104 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS}$ = 10 V; $I_D$ = 400 mA | 1.25 | 1.8 | 2.25 | V |
| $I_{DSS}$ | drain leakage current | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V | - | - | 2.8 | μA |
| $I_{DSX}$ | drain cut-off current | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $V_{DS}$ = 10 V | - | 62 | - | A |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 11 V; $V_{DS}$ = 0 V | - | - | 280 | nA |
| $g_{fs}$ | forward transconductance | $V_{DS}$ = 10 V; $I_D$ = 20 A | - | 34 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $I_D$ = 14 A | - | 75 | - | mΩ |

**Table 7. RF characteristics**

*Test signal: pulsed RF; $t_p$ = 50 μs; δ = 2 %; RF performance at $V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $T_{case}$ = 25 °C; unless otherwise specified, in a class-AB production test circuit.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $P_L$ = 1000 W | - | - | 50 | V |
| $G_p$ | power gain | $P_L$ = 1000 W | 14 | 15.5 | - | dB |
| $RL_{in}$ | input return loss | $P_L$ = 1000 W | - | −19 | −11 | dB |
| $\eta_D$ | drain efficiency | $P_L$ = 1000 W | 47 | 51 | - | % |
| $P_{droop(pulse)}$ | pulse droop power | $P_L$ = 1000 W | - | 0 | 0.3 | dB |
| $t_r$ | rise time | $P_L$ = 1000 W | - | 11 | 30 | ns |
| $t_f$ | fall time | $P_L$ = 1000 W | - | 5 | 30 | ns |

# 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLA6H0912L-1000 and the BLA6H0912LS-1000 are capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the following conditions: $V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; $P_L$ = 1000 W; $t_p$ = 50 μs; δ = 2 %; f = 1030 MHz.

## 7.2 Impedance information

**Table 8. Typical impedance**
*Typical values per section unless otherwise specified.*

| f | $Z_S$ | $Z_L$ [1] | $Z_L$ [2] |
|---|---|---|---|
| (MHz) | (Ω) | (Ω) | (Ω) |
| 950 | 1.12 – j2.27 | 0.60 + j0.21 | 0.62 – j0.02 |
| 1000 | 1.39 – j2.69 | 0.54 + j0.08 | 0.66 – j0.06 |
| 1050 | 1.79 – j2.79 | 0.40 + j0.03 | 0.52 – j0.28 |
| 1100 | 2.44 – j2.72 | 0.41 – j0.12 | 0.67 – j0.29 |
| 1150 | 1.68 – j2.52 | 0.49 – j0.21 | 0.53 – j0.35 |
| 1200 | 4.68 – j2.97 | 0.36 – j0.30 | 0.57 – j0.40 |

[1] Optimized for drain efficiency.

[2] Optimized for power gain.

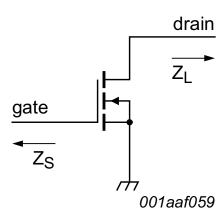
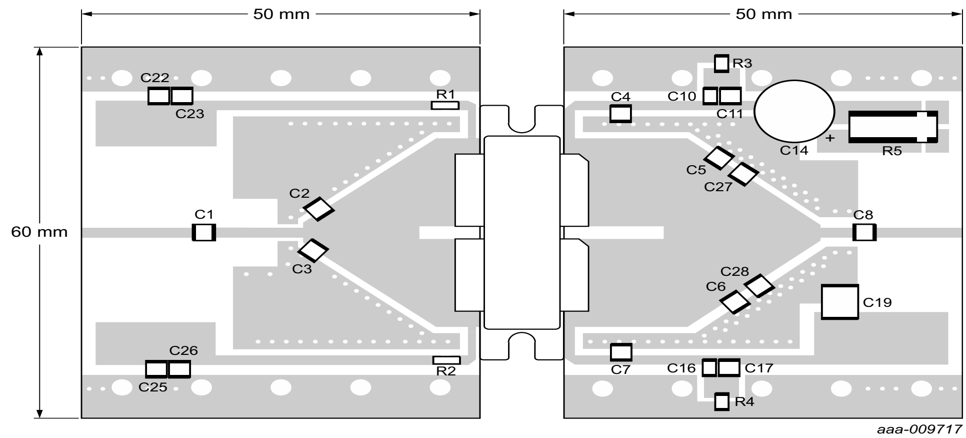



**Fig 1. Definition of transistor impedance**

### 7.3 Circuit information




Printed-Circuit Board (PCB) material: Rogers Duroid 6002 with $\varepsilon_r$ = 2.94 and thickness = 0.762 mm.

See Table 9 for list of components.

**Fig 2. Component layout**

**Table 9. List of components**

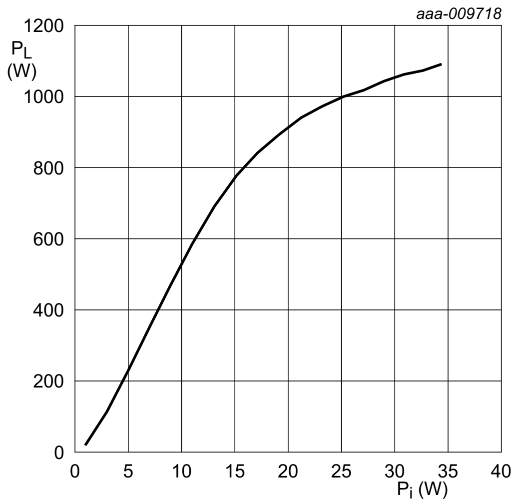
*See Figure 2 for component layout.*

| Component | Description | Value | Remarks |
|---|---|---|---|
| C1, C4, C7, C8, C22, C25 | multilayer ceramic chip capacitor | 33 pF [1] | |
| C2, C3, C27, C28 | multilayer ceramic chip capacitor | 6.2 pF [1] | |
| C5, C6 | multilayer ceramic chip capacitor | 3.9 pF [1] | |
| C23, C26 | multilayer ceramic chip capacitor | 1 nF [1] | |
| C10, C16 | multilayer ceramic chip capacitor | 10 nF | Murata |
| C11, C17 | multilayer ceramic chip capacitor | 100 nF | TDK |
| C14 | electrolytic capacitor | 220 μF, 63 V | |
| C19 | multilayer ceramic chip capacitor | 10 μF, 100 V | |
| R1 | SMD resistor | 1 kΩ | SMD 0603 |
| R2 | SMD resistor | 20 Ω | SMD 0603 |
| R3, R4 | SMD resistor | 2.4 Ω | SMD 0603 |
| R5 | current sense resistor | 0.005 Ω | |

[1] American Technical Ceramics type 100B or capacitor of same quality.

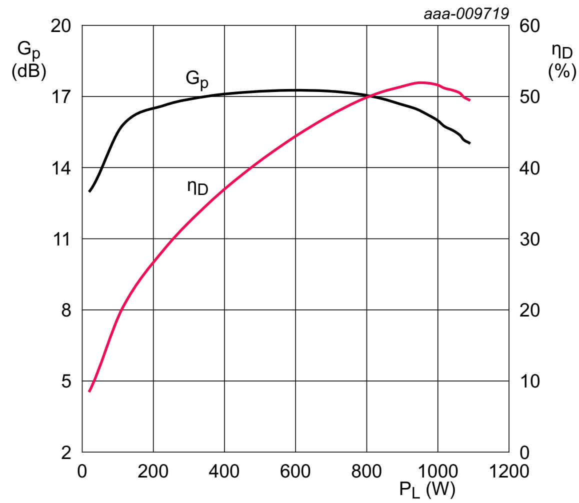
## 7.4 Graphical data

### 7.4.1 Pulsed CW



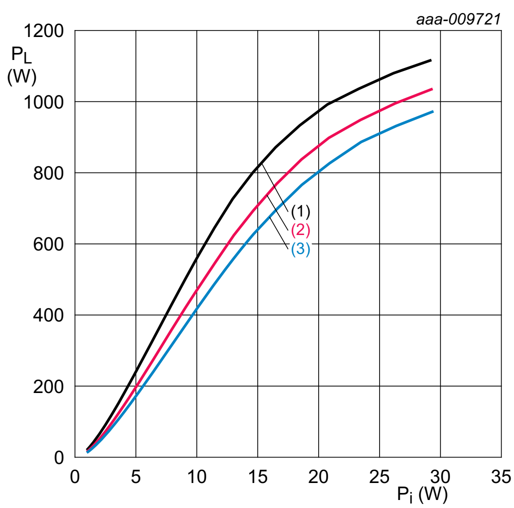

$V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $t_p$ = 50 μs; δ = 2 %.

**Fig 3. Output power as a function of input power; typical values**




$V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $t_p$ = 50 μs; δ = 2 %.

**Fig 4. Power gain and drain efficiency as function of output power; typical values**



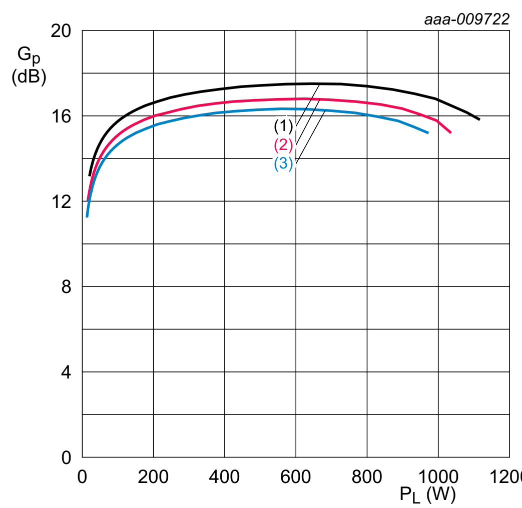

$V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $t_p$ = 50 μs; δ = 2 %.

(1) $T_{case}$ = 20 °C

(2) $T_{case}$ = 50 °C

(3) $T_{case}$ = 70 °C

**Fig 5. Output power as a function of input power; typical values**



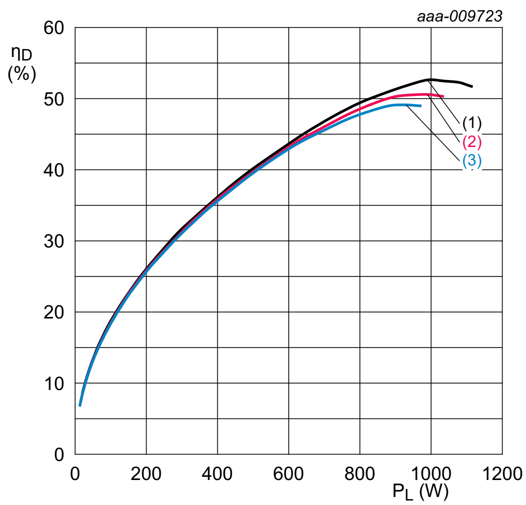

$V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $t_p$ = 50 μs; δ = 2 %.

(1) $T_{case}$ = 20 °C

(2) $T_{case}$ = 50 °C

(3) $T_{case}$ = 70 °C

**Fig 6. Power gain as a function of output power; typical values**



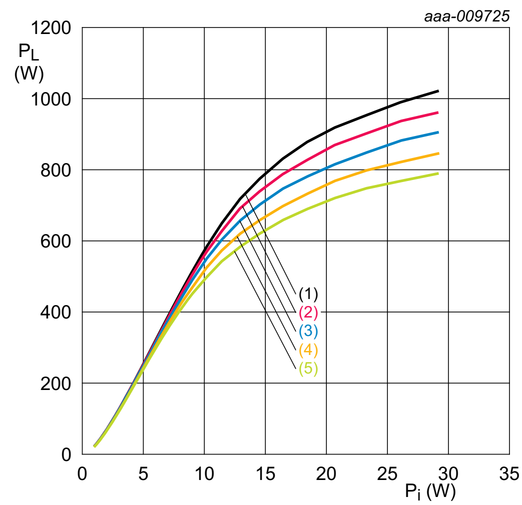

$V_{DS}$ = 50 V; $I_{Dq}$ = 200 mA; f = 1030 MHz; $t_p$ = 50 μs; δ = 2 %.

(1) $T_{case}$ = 20 °C

(2) $T_{case}$ = 50 °C

(3) $T_{case}$ = 70 °C

**Fig 7. Drain efficiency as a function of output power; typical values**




$I_{Dq}$ = 200 mA; $t_p$ = 50 μs; δ = 2 %.

(1) $V_{DS}$ = 50 V

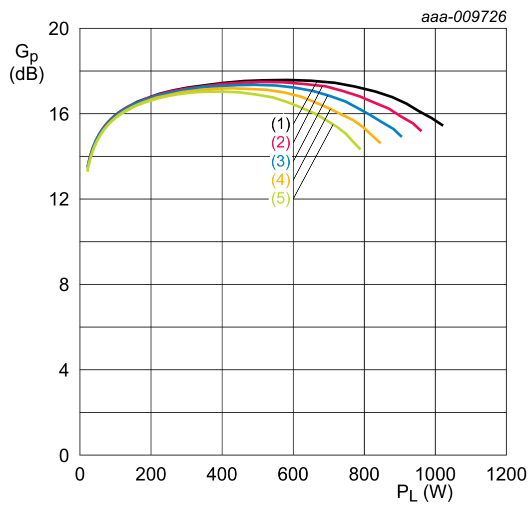
(2) $V_{DS}$ = 48 V

(3) $V_{DS}$ = 46 V

(4) $V_{DS}$ = 44 V

(5) $V_{DS}$ = 42 V

**Fig 8. Output power as a function of input power; typical values**




$I_{Dq}$ = 200 mA; $t_p$ = 50 μs; δ = 2 %.

(1) $V_{DS}$ = 50 V

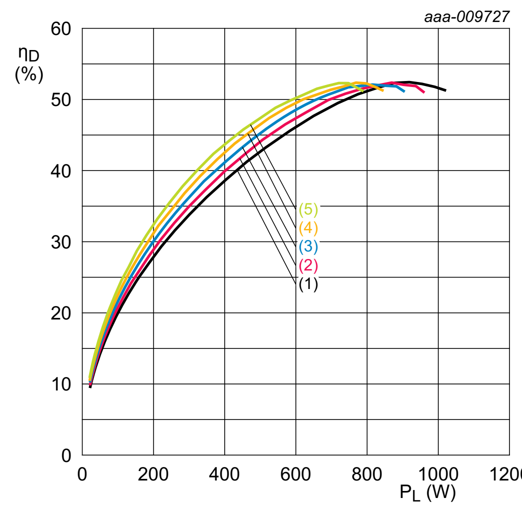
(2) $V_{DS}$ = 48 V

(3) $V_{DS}$ = 46 V

(4) $V_{DS}$ = 44 V

(5) $V_{DS}$ = 42 V

**Fig 9. Power gain as a function of output power; typical values**




$I_{Dq}$ = 200 mA; $t_p$ = 50 μs; δ = 2 %.

(1) $V_{DS}$ = 50 V

(2) $V_{DS}$ = 48 V

(3) $V_{DS}$ = 46 V

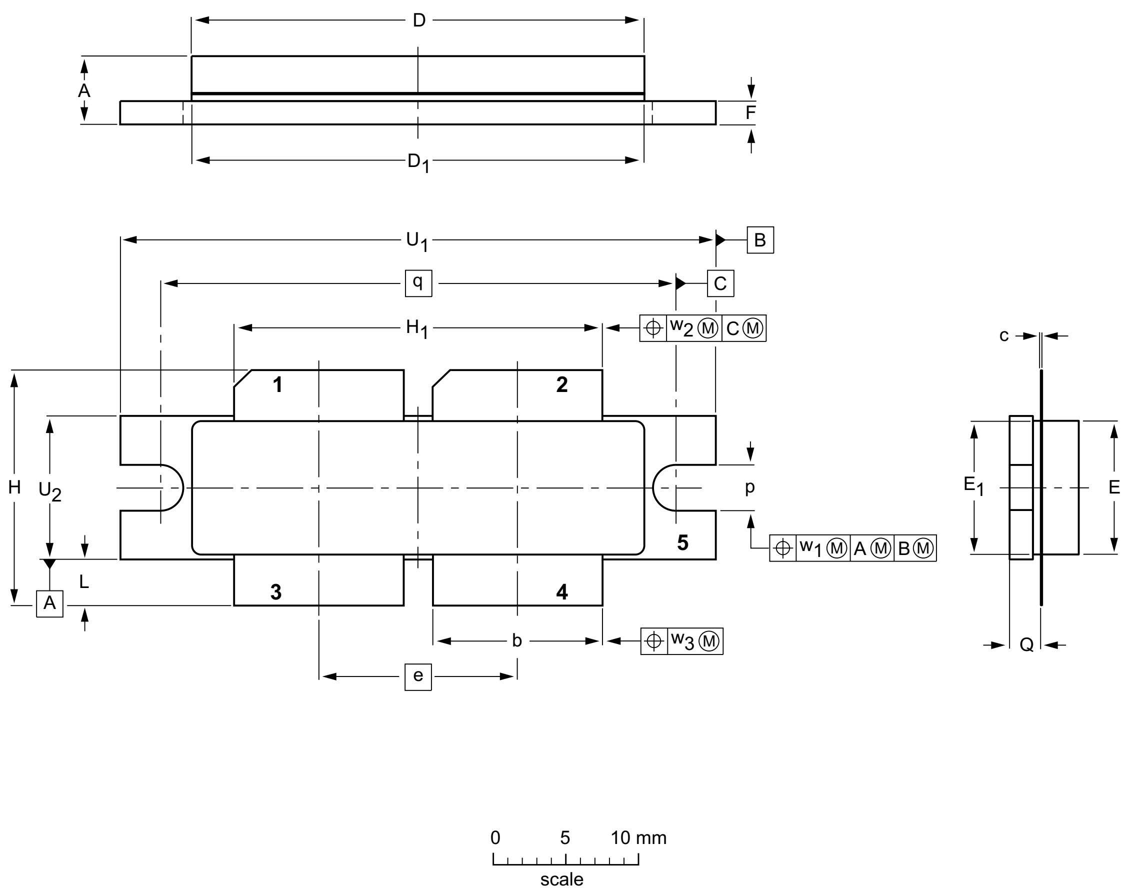
(4) $V_{DS}$ = 44 V

(5) $V_{DS}$ = 42 V

**Fig 10. Drain efficiency as a function of output power; typical values**

## 8. Package outline

**Flanged balanced ceramic package; 2 mounting holes; 4 leads** **SOT539A**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

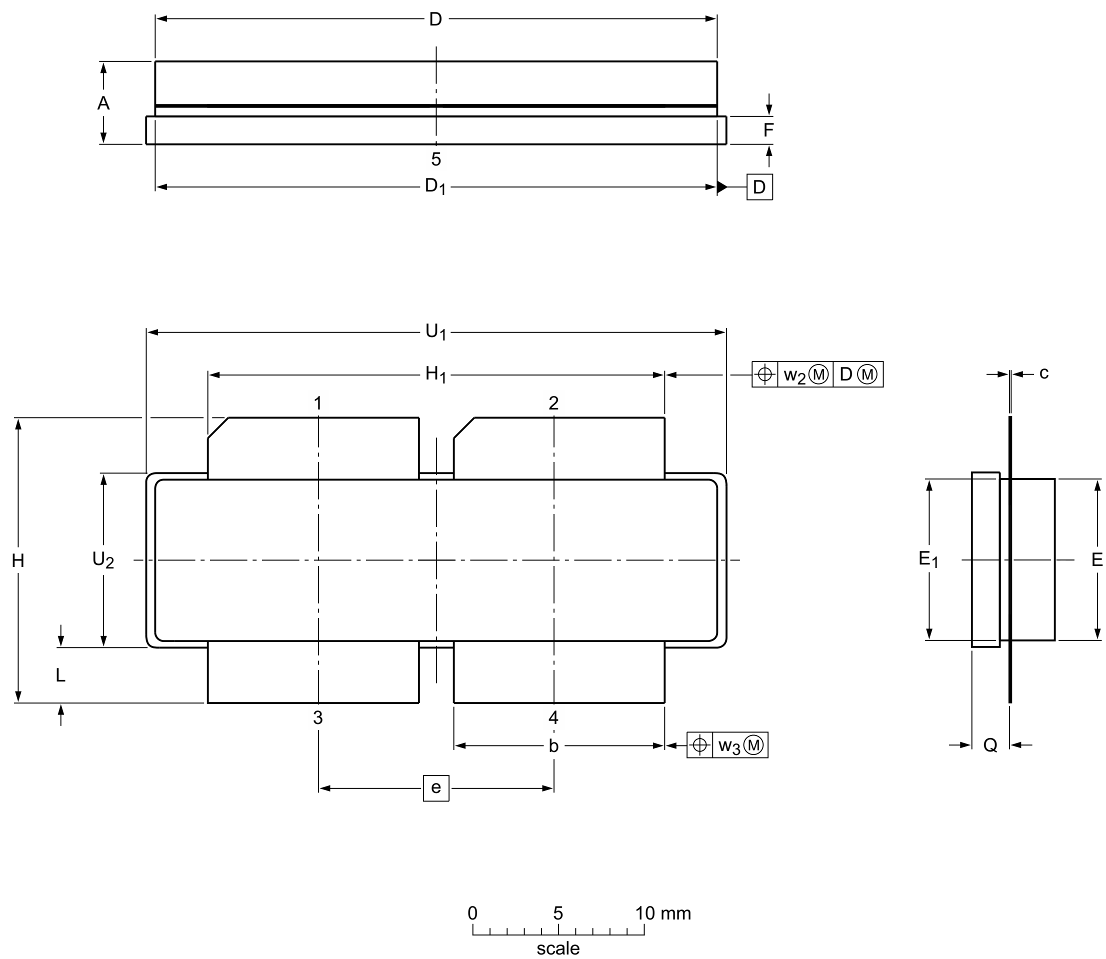
| UNIT | A | b | c | D | $D_1$ | e | E | $E_1$ | F | H | $H_1$ | L | p | Q | q | $U_1$ | $U_2$ | $w_1$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7<br>4.2 | 11.81<br>11.56 | 0.18<br>0.10 | 31.55<br>30.94 | 31.52<br>30.96 | 13.72 | 9.50<br>9.30 | 9.53<br>9.27 | 1.75<br>1.50 | 17.12<br>16.10 | 25.53<br>25.27 | 3.48<br>2.97 | 3.30<br>3.05 | 2.26<br>2.01 | 35.56 | 41.28<br>41.02 | 10.29<br>10.03 | 0.25 | 0.51 | 0.25 |
| inches | 0.185<br>0.165 | 0.465<br>0.455 | 0.007<br>0.004 | 1.242<br>1.218 | 1.241<br>1.219 | 0.540 | 0.374<br>0.366 | 0.375<br>0.365 | 0.069<br>0.059 | 0.674<br>0.634 | 1.005<br>0.995 | 0.137<br>0.117 | 0.130<br>0.120 | 0.089<br>0.079 | 1.400 | 1.625<br>1.615 | 0.405<br>0.395 | 0.010 | 0.020 | 0.010 |

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT539A | | | | | | ~~10-02-02~~<br>12-05-02 |

**Fig 11. Package outline SOT539A**

**Earless flanged balanced ceramic package; 4 leads** **SOT539B**




Dimensions

| Unit(1) | | A | b | c | D | $D_1$ | E | $E_1$ | e | F | H | $H_1$ | L | Q | $U_1$ | $U_2$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 4.7 | 11.81 | 0.18 | 31.55 | 31.52 | 9.5 | 9.53 | | 1.75 | 17.12 | 25.53 | 3.48 | 2.26 | 32.39 | 10.29 | | |
| | nom | | | | | | | | 13.72 | | | | | | | | 0.25 | 0.25 |
| | min | 4.2 | 11.56 | 0.10 | 30.94 | 30.96 | 9.3 | 9.27 | | 1.50 | 16.10 | 25.27 | 2.97 | 2.01 | 32.13 | 10.03 | | |
| inches | max | 0.185 | 0.465 | 0.007 | 1.242 | 1.241 | 0.374 | 0.375 | | 0.069 | 0.674 | 1.005 | 0.137 | 0.089 | 1.275 | 0.405 | | |
| | nom | | | | | | | | 0.54 | | | | | | | | 0.01 | 0.01 |
| | min | 0.165 | 0.455 | 0.004 | 1.218 | 1.219 | 0.366 | 0.365 | | 0.059 | 0.634 | 0.995 | 0.117 | 0.079 | 1.265 | 0.395 | | |

Note

1. millimeter dimensions are derived from the original inch dimensions.

*sot539b_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT539B | | | | | | ~~12-05-02~~<br>13-05-24 |

**Fig 12. Package outline SOT539B**

## 9. Handling information

| CAUTION | |
|---|---|
|  | This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.<br>Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards. |

## 10. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CW | Continuous Wave |
| DME | Distance Measuring Equipment |
| ESD | ElectroStatic Discharge |
| JTIDS | Joint Tactical Information Distribution System |
| LDMOS | Laterally Diffused Metal-Oxide Semiconductor |
| Mode-S | Mode Select |
| MTF | Median Time to Failure |
| SMD | Surface Mounted Device |
| TACAN | TACtical Air Navigation |
| TCAS | Traffic Collision Avoidance System |
| VSWR | Voltage Standing-Wave Ratio |

## 11. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BLA6H0912L-1000_0912LS-1000#5 | 20150901 | Product data sheet | - | BLA6H0912L-1000_0912LS-1000 v.4 |
| Modifications | • The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| BLA6H0912L-1000_0912LS-1000 v.4 | 20150702 | Product data sheet | - | BLA6H0912L-1000_0912LS-1000 v.3 |
| BLA6H0912L-1000_0912LS-1000 v.3 | 20150615 | Product data sheet | - | BLA6H0912L-1000_0912LS-1000 v.2 |
| BLA6H0912L-1000_0912LS-1000 v.2 | 20140210 | Objective data sheet | - | BLA6H0912L-1000_0912LS-1000 v.1 |
| BLA6H0912L-1000_0912LS-1000 v.1 | 20131104 | Objective data sheet | - | - |

# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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## 13. Contact information

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