DAC31x4 EVM User's Guide

This document is intended to serve as a basic user's guide for the DAC31x4 EVM Revision A. The EVM provides a basic platform to evaluate the DAC31x4, which is a 500 MSPS high-speed digital-to-analog converter. The DAC3174 is a dual-channel DAC with 14-bit LVDS input. DAC3174 is pin compatible with the dual-channel, 12-/10-bit, 500 MSPS digital-to-analog converter, DAC3164 and DAC3154. The DAC3174 EVM GUI can be used for DAC31x4 EVM.

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1 Introduction

1.1 Overview

The EVM includes the CDCE62005 clocking source which provides the clocks required for the DAC and the pattern generator. The on-board TRF3705-15 modulator provides on-board IF-to-RF up-conversion for basic transmitter evaluation. This EVM is ideally suited for mating with the TSW1400 pattern generation card for evaluating WCDMA, LTE, or other high-performance modulation schemes.

1.2 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW1400 used for pattern generation.

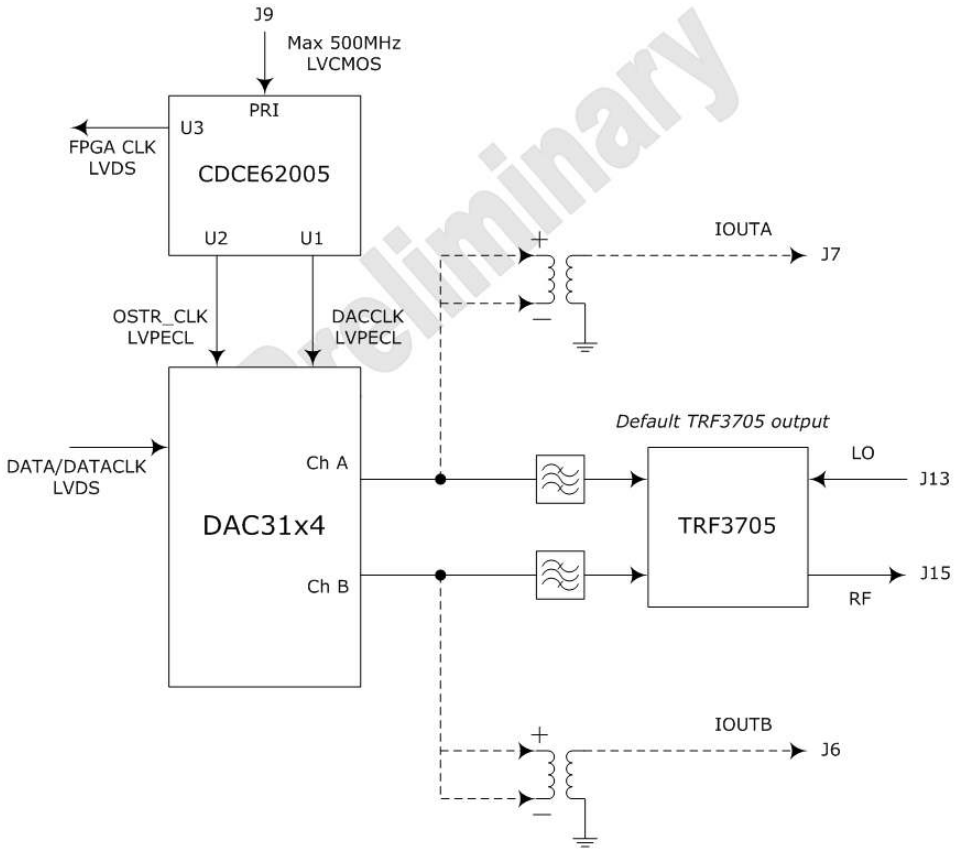

Figure 1. EVM Block Diagram

2 Software Control

2.1 Installation Instructions

- Open the folder named DAC3174_Installer_vxpx (xpx represents the latest version)
- Run Setup.exe
- Follow the on-screen instructions
- Once installed, launch by clicking on the DAC3174_GUI_vxpx program in Start → Texas Instruments DACs
- When plugging in the USB cable for the first time, you are prompted to install the USB drivers.
  - When a pop-up screen opens, select *Continue Downloading*
  - Follow the on-screen instructions to install the USB drivers
  - If needed, you can access the drivers directly in the install directory, C:\Program Files (x86)\Texas Instruments\DAC3174 for Windows® 7 and C:\Program Files\Texas Instruments\DAC3174 for Windows XP.

2.2 Software Operation

The software allows programming control of the DAC and CDCE devices. The front panel provides a tab for full programming of each. The GUI tabs provide a more convenient and simplified interface to the most-used registers of each device.

2.2.1 Input Control Options

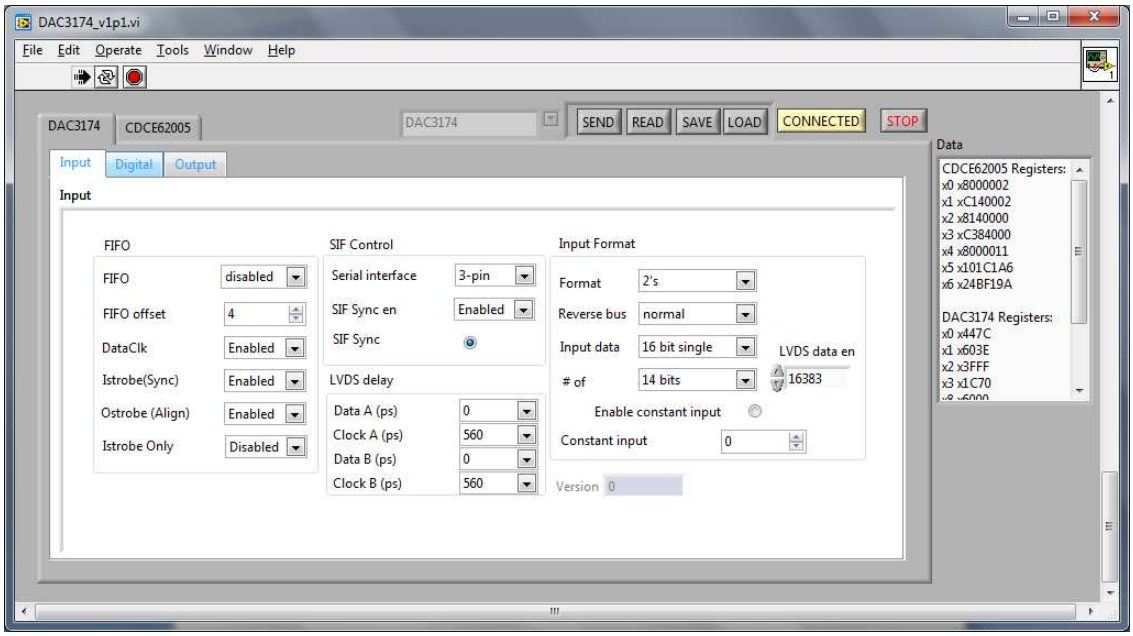

Figure 2. Input Control Options

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS data or LVDS data clock to help meet the input setup and hold time.
- SIF Control: provides control of the Serial Interface (3-wires or 4-wires) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (that is, 2s complement or offset binary).

2.2.2 Digital Block Options

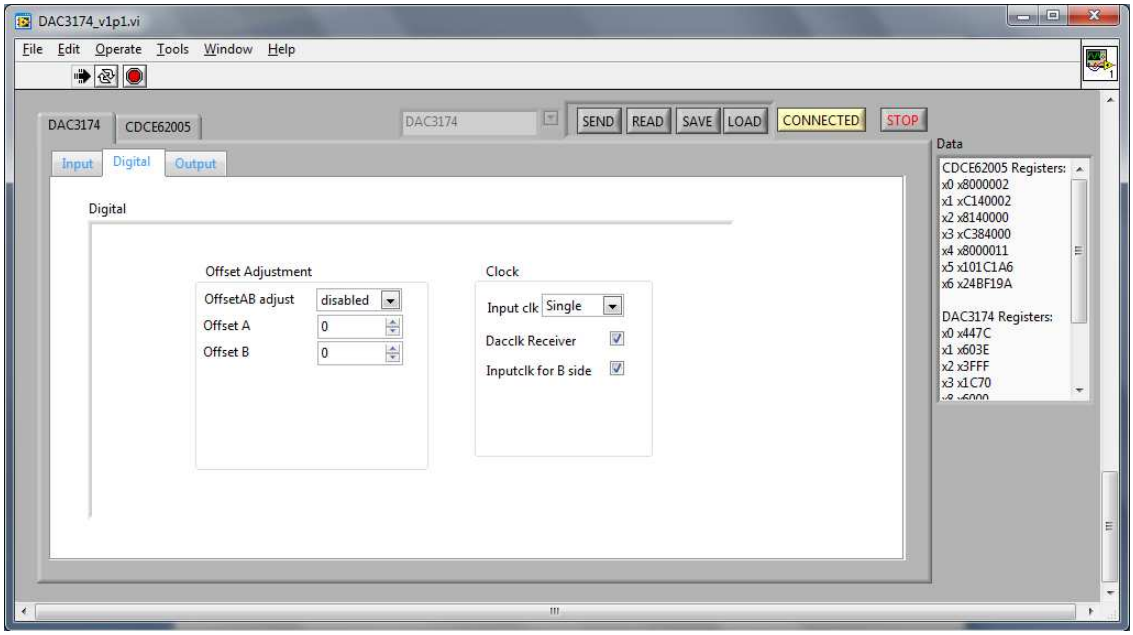

Figure 3. Digital Filtering Options

- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Offset Adjustment: allows adjustment of DC offset to minimize the LO feed-through of the modulator output. Writing the register for Offset B causes an autosync generation in the QMOFFSET block.

2.2.3 Output Control Options

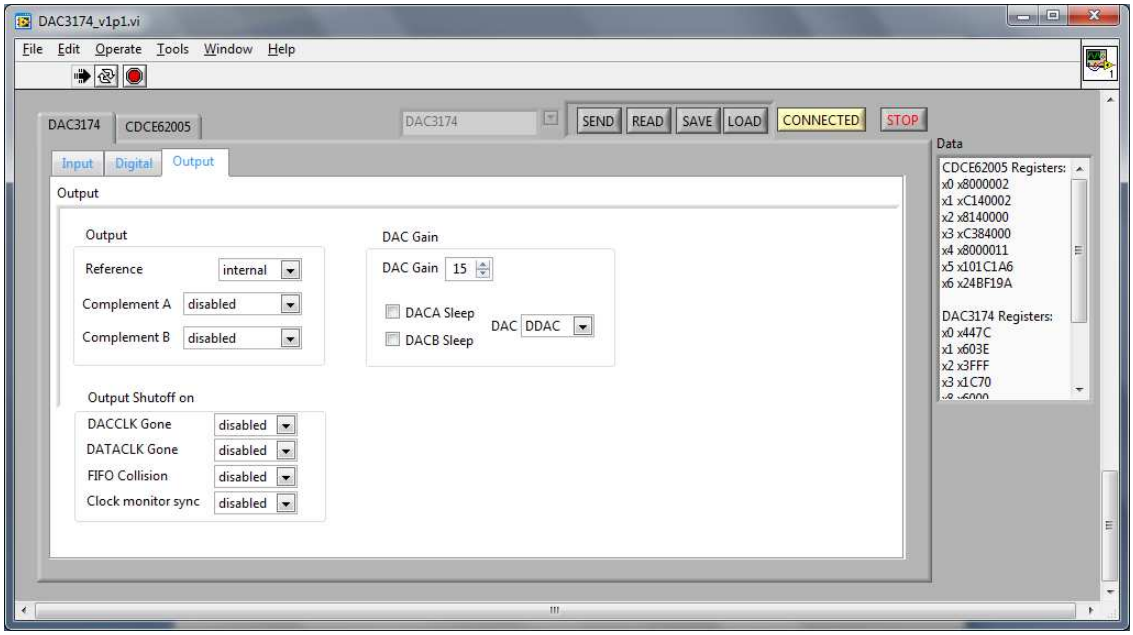

Figure 4. Output Control Options

- Output: allows the configuration of reference, output polarity, and output delay
- DAC Gain: configures the full-scale DAC current and DAC3174 mode

  - DAC Gain = 15 for 20-mA full-scale current
  - DAC3174 = DDAC
- Output Shutoff On: allows outputs to shut-off when alarm event occurs

2.2.4 CDCE62005

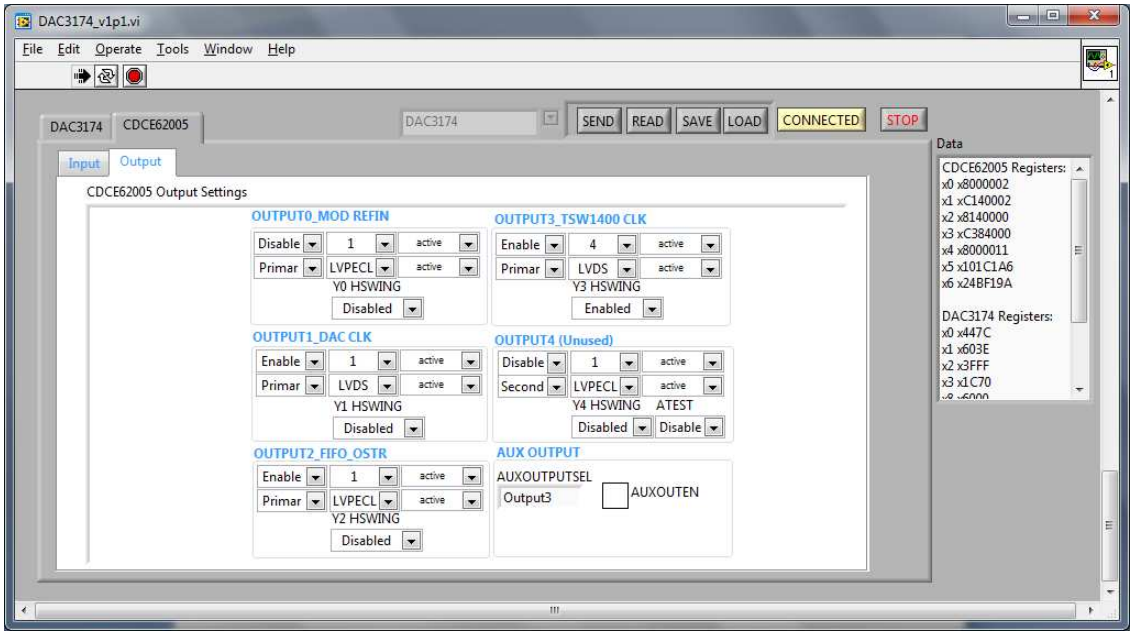

Figure 5. CDCE62005 Tab Configured for DAC3174

Clock frequency control is determined by register values in the CDC tab. Please refer to the CDCE62005 datasheet for detailed explanations of the register configuration to change the clock frequency.

The following CDCE62005 outputs are critical to proper operation of the DAC3174:

- OUTPUT1_DAC_CLK: DAC3174 Sampling clock
- OUTPUT3_TSW1400_CLK: TSW1400 FPGA clock

Configure the CDCE62005 registers with the following steps:

1. Open the DAC3174 GUI
2. Click the **Load Regs** button
3. Open the *dac3174_reg.txt* file.

This automatically configures the CDCE62005 registers.

2.2.5 Register Control

- Send All: Sends the register configuration to all devices
- Read All: Reads register configuration from the DAC3174 device
- Load Regs: Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory.
  - Select *Load Regs* button
  - Double click the *data* folder
  - Double click the desired register file
  - Clicking *Send All* ensures all the values are loaded properly
- Save Regs: Saves the register configuration for all devices

2.2.6 Miscellaneous Settings

- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address.

NOTE: It is recommended to reset the board and select the **Reset USB** button after every power cycle.

- Exit: Stops the program

3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test set-up for general testing of the DAC31x4 with the TSW1400 pattern generation card is shown in Figure 6

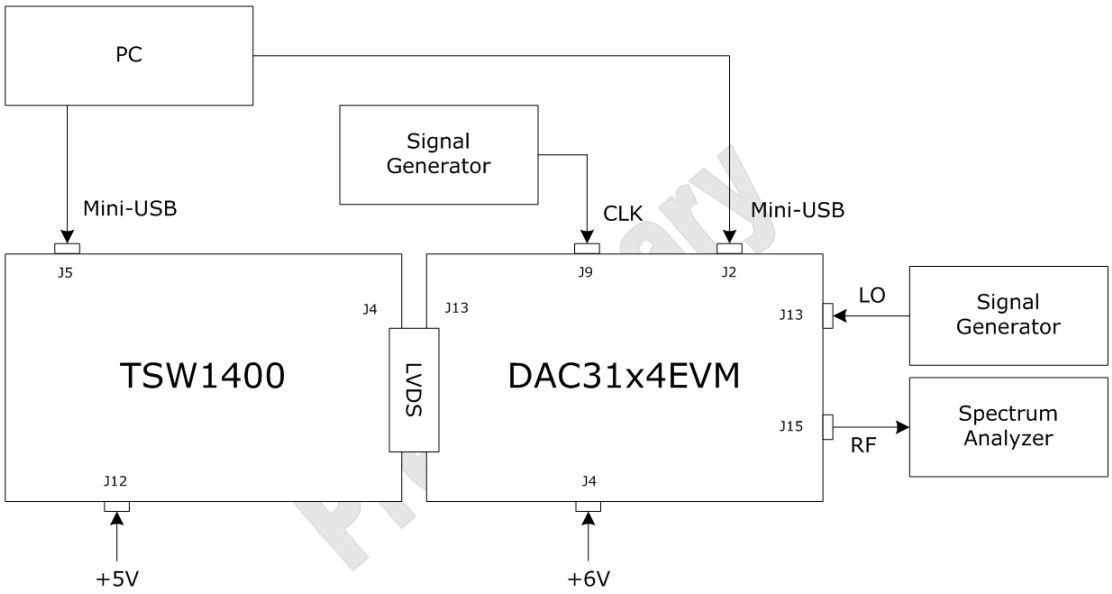

Figure 6. Test Setup Block Diagram

3.2 Test Set-up Connection

- TSW1400 Pattern Generator
  1. Connect the 5-V power supply to J12, the 5V_IN jack of the TSW1400 EVM.
  2. Connect the PC's USB port to J5, the mini-USB port of the TSW1400.
- DAC31x4 EVM
  1. Connect the J13 connector of DAC31x4 EVM to the J4 connector of TSW1400 EVM.
  2. Connect 6 V to J3, the power in jack of the DAC31x4 EVM.
  3. Connect the PC's USB port to J2, the USB port of the DAC31x4 EVM. Use a standard A to mini-B connector cable.
  4. Provide a 1.5-Vrms, 500-MHz max clock at J9, the *CLKIN* SMA port of the DAC31x4 EVM.
  5. Provide 12-dBm maximum, 300-MHz to 4-GHz LO source at the J13 port of the DAC31x4 EVM. This provides the LO source to the TRF3705-15 modulators.
  6. Connect the RF output port of J15 to the spectrum analyzer.

3.3 TSW1400 Quick Start Operation

Please reference the TSW1400 user's guide for more detailed explanations of the TSW1400 setup and operation. This document assumes the TSW1400 software is installed and functioning properly.

Two-tone test configuration from *High Speed Data Converter Pro* (*HSDCP*) as illustrated in Figure 7:

- In the *Tone BW* section, entering *3M* for the two-tone case means tone-spacing. For single-tone, *Tone BW* can be 1.
- Enter the desired number of tones (#).
- Enter the value for the baseband shifting in the *Tone Center*.
- On *Tone selection* select *I/Q* for a complex pattern, and *Real* for a real pattern.
- Enter *Data Rate (SPS)* for the *DAC sampling frequency*.
- In the *DAC Option* selection, choose between *2's Complement* and *Offset binary*.

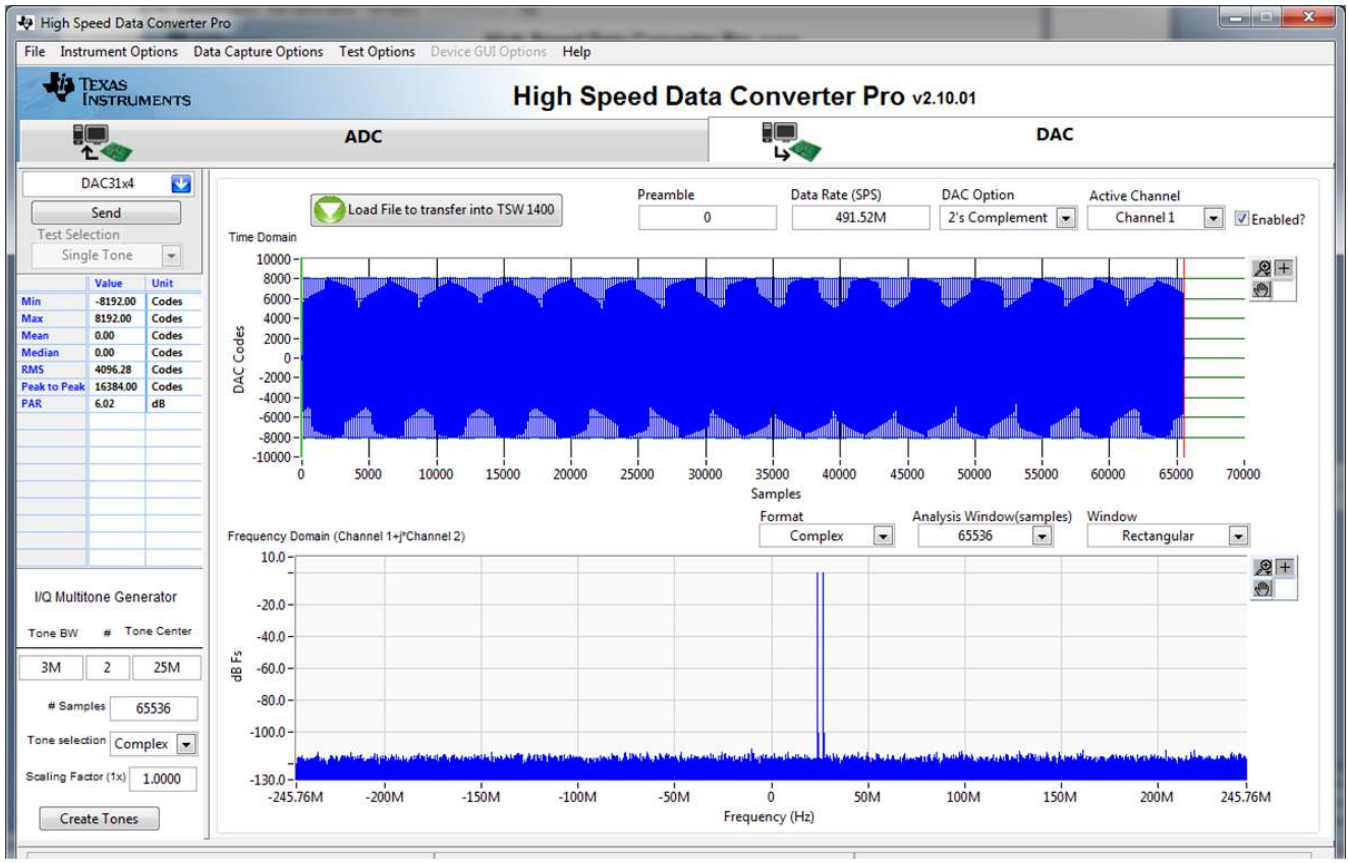

Figure 7. TSW1400 Two-Tone Programming GUI

3.4 DAC31x4 Software Quick-Start Guide

- Provide the clock input 491.52 MHz at 1.5 Vrms at J9 SMA connector of the DAC31x4 EVM
- Provide the LO source of 885 MHz (12-dBm max) at either J13 SMA connector of the DAC31x4 EVM
- Turn on the power to the board and press the reset button on the EVM
- Press the *Reset USB Port* button in the GUI and verify the USB communication
- Switch to the INPUT tab of the GUI
- Click *LOAD REGS*, browse to the installation folder and load example file *dac3174_reg.txt*. This file contains settings for DAC3174 running at 491.52 MSPS. Load this file and wait a couple of seconds for the settings to go into effect.
- Verify the spectrum using the Spectrum Analyzer at the two RF outputs of the DAC EVM (J15).

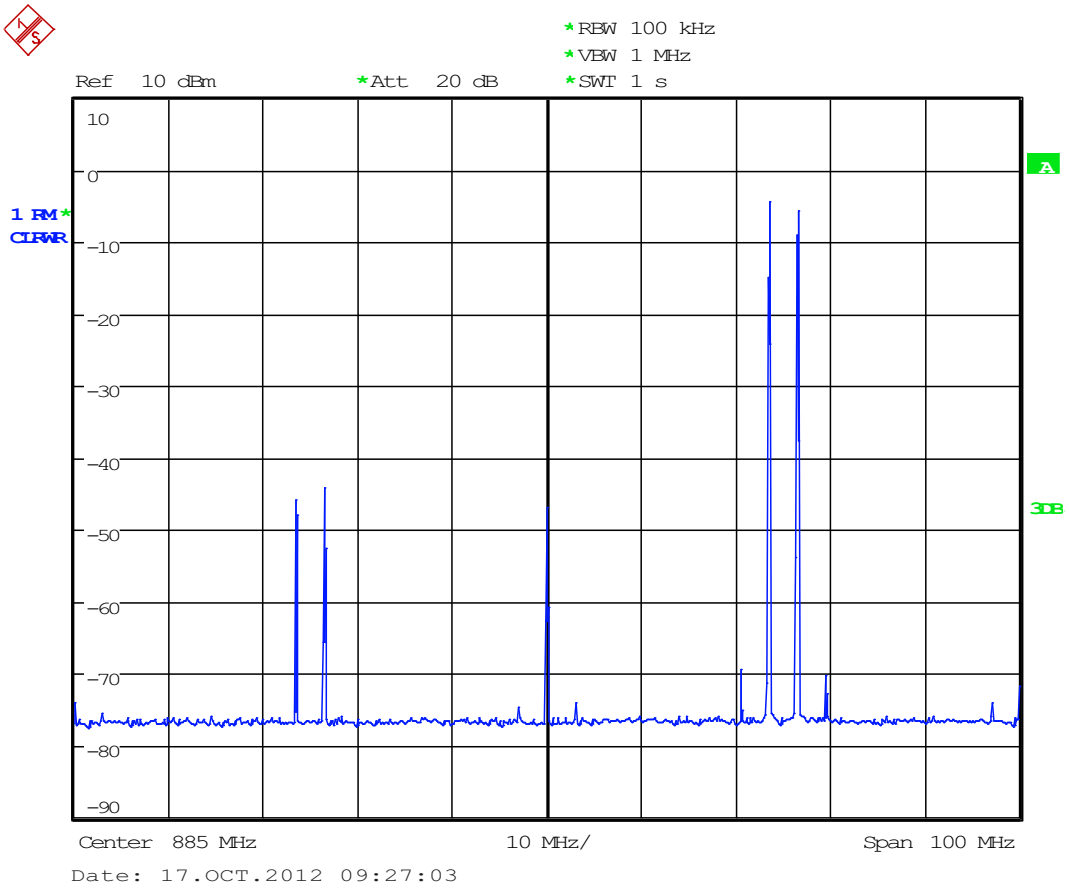

Figure 8. Captured Two-Tone from Spectrum Analyzer

Figure 8 shows a captured two-tone from spectrum analyzer as illustrated configuration of TSW1400 GUI, *High Speed Data Converter Pro*, in Figure 7. This two-tone is centered at 885 MHz as providing 885 MHz of external LO from the signal generator.

3.5 DAC3174 Output Performance for WCDMA and LTE

10 MHz of LTE signal is measured for Adjacent Channel Power Ratio (ACPR) performance, as shown in Figure 9. The specification of this pattern is based on 3GPP LTE FDD E-TM1.1 and Quadrature Phase Shift Keying (QPSK) of the modulation scheme. Measured ACPR shows –72.80 dB and –72.18 dB at adjacent channel and –74.73 dB and –74.83 dB at alternate channel.

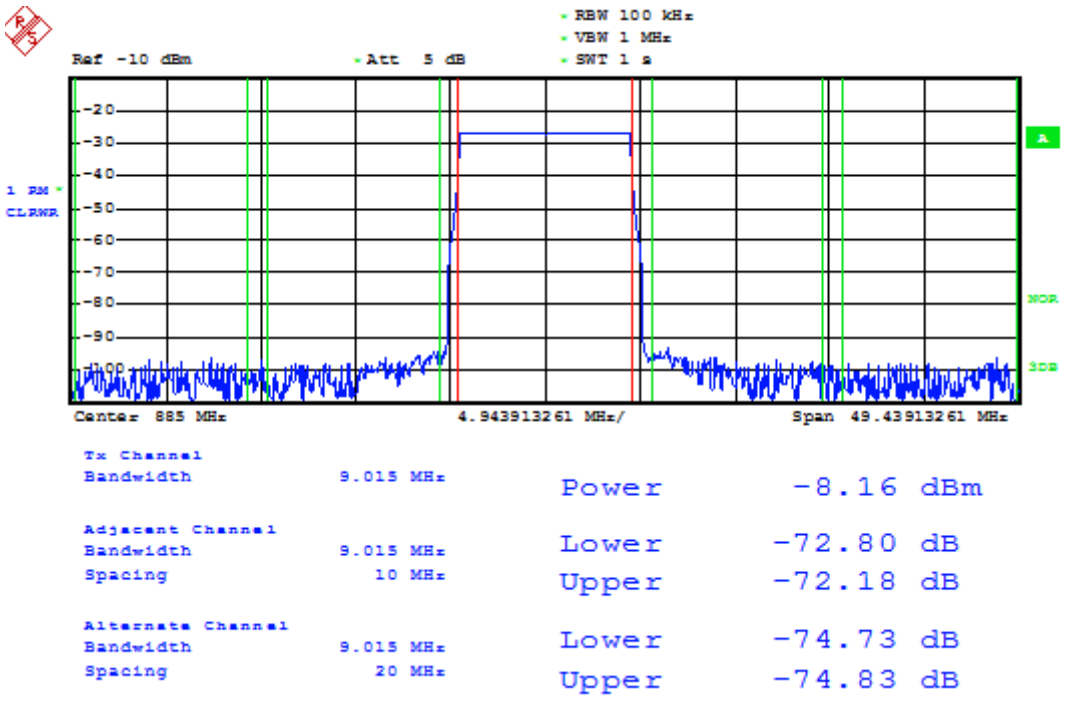

Figure 9. DAC3174 and TRF3705 LTE, 10-MHz Output (Baseband = 0 MHz, LO = 885 MHz)

5 MHz of WCDMA signal is measured for ACPR performance as shown in Figure 10. The specification of this pattern is based on 3GPP FDD and spread-spectrum modulation technique. Measured ACPR shows –71.44 dB and –71.27 dB at adjacent channel and –73.87 dB and –74.37 dB at alternate channel.

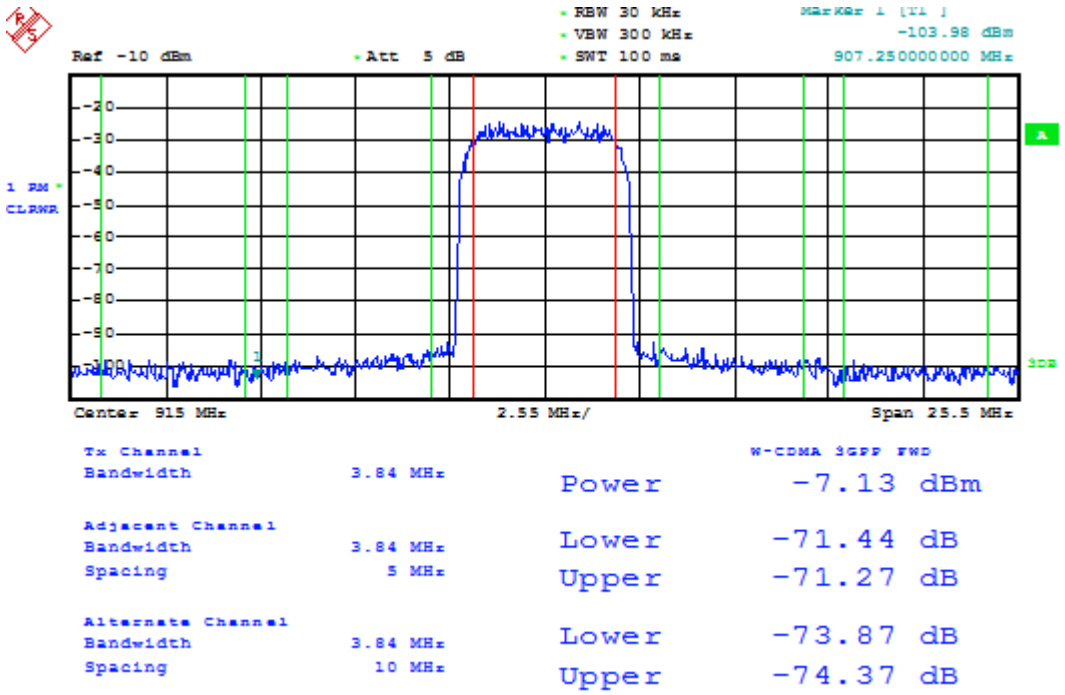

Figure 10. DAC3174 and TRF3705 WCDMA, 5-MHz Output (Baseband = 30 MHz, LO = 885 MHz)

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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