MP2141Q

1.5A, Synchronous Step-Down Converter with VSEL Pin

The Future of Analog IC Technology

DESCRIPTION

The MP2141Q is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs. The MP2141Q achieves 1.5A of continuous output currents from a 2.3V to 5.5V input voltage with excellent load and line regulation.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2141Q is ideal for a wide range of applications including high performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

The MP2141Q requires a minimal number of readily available, standard, external components and is available in an ultra-small SOT563 package.

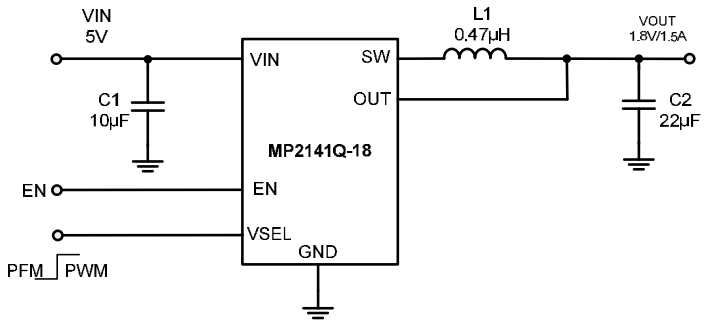
FEATURES

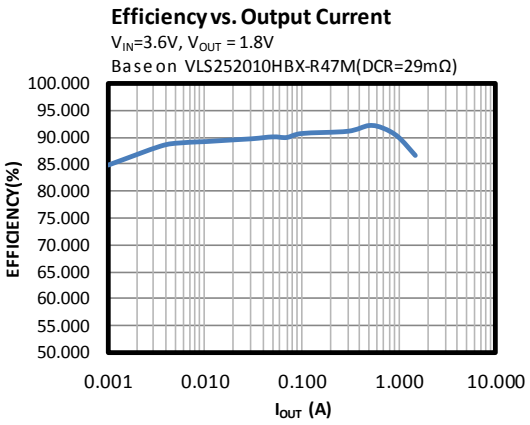
- PFM Quiescent Current: 20μA
- EN for Power Sequencing
- VSEL for PFM/PWM
- Wide 2.3V to 5.5V Operating Input Range
- Fixed Output Voltage: 1.8V
- Up to 1.5A of Output Current
- 120mΩ and 80mΩ Internal Power MOSFET Switches
- Output Discharging
- Short-Circuit Protection (SCP) with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- 100% Duty Cycle
- Available in a SOT563 Package

APPLICATIONS

- DDR/Codec
- Portable Instruments
- Battery-Powered Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range
MP2141QGTF-18	SOT563	*See Below*	Fixed 1.8V

* For Tape & Reel, add suffix –Z (e.g. MP2141QGTF-18–Z);

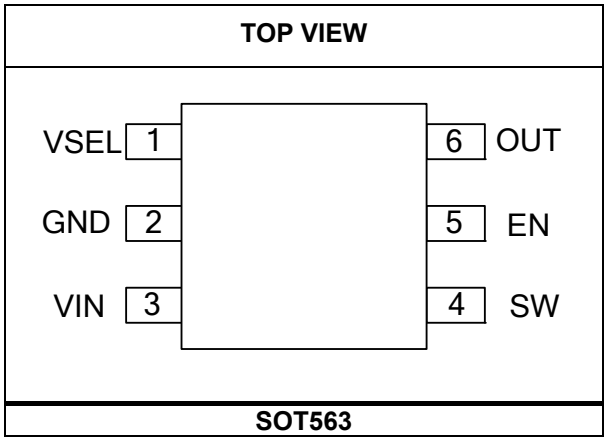
TOP MARKING

AZHY

LLL

AZH: Product code of MP2141QGTF-18
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 6V
V_{SW} ..... -0.3V (-5V for <10ns) to 6V (8V for <10ns)
All other pins ..... -0.3V to 6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2)(4)
SOT563 ..... 1.78W
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 2.3V to 5.5V
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance

SOT563	***θ_{JA}***	***θ_{JC}***	
EV2141Q-TF-00A (4)	70	35	°C/W
JESD51-7 (5)	130	60	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2141Q-TF-00A, 2-layer PCB.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN range			2.3		5.5	V
Under-voltage lockout threshold rising				2	2.25	V
Under-voltage lockout threshold hysteresis				150		mV
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	µA
Supply current (quiescent)		V_{EN} = 2V, no switching, VIN = 5V, PFM, T_J = 25°C		20	30	µA
		V_{EN} = 2V, no switching, VIN = 5V, PWM		620		µA
Fixed output voltage		For MP2141Q-18, 2.3V ≤ VIN ≤ 5.5V, T_J = 25°C	1.782	1.8	1.818	V
		For MP2141Q-18, 2.3V ≤ VIN ≤ 5.5V, T_J = -40°C to +125°C	1.764	1.8	1.836	V
P-FET switch on resistance	R_{DSON_P}	VIN = 5V		120		mΩ
N-FET switch on resistance	R_{DSON_N}	VIN = 5V		80		mΩ
Switch leakage		V_{EN} = 0V, VIN = 6V, V_{SW} = 0V or 6V, T_J = 25°C			1	µA
Switching frequency	f_s	VIN = 3.6V, V_{OUT} = 1.8V, CCM, Io = 0A, T_J = 25°C [7]	1760	2200	2640	kHz
		VIN = 3.6V, V_{OUT} = 1.8V, CCM, Io = 0A, T_J = -40°C to +125°C [7]	1650	2200	2750	kHz
Minimum on time [7]	T_{MIN-ON}	VIN = 3.6V		60		ns
Minimum off time	$T_{MIN-OFF}$	VIN = 3.6V		60		ns
On time	T_{ON}	VIN = 5V, V_{OUT} = 1.8V		160		ns
		VIN = 3.6V, V_{OUT} = 1.8V		230		
P-FET peak current limit		Sourcing	2	2.7		A
N-FET valley current limit		Sourcing, valley current limit		1.5		A
ZCD [6]		PFM		0		mA
Soft-start time	T_{SS-ON}	V_{OUT} rise from 10% to 90%			400	µs
Maximum duty cycle			100			%
VSEL input logic low voltage					0.4	V
VSEL input logic high voltage			1.2			V
VSEL delay PFM to PWM [7]				5		µs
VSEL delay PWM to PFM [7]				10		µs
VSEL pull-down resistor	R_{VSEL}			1		MΩ

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 3.6V, T_J = -40°C to +125°C [6], typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN turn on delay		EN on to SW active		100		µs
EN turn off delay [7]		EN off to stop switching		20		µs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN pull-down resistor	R_{EN}			0.78		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V		250		Ω
EN input current		V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Thermal shutdown [7]				160		°C
Thermal hysteresis [7]				30		°C
System Level						
Recommended input capacitance	C_{IN}	VIN = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1.5A		10		µF
Recommended inductance	L		0.47		2.2	µH
Output capacitance	C_{OUT}	VIN = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1.5A	10		47	µF
Output ripple		VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, CCM		10		mV
Load regulation		VIN = 3.6V, V_{OUT} = 1.8V, CCM, from 0A to 1.5A			1	%
Line regulation		VIN from 2.3 to 5.5V, V_{OUT} = 1.8V, I_{OUT} = 1.5A			0.5	%
Efficiency		VIN = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1A, L_DCR = 29mΩ		90		%

NOTES:

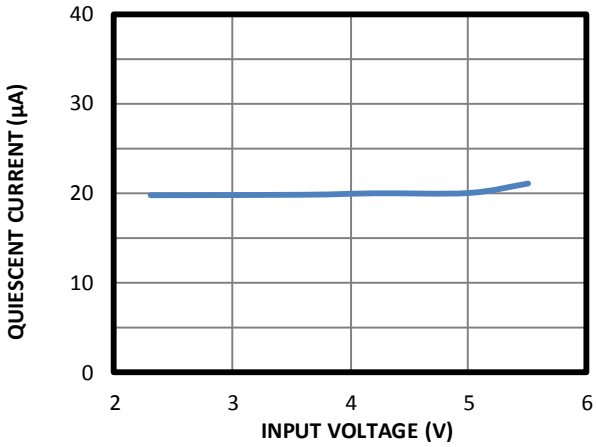
6) No production test, guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

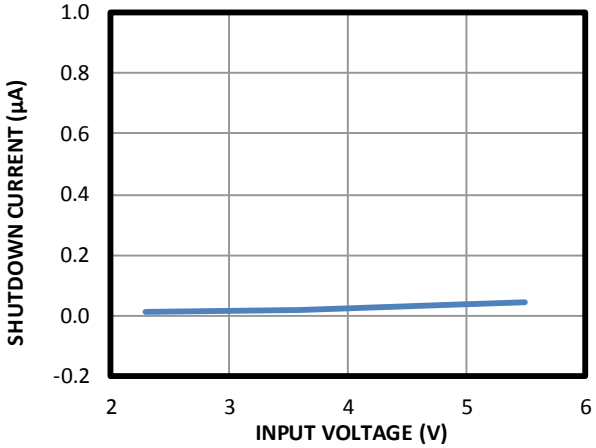
Quiescent Current vs. Input Voltage

PFM



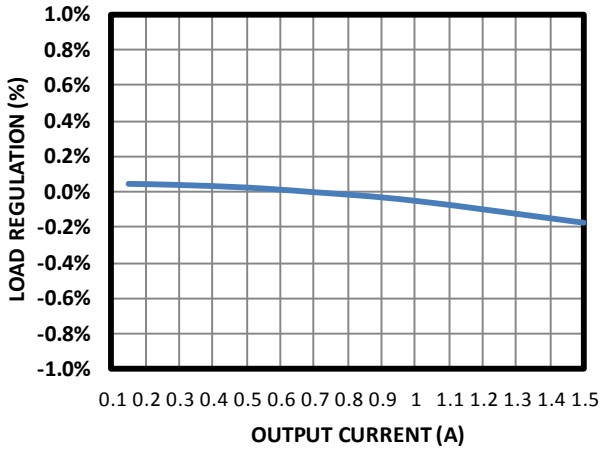
Shutdown Current vs. Input Voltage

V_{EN} = 0V



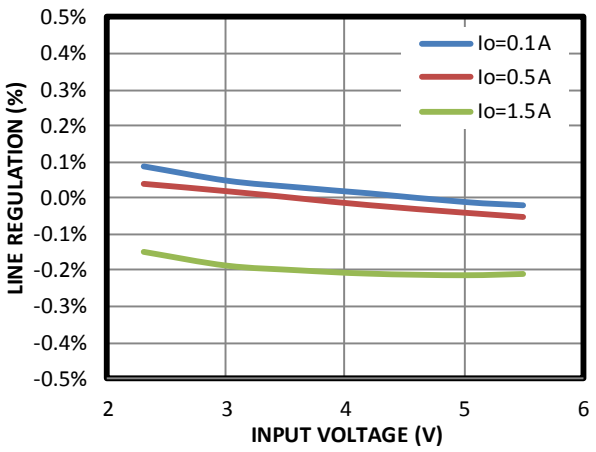
Load Regulation vs. Output Current

VIN = 3.6V, PFM, V_{OUT} = 1.8V



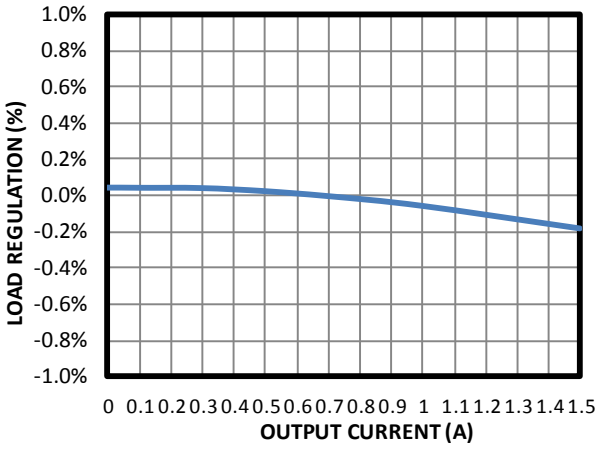
Line Regulation vs. Input Voltage

V_{OUT} = 1.8V, PFM



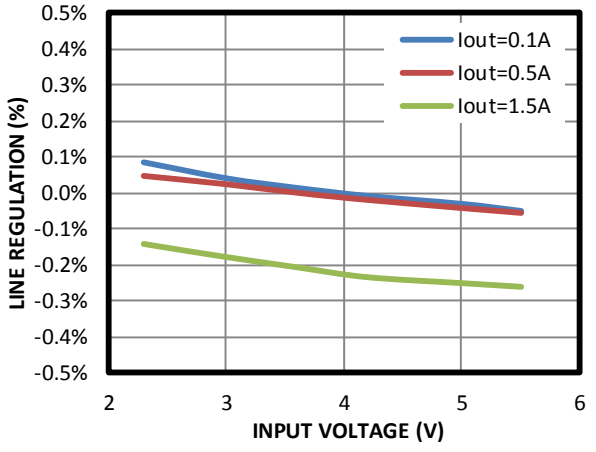
Load Regulation vs. Output Current

VIN = 3.6V, PWM, V_{OUT} = 1.8V



Line Regulation vs. Input Voltage

V_{OUT} = 1.8V, PWM

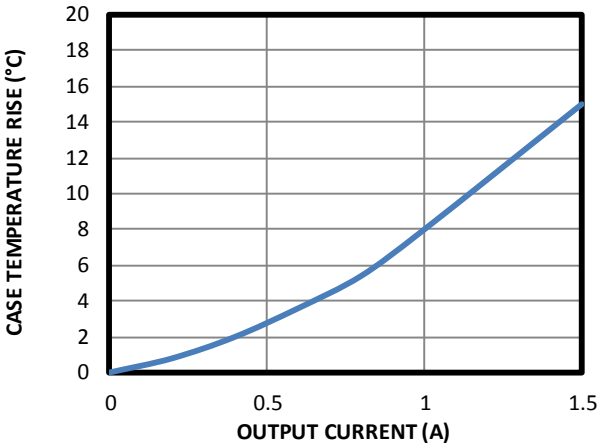


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

Case Temperature Rise vs. Output Current

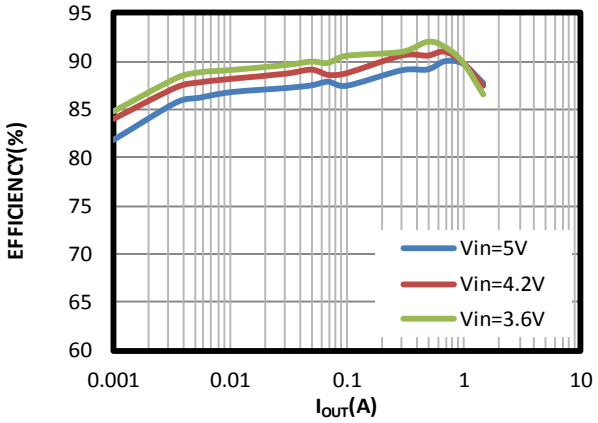
VIN = 3.6V, PFM



Efficiency vs. Output Current

V_{OUT} = 1.8V, PFM

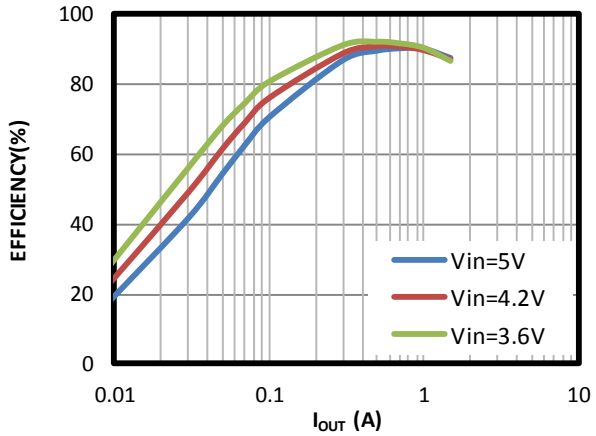
Based on VLS252010HBX-R47M (DCR = 29mΩ)



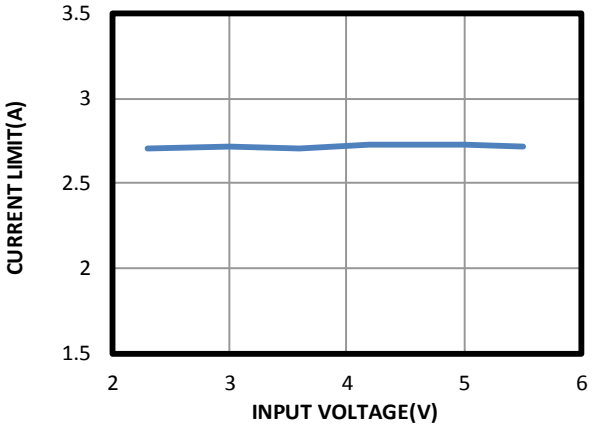
Efficiency vs. Output Current

V_{OUT} = 1.8V, PWM

Based on VLS252010HBX-R47M (DCR = 29mΩ)



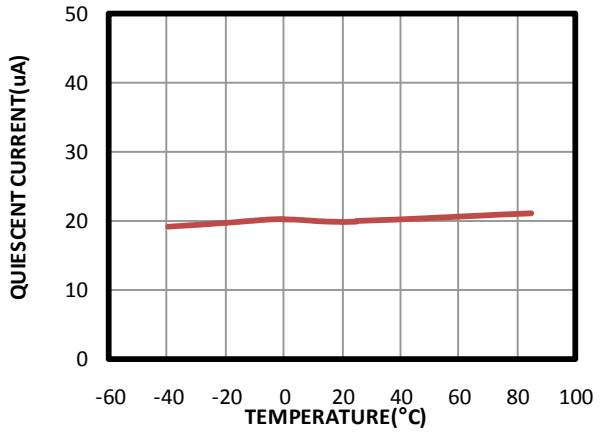
Current Limit vs. Input Voltage



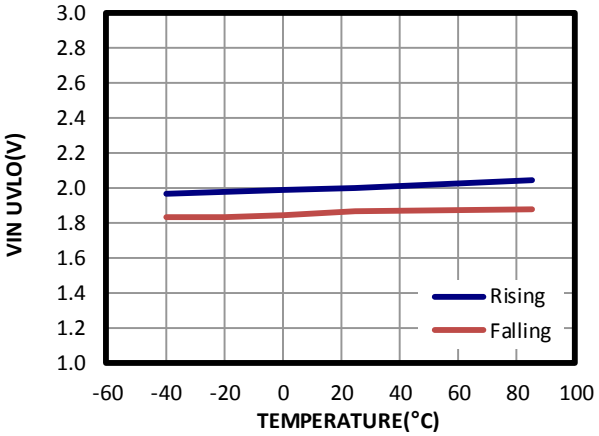
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

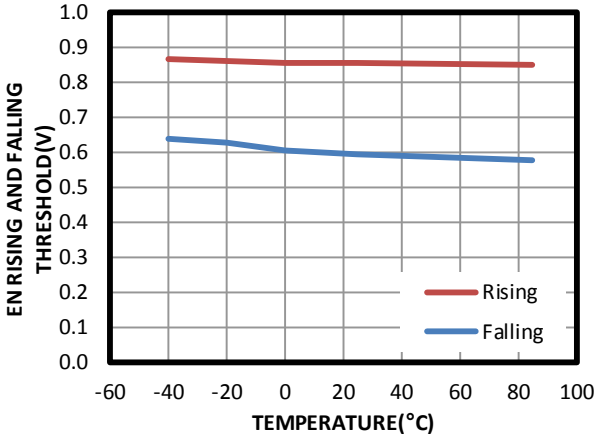
Quiescent Current vs. Temperature



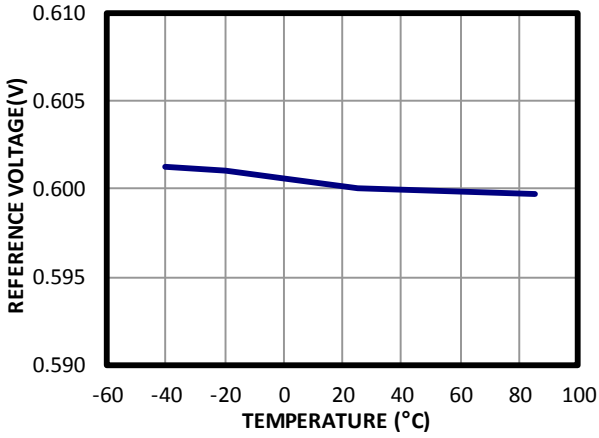
VIN UVLO Rising and Falling Threshold vs. Temperature



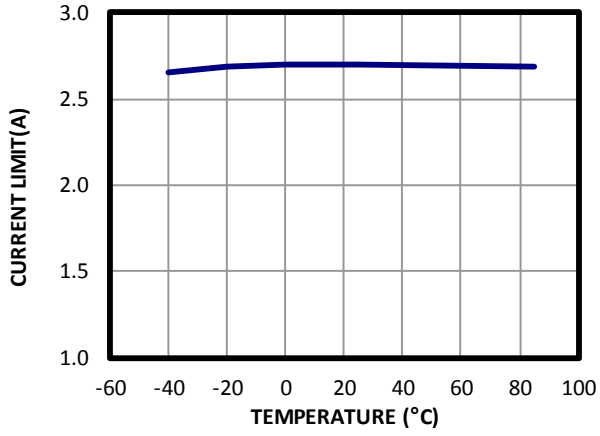
EN Rising and Falling Threshold vs. Temperature



Reference vs. Temperature



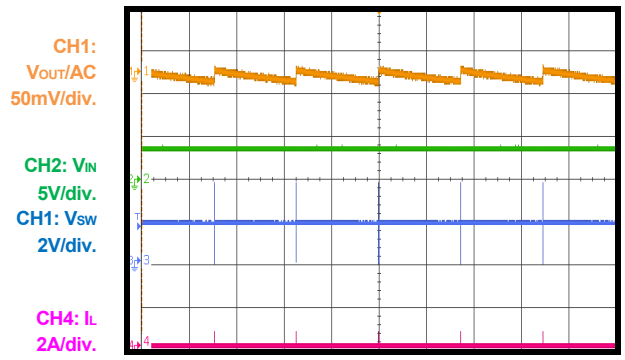
Current Limit vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

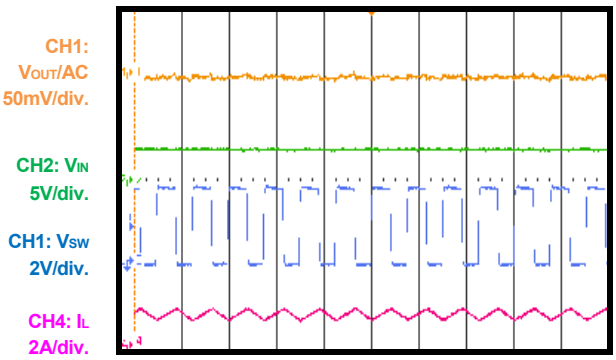
VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

Steady State
without load, PFM



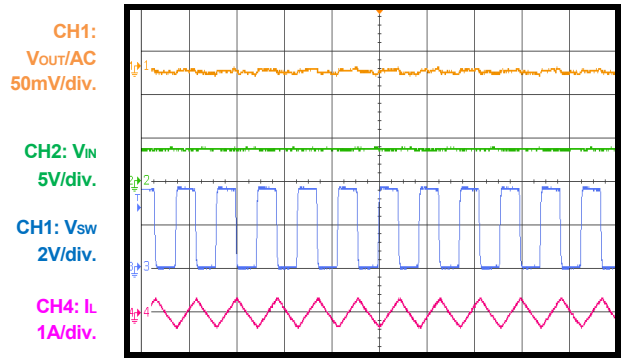
10ms/div.

Steady State
with 1.5A load, PFM



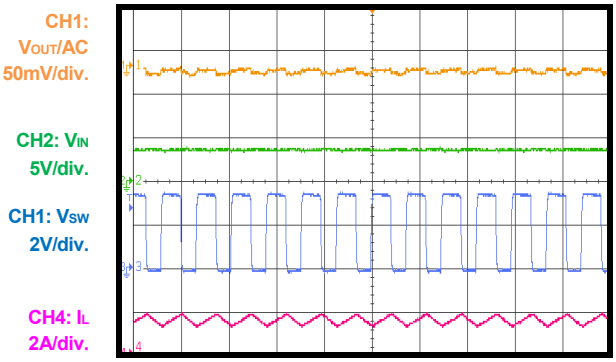
500ns/div.

Steady State
without load, PWM



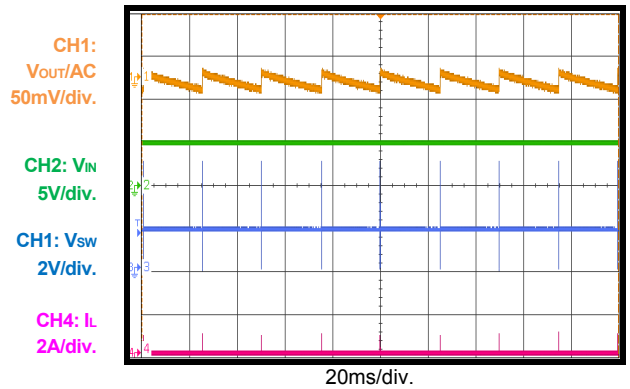
500ns/div.

Steady State
with 1.5A load, PWM



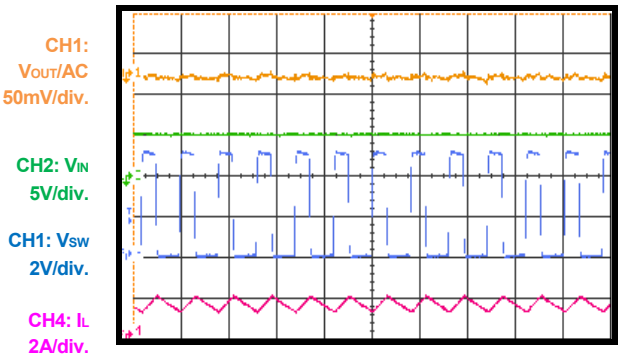
500ns/div.

Steady State
VIN = 5V, V_{OUT} = 1.8V, without load, PFM



20ms/div.

Steady State
VIN = 5V, V_{OUT} = 1.8V, with 1.5A load, PFM

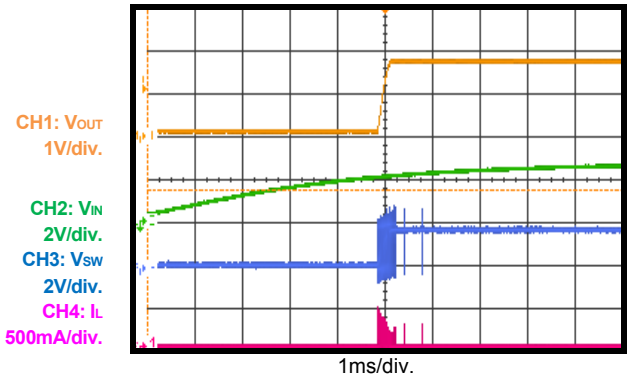


500ns/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

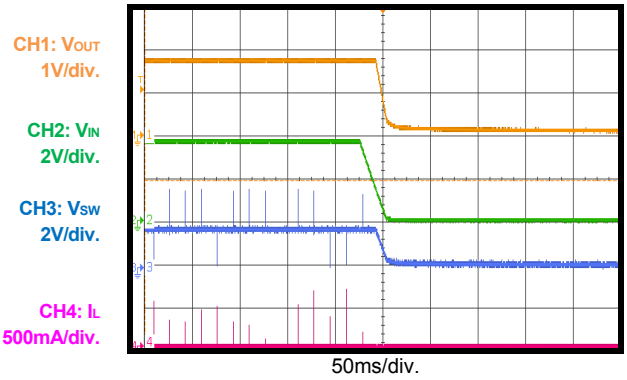
VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

VIN Power-Up
without load, PFM



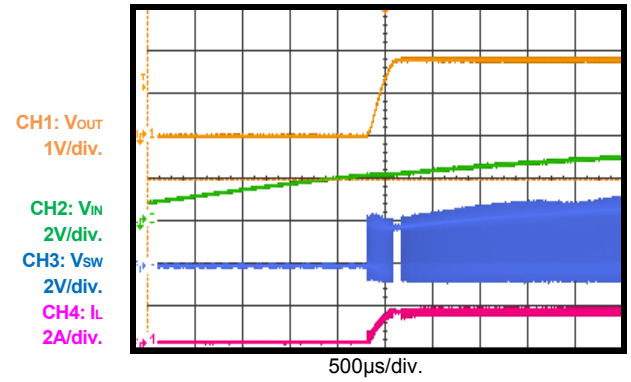
1ms/div.

VIN Shutdown
without load, PFM



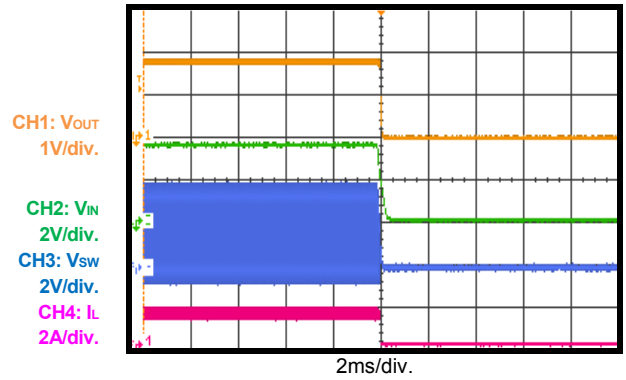
50ms/div.

VIN Power-Up
with 1.5A load, PFM



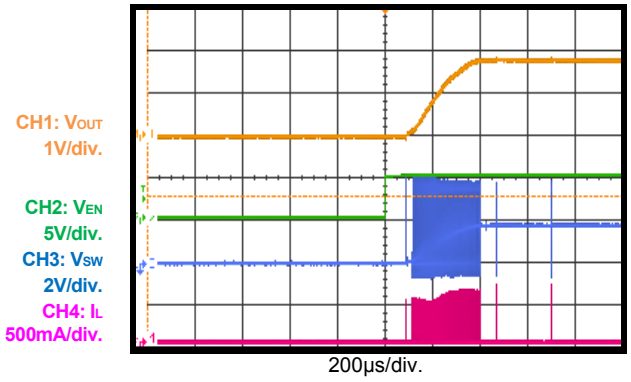
500µs/div.

VIN Shutdown
with 1.5A load, PFM



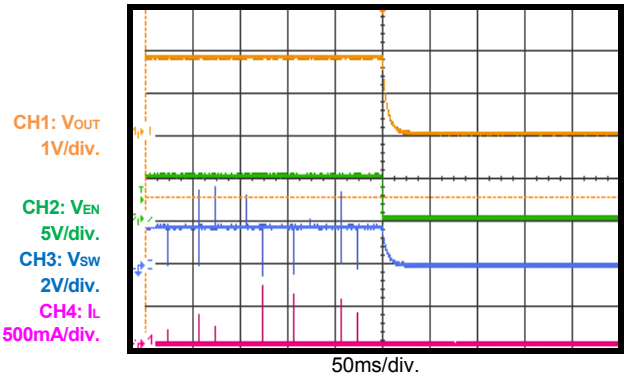
2ms/div.

EN Start-Up
without load, PFM



200µs/div.

EN Shutdown
without load, PFM



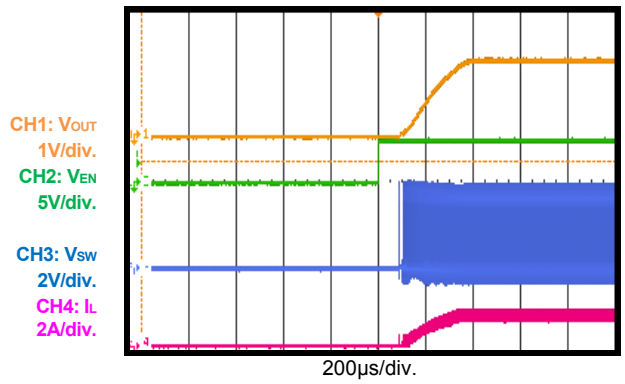
50ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

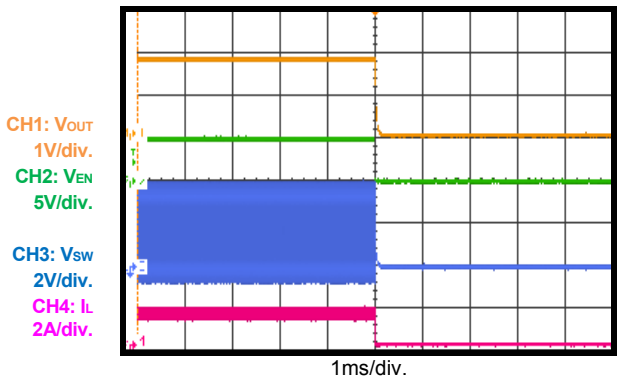
EN Start-Up

with 1.5A load, PFM



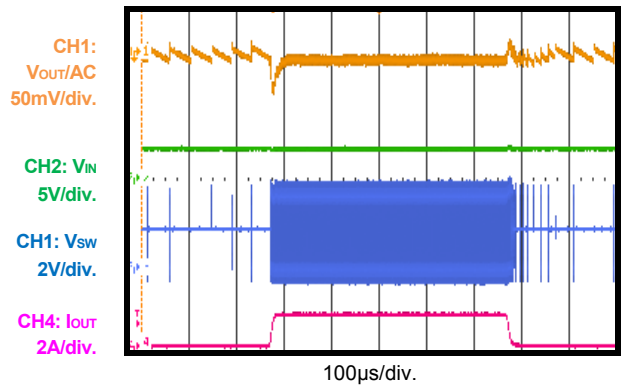
EN Shutdown

with 1.5A load, PFM



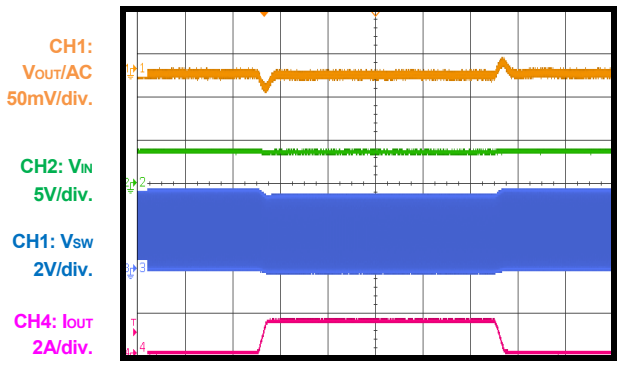
Load Transient Response

I_{OUT} = 0A to 1.5A, PFM



Load Transient Response

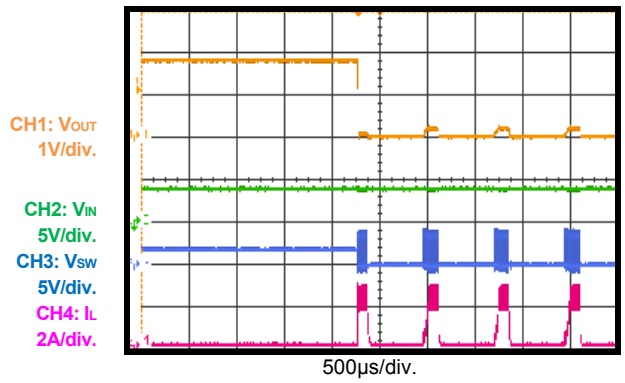
I_{OUT} = 0A to 1.5A, PWM



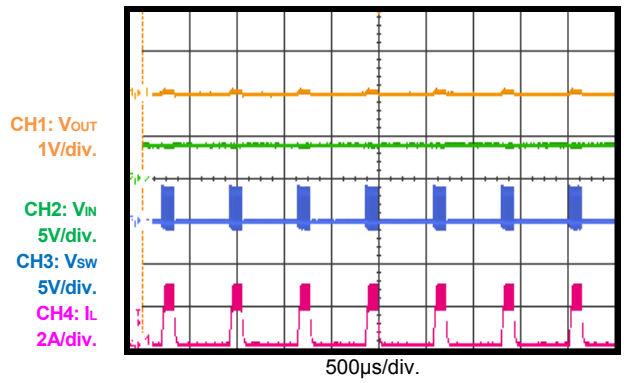
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L = 0.47µH, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.

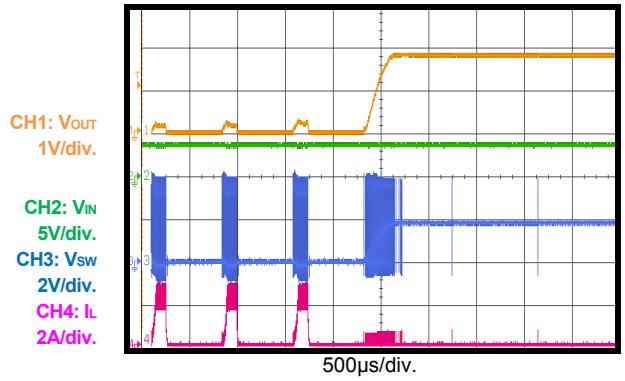
Short-Circuit Entry
PFM



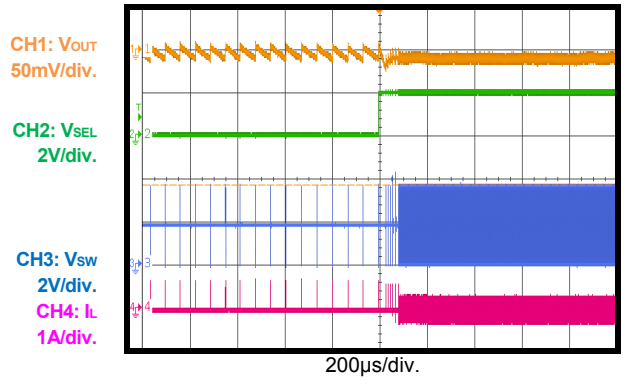
Short Circuit
PFM



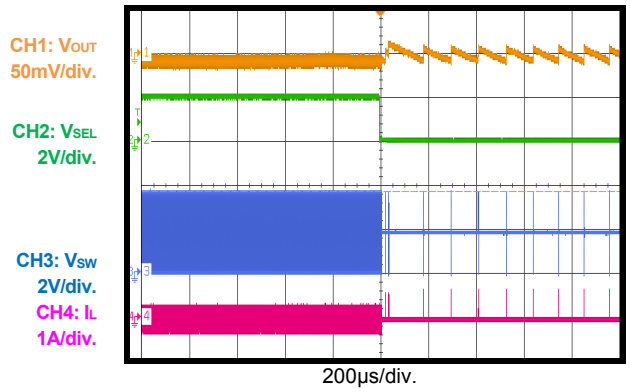
Short-Circuit Recovery
PFM



V_{SEL} Rising
with 10mA load



V_{SEL} Falling
with 10mA load



PIN FUNCTIONS

Pin #	Name	Description
1	VSEL	**PWM and PFM selection.** When VSEL is above 1.2V, the MP2141Q enters PWM mode. When VSEL is below 0.4V or floating, the MP2141Q enters PFM mode.
2	GND	**Power ground.**
3	VIN	**Supply voltage.** The MP2141Q operates on a +2.3V to +5.5V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input.
4	SW	**Output switching node.** SW is the drain of the internal high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.
5	EN	**On/off control.**
6	OUT	**Output voltage power rail and input sense.** Connect the load to OUT. An output capacitor is needed to decrease the output voltage ripple.

BLOCK DIAGRAM

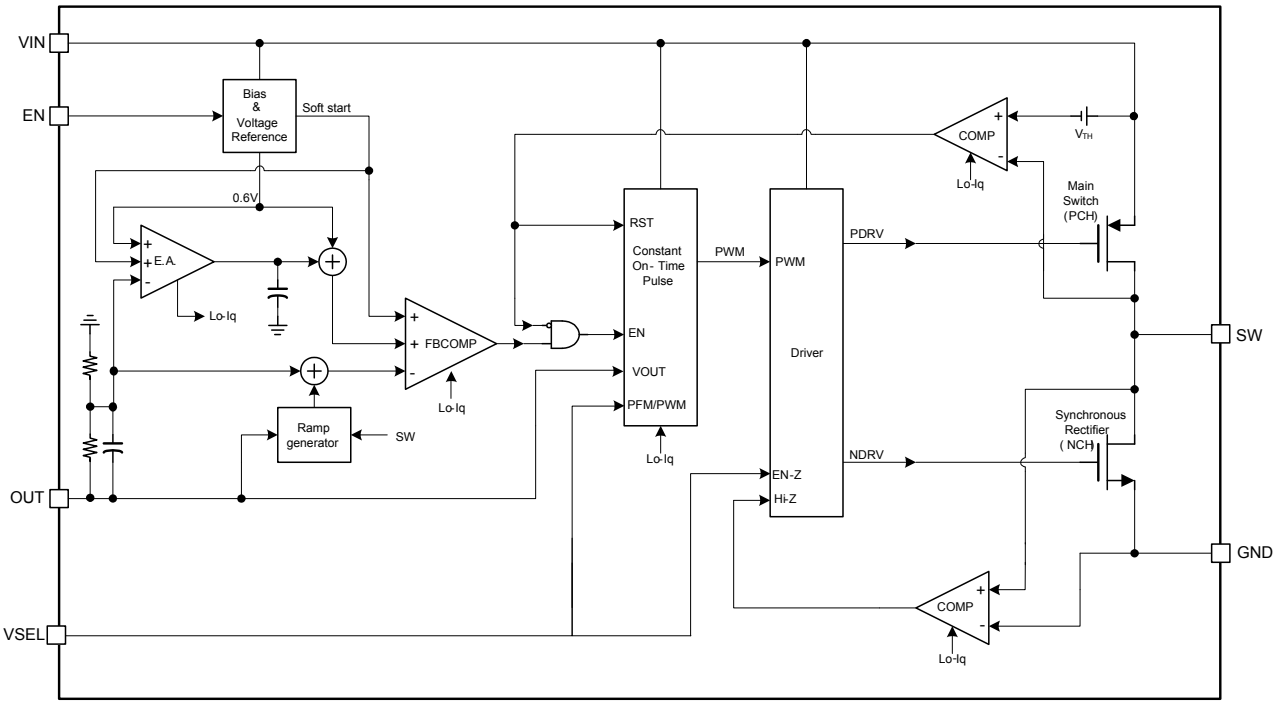


Figure 1: Functional Block Diagram

OPERATION

The MP2141Q uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the entire input range. The MP2141Q achieves 1.5A of continuous output current from a 2.3V to 5.5V input voltage with excellent load and line regulation.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, constant-on-time (COT) control offers a simpler control loop and faster transient response. By using an input-voltage feed-forward, the MP2141Q maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.454\mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the MP2141Q has a fixed minimum off time of 60ns.

Sleep Mode Operation

The MP2141Q uses sleep mode to achieve high efficiency at extremely light load. In sleep mode, most of the circuit blocks are turned off except for the error amplifier and PWM comparator. Therefore, the operation current is reduced to a minimal value (see Figure 2).

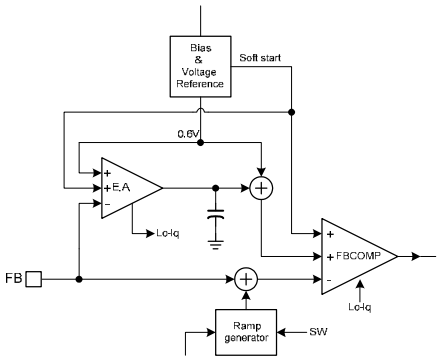


Figure 2: Operation Blocks at Sleep Mode

When the load becomes lighter, the ripple of the output voltage is larger and drives the error amplifier output (EAO) lower. When EAO reaches an internal low threshold, it is clamped at that level, and the MP2141Q enters sleep mode. During sleep mode, the valley of the FB voltage (internal divided voltage) is regulated to the internal reference voltage, making the average output voltage slightly higher than the output voltage at discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse in sleep mode is around 40% larger than that in DCM or CCM. Figure 3 shows the average FB voltage relationship with the internal reference at sleep mode.

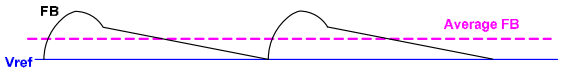


Figure 3: FB Average Voltage at Sleep Mode

When the MP2141Q is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated, and the output voltage ripple decreases relatively. Once the EAO is higher than the internal low threshold, the MP2141Q exits sleep mode and enters either DCM or CCM depending on the load. In DCM or CCM, the error amplifier regulates the average output voltage to the internal reference (see Figure 4).

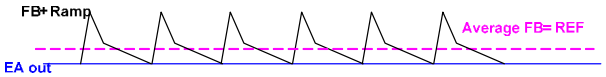


Figure 4: DCM Control

There is always a loading hysteresis when entering and exiting sleep mode due to the error amplifier clamping response time.

AAM Operation at Light-Load Operation

The MP2141Q uses advanced asynchronous mode (AAM) power-save mode together with zero-current cross detection (ZCD) circuit for light load.

The MP2141Q uses AAM power-save mode for light load (see Figure 5). The AAM current (I_{AAM}) is set internally. The SW on-pulse time is decided by the on-time generator and AAM comparator. At light-load condition, the SW on-pulse time is the longer of the two. If the AAM comparator pulse is longer than the on-time generator, the operation mode is as shown in Figure 6.

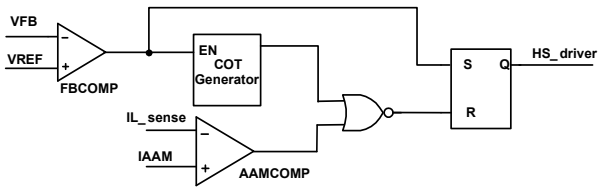


Figure 5: Simplified AAM Control Logic

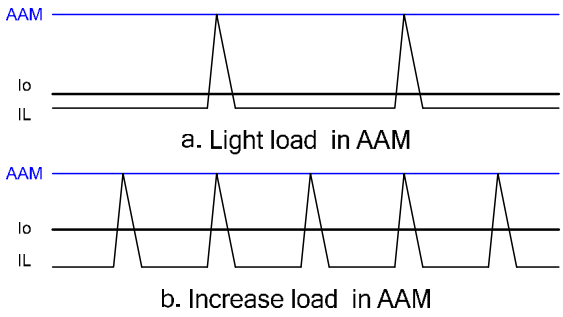


Figure 6: AAM Comparator Control T_{ON}

If the AAM comparator pulse is shorter than the on-time generator, the operation mode is as shown in Figure 7. This usually occurs when using a very small inductance.

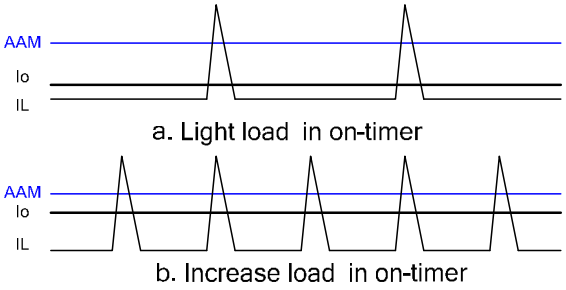


Figure 7: On-Timer Control T_{ON}

In addition to the upper on-time method, the AAM circuit has another 150ns of AAM blank time in sleep mode. This means that if the on-time is less than 150ns, the high-side MOSFET may turn off after the on-time generator pulse without AAM control. The on-time pulse in sleep mode is around 40% larger than that in DCM or CCM. In this condition, I_L may not reach the AAM threshold (se Figure 8).

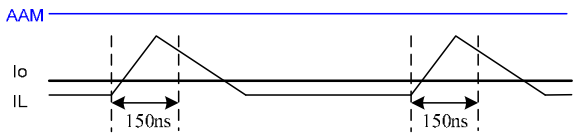


Figure 8: AAM Blank Time in Sleep Mode

Figure 9 shows the AAM threshold decreasing as T_{ON} increases gradually. For CCM, Io must be more than at least half of the AAM threshold.

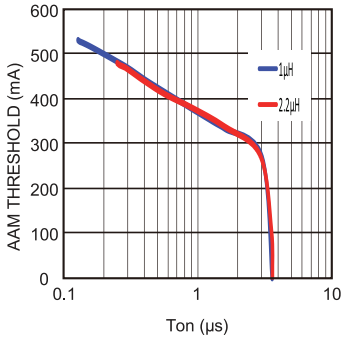


Figure 9: AAM Threshold Decreasing as Ton Increases

The MP2141Q has a ZCD to determine when the inductor current starts to reverse. When the inductor current reaches the ZCD threshold, the low-side switch is turned off.

AAM together with the ZCD circuit makes the MP2141Q always work in DCM at light load, even if V_{OUT} is close to VIN.

Selecting PFM/PWM Mode with VSEL

VSEL can select PWM and PFM dynamically.

When VSEL is below 0.4V or floating, the MP2141Q enters pulse-frequency modulation (PFM) mode. In PFM mode, sleep mode, ZCD, and AAM make the MP2141Q achieve high light-load efficiency.

When VSEL is above 1.2V, the MP2141Q enters PWM mode, disables sleep mode, AAM, and the ZCD threshold. PWM mode can maintain a smaller Vo ripple and fast load transient but has low efficiency at light load.

The delay time from PFM to PWM is about 5µs. When the VSEL logic changes from low to high, the MP2141Q turns on a discharge resistor for about 200µs to activate the PWM pulse more quickly in light load.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2V), the MP2141Q can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP2141Q. There is an internal 0.78MΩ resistor from EN to ground.

When the device is disabled, the part enters output discharge mode automatically, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MP2141Q has a built-in soft start that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The maximum soft-start time is about 0.4ms.

Current Limit

The MP2141Q has a typical 2.7A high-side switch current limit. When the high-side switch reaches its current limit, the MP2141Q remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short-Circuit and Recovery

The MP2141Q also enters short-circuit protection mode when it reaches the current limit and attempts to recover with hiccup mode. The MP2141Q disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the short-circuit condition remains after the soft start ends, the MP2141Q repeats this cycle until the short circuit disappears and the output rises back to the regulation level.

APPLICATION INFORMATION

Selecting the Output Inductor

Most applications work best with a 0.47μH to 2.2μH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with a magnetic device have strong electronic magnetic inference for the system. Any unshielded power inductor should be avoided since it has poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended for applications since they can decrease influence effectively. Table 2 lists some recommended inductors.

Table 2: Suggested Inductor List

Manufacturer P/N	Inductance (μH)	Manufacturer
VLS252010HBX-R47M	0.47	TDK
1239AS-H-1R0M	1.0	Tokyo
74438322010	1.0	Wurth

For most designs, estimate the inductance value from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient. Higher output voltages may require more capacitors to increase system stability.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current.

Estimate the RMS current in the input capacitor with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case scenario occurs at VIN = $2V_{OUT}$, shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic, low ESR capacitors are recommended for limiting the output voltage ripple. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 10 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and away from the feedback network.
5. Keep the V_{OUT} sense line as short as possible and away from the power inductor, especial the surrounding inductors.

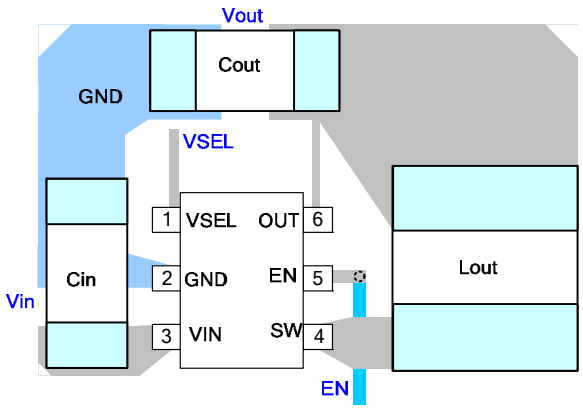


Figure 10: Two Ends of Input Decoupling Capacitor Close to Pin 2 and Pin 3

TYPICAL APPLICATION CIRCUIT

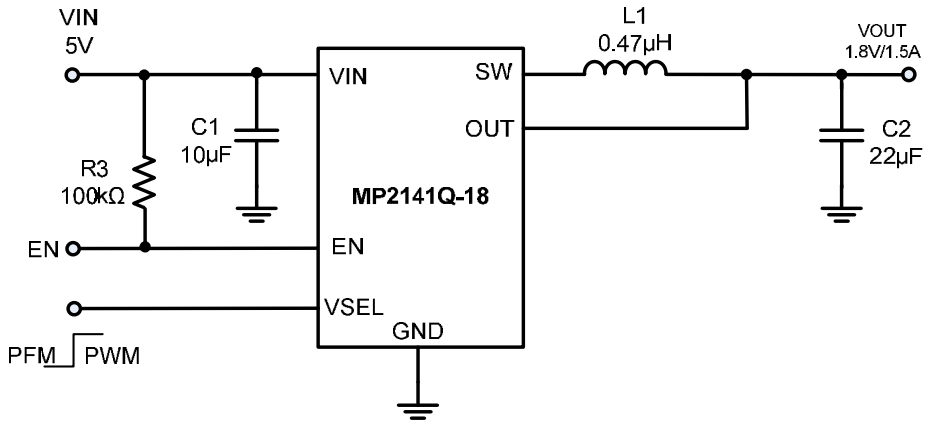
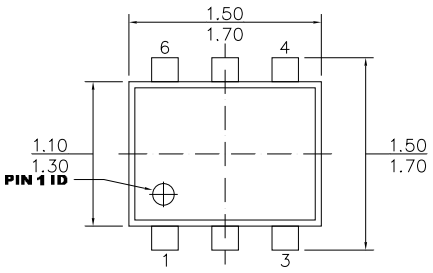


Figure 11: Typical Application Circuit

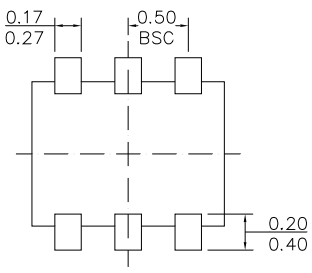
NOTE: VIN < 3.3V may need more input capacitors.

PACKAGE INFORMATION

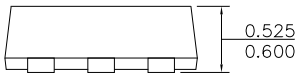
SOT563



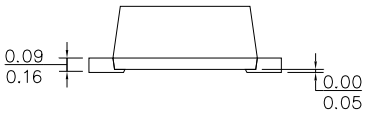
TOP VIEW



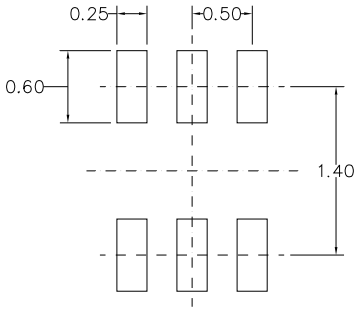
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.