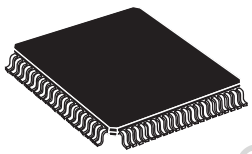
STDVE003A

Adaptive 3.4 Gbps 3:1 TMDS/HDMI signal equalizer

Features

- Compatible with the high-definition multimedia interface (HDMI) v1.3 digital interface
- Conforms to the transition minimized differential signaling (TMDS) voltage standard on input and output channels
- 340 MHz maximum clock speed operation supports all video formats with deep color at maximum refresh rates
- 3.4 Gbps data rate per channel
- Fully automatic adaptive equalizer
- Single supply V_{CC}: 3.135 to 3.465 V
- ESD: > ± 5 KV HBM for all TMDS I/Os
- Integrated open-drain I^2C buffer for display data channel (DDC)
- 5.3 V tolerant DDC and HPD I/Os
- Lock-up free operation of I^2C bus
- 0 to 400 kHz clock frequency for I^2C bus
- Low capacitance of all the channels
- Equalizer regenerates the incoming attenuated TMDS signal
- Buffer drives the TMDS outputs over long PCB track lengths
- Low output skew and jitter
- Tight input thresholds reduce bit error rates
- On-chip selectable 50 Ω input termination
- Low ground bounce
- Data and control inputs provide undershoot clamp diode
- -40°C to 85°C operating temperature range
- Evaluation kit is available



TQFP80

Description

The STDVE003A integrates a 4-channel 3.4 Gbps TMDS equalizer and a 3:1 switch to select one of the three HDMI ports. The 3-input HDMI ports can be either external ports or internal sources. High-speed data paths and flow-through pinout minimize the internal device jitter and simplify the board layout. The equalizer overcomes the intersymbol interference (ISI) jitter effects from lossy cables. The buffer/driver on the output can drive the TMDS output signals over long distances. In addition to this, STDVE003A integrates the 50 Ω termination resistor on all the input channels to improve performance and reduce board space. The device can be placed in a low-power mode by disabling the output current drivers. The STDVE003A is ideal for advanced TV and STB applications supporting HDMI/DVI standard. The differential signal from the HDMI/DVI ports can be routed through the STDVE003A to guarantee good signal quality at the HDMI receiver. Designed for very low skew, jitter and low I/O capacitance, the switch preserves the signal integrity to pass the stringent HDMI compliance requirements.

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
STDEV003ABTR	-40°C to 85°C	TQFP80	Tape and reel

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1 Block diagram

Figure 1. STDVE003A block diagram

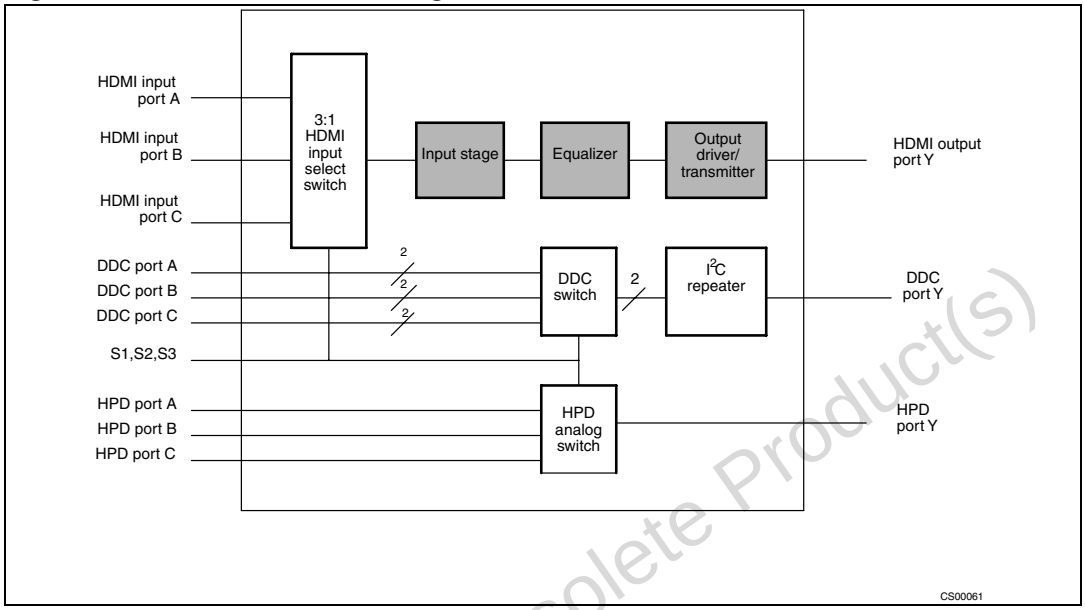


Figure 2. Equalizer functional diagram (one signal pair)

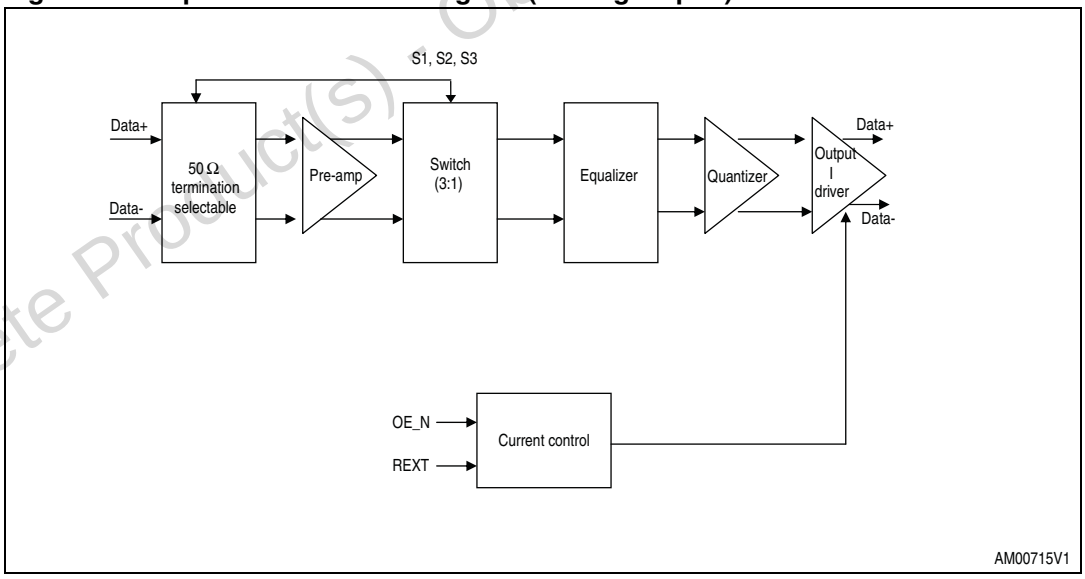
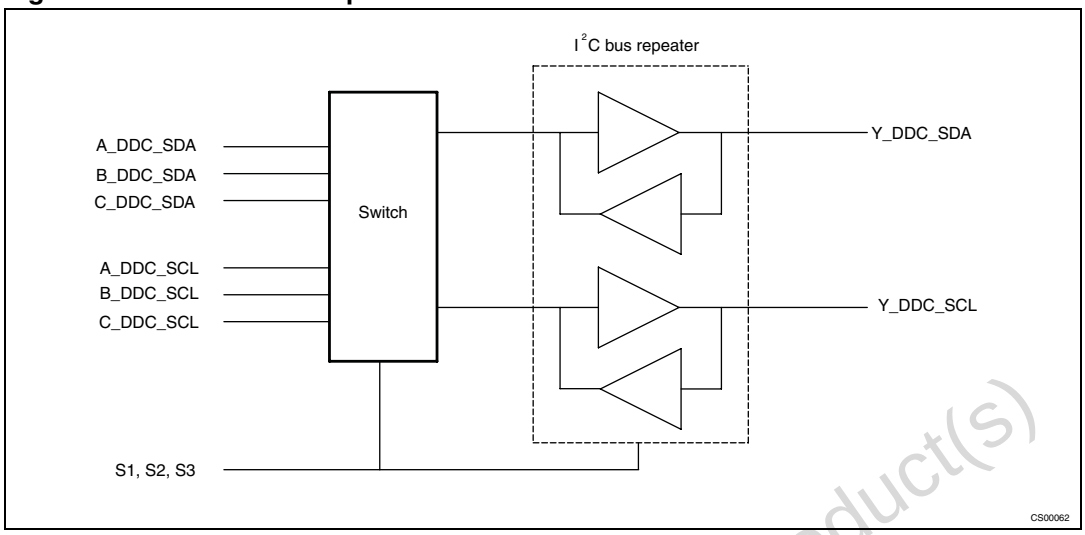
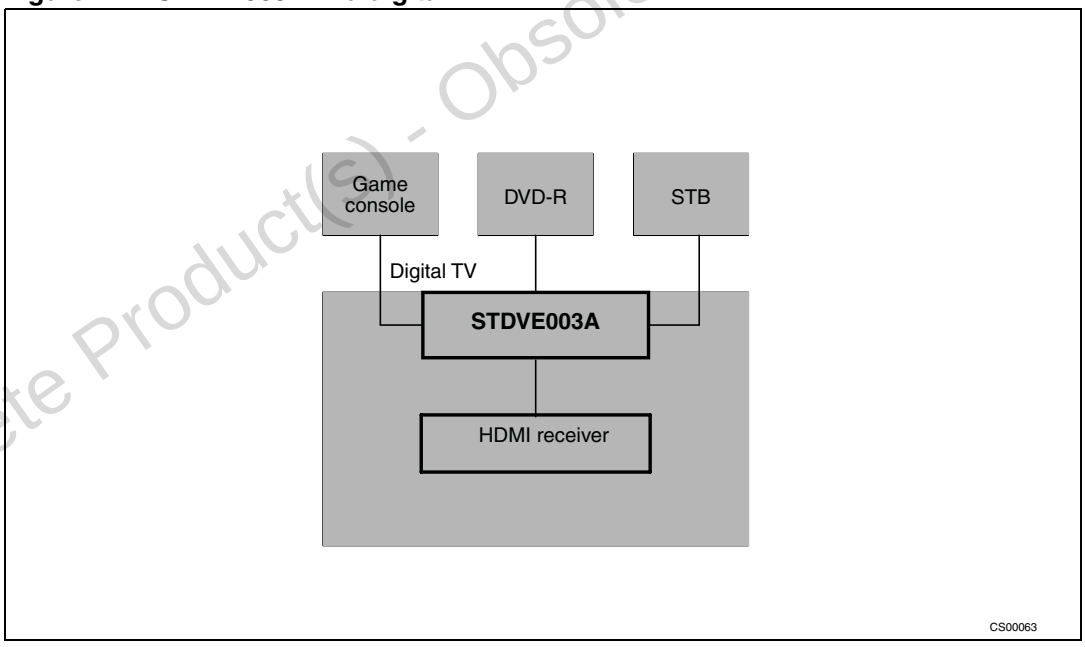


Figure 3. DDC I²C bus repeater



1.1 Application diagrams

Figure 4. STDVE003A in a digital TV



2 Pin configuration

Figure 5. Pin configuration (TQFP80 package)

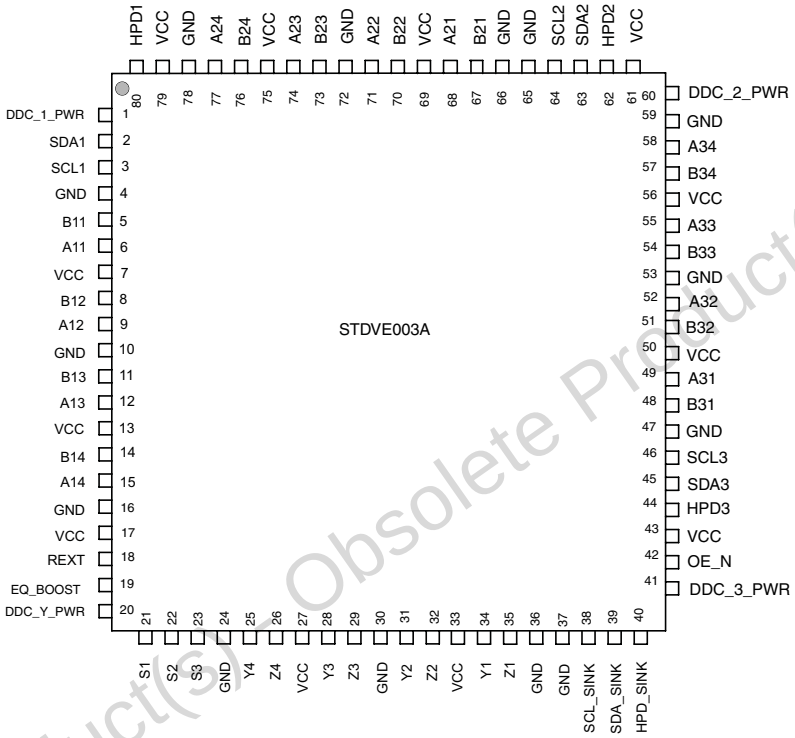


Table 2. Pin description

Pin number	Pin name	Type	Function
1	DDC_1_PWR	Power	External power to connect the pull-up resistor on DDC A ports. Connect to GND if unused.
2, 3	SDA1, SCL1	I/O	Port1 DDC bus data and clock lines
4	GND	Power	Ground
5, 6	B11, A11	Input,TMDS	Port 1 differential inputs for channel 1
7	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
8, 9	B12, A12	Input,TMDS	Port 1 differential inputs for channel 2
10	GND	Power	Ground
11, 12	B13, A13	Input,TMDS	Port 1 differential inputs for channel 3
13	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
14, 15	B14, A14	Input, TMDS	Port 1 differential inputs for channel 4

Table 2. Pin description (continued)

Pin number	Pin name	Type	Function
16	GND	Power	Ground
17	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
18	R_{EXT}	Analog	Connect to GND through a 4.7 KΩ ± 1% precision reference resistor. Sets the output current to generate the output voltage compliant with TMDS
19	EQ_BOOST	Input	Provides equalizer boost function. Set to L for short cables and H for long cables.
20	DDC_Y_PWR	Power	External power to connect the pull-up resistor on DDC Y ports. Connect to GND if unused.
21, 23	S1,S2,S3	Input	Source select inputs
24	GND	Power	Ground
25, 26	Y4, Z4	Output, TMDS	Channel 4 differential outputs
27	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
28, 29	Y3, Z3	Output, TMDS	Channel 3 differential outputs
30	GND	Power	Ground
31, 32	Y2, Z2	Output, TMDS	Channel 2 differential outputs
33	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
34, 35	Y1, Z1	Output, TMDS	Channel 1 differential outputs
36	GND	Power	Ground
37	GND	Power	Ground
38	SCL_SINK	I/O	Sink side DDC bus clock line
39	SDA_SINK	I/O	Sink side DDC bus data line
40	HPD_SINK	Input	Sink side hot plug detector input High: 5 V power signal asserted from source to sink and EDID is ready. Low: No 5 V power signal is asserted from source to sink or EDID is not ready.
41	DDC_3_PWR	Power	External power to connect the pull-up resistor on DDC C ports. Connect to GND if unused.
42	OE_N	Input	Output enable, active low
43	VCC	Power	Supply voltage (3.3 V ± 5%)
44	HPD3	Output	Port 3 hot plug detector output. Open drain output. Connect an external resistor according to the HDMI specification.
45	SDA3	I/O	Port 3 DDC bus data line
46	SCL3	I/O	Port 3 DDC bus clock line

Table 2. Pin description (continued)

Pin number	Pin name	Type	Function
47	GND	Power	Ground
48, 49	B31, A31	Input, TMDS	Port 3 differential inputs for channel 1
50	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
51, 52	B32, A32	Input, TMDS	Port 3 differential inputs for channel 2
53	GND	Power	Ground
54, 55	B33, A33	Input, TMDS	Port 3 differential inputs for channel 3
56	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
57, 58	B34, A34	Input, TMDS	Port 3 differential inputs for channel 4
59	GND	Power	Ground
60	DDC_2_PWR	Power	External power to connect the pull-up resistor on DDC B ports. Connect to GND if unused.
61	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
62	HPD2	Output	Port 2 hot plug detector output. Open drain output. Connect an external resistor according to the HDMI specification.
63	SDA2	I/O	Port 2 DDC bus data line
64	SCL2	I/O	Port 2 DDC bus clock line
65	GND	Power	Ground
66	GND	Power	Ground
67, 68	B21, A21	Input, TMDS	Port 2 differential inputs for channel 1
69	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
70, 71	B22, A22	Input, TMDS	Port 2 differential inputs for channel 2
72	GND	Power	Ground
73, 74	B23, A23	Input, TMDS	Port 2 differential inputs for channel 3
75	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
76, 77	B24, A24	Input, TMDS	Port 2 differential inputs for channel 4
78	GND	Power	Ground
79	V_{CC}	Power	Supply voltage (3.3 V ± 5%)
80	HPD1		Port 1 hot plug detector output. Open drain output. Connect an external resistor according to the HDMI specification.

3 Functional description

The STDVE003A routes physical layer signals for high bandwidth digital video and is compatible with low voltage differential signaling standard like TMDS. The device passes the differential inputs from a video source to a common display when it is in the active mode of operation. The device conforms to the TMDS standard on both inputs and outputs.

The low on-resistance and low I/O capacitance of the switch in STDVE003A result in a very small propagation delay. The device integrates SPDT-type switches for 3 differential data TMDS channels and 1 differential clock channel. Additionally, it integrates the switches for DDC and HPD line switching with I^2C repeater on the DDC lines.

The I^2C interface of the selected input port is linked to the I^2C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD_SINK. For the unused ports, the I^2C interfaces are isolated and the HPD pins are driven to L state.

3.1 Adaptive equalizer

The equalizer dramatically reduces the intersymbol interference (ISI) jitter and attenuation from long or lossy transmission media. The inputs present high impedance when the device is not active or when V_{CC} is absent or 0 V. In all other cases, the 50 Ω termination resistors on input channels are present.

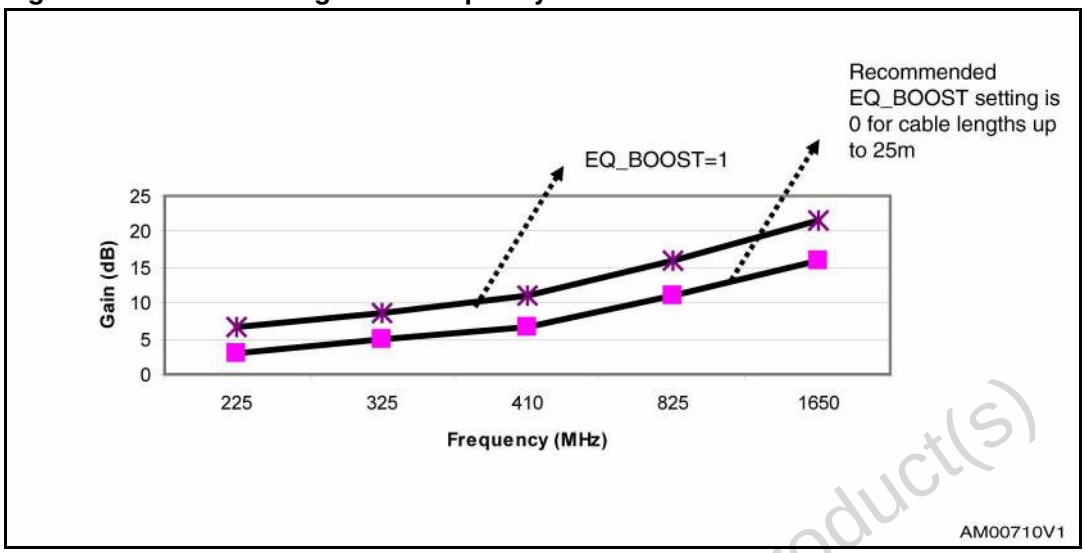
This circuit helps to improve the signal eye pattern significantly. Shaping is performed by the gain stage of the equalizer to compensate the signal degradation and then the signals are driven on to the output ports.

The equalizer is fully adaptive and automatic in function providing smaller gain at low frequencies and higher gain at high frequencies. The default setting of EQ_BOOST = L is recommended for optimized operation.

Table 3. Gain frequency response

Frequency (MHz)	Gain in dB (EQ_BOOST = 0)	Gain in dB (EQ_BOOST = 1)
225	3	6.5
325	5	8.5
410	6.5	11
825	11	16
1650	16	21.5

Figure 6. STDVE003A gain vs. frequency



The STDVE003A equalizer is fully adaptive and automatic in function. The default setting of EQ_BOOST = L is recommended for optimal operation. The equalizer's performance is optimized for all frequencies over the cable lengths from 1 m to 25 m at EQ_BOOST = L. If cable lengths greater than 25 m are desired in application, then EQ_BOOST = H setting is recommended.

Input termination

The STDVE003A integrates precise 50 Ω ± 5% termination resistors, pulled up to V_{CC}, on all its differential input channels. External terminations are not required. This gives better performance and also minimizes the PCB board space. These on-chip termination resistors should match the differential characteristic impedance of the transmission line. Since the output driver consists of current steering devices, an output voltage is not generated without a termination resistor. Output voltage levels are dependent on the value of the total termination resistance. The STDVE003A produces TMDS output levels for point-to-point links that are doubly terminated (100 Ω at each end). With the typical 10 mA output current, the STDVE003A produces an output voltage of 3.3 – 0.5 V = 2.8 V when driving a termination line terminated at each end. The input terminations are selectable thus saving power for the unselected ports.

Output buffers

Each differential output of the STDVE003A drives external 50 Ω load (pull-up resistor) and conforms to the TMDS voltage standard. The output drivers consist of 10 mA differential current-steering devices.

The driver outputs are short-circuit current limited and are high-impedance to ground when OE_N = H or the device is not powered. The current steering architecture requires a resistive load to terminate the signal to complete the transmission loop from V_{CC} to GND through the termination resistor. Because the device switches the direction of the current flow and not voltage levels, the output voltage swing is determined by V_{CC} minus the voltage drop across the termination resistor. The output current drivers are controlled by the OE_N pin and are turned off when OE_N is a high. A stable 10 mA current is derived by accurate internal current mirrors of a stable reference current which is generated by band-gap voltage

across the REXT. The differential output driver provides a typical 10 mA current sink capability, which provides a typical 500 mV voltage drop across a 50 Ω termination resistor.

TMDS voltage levels

The TMDS interface standard is a signaling method intended for point-to-point communication over a tightly controlled impedance medium. The TMDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise. The device is capable of detecting differential signals as low as 100 mV within the entire common mode voltage range.

3.2 Operating modes

Table 4. OE_N operating modes

Input			Output		Function
OE_N	IN+ (ports A1, A2 or A3)	IN- (ports B1, B2 or B3)	OUT+	OUT-	
L	H	L	H	L	Active mode
L	L	H	L	H	Active mode
H	X	X	Hi-Z	Hi-Z	Low power mode

The OE_N input activates a hardware power down mode. When the power down mode is active (OE_N = H), all input and output buffers and internal bias circuitry are powered-off and disabled.

Outputs are tri-stated in power-down mode. When exiting power-down mode, there is a delay associated with turning on band-references and input/output buffer circuits.

3.2.1 SEL operating modes

The active source is selected by configuring source select inputs, S1, S2 and S3. The selected TMDS inputs from each port are switched through a 3-to-1 multiplexer. The I^2C interface of the selected input port is linked to the I^2C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD_SINK. For the unused ports, the I^2C interfaces are isolated, and the HPD pins are kept low.

Table 5. SEL operating modes

Control pins			I/O selected		Hot-plug detect status		
S1	**S2**	**S3**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	X	X	A1/B1	SCL1 SDA1	HPD_SINK	L	L
L	H	X	A2/B2	SCL2 SDA2	L	HPD_SINK	L
L	L	H	A3/B3	SCL3 SDA3	L	L	HPD_SINK
L	L	L	None (Z)	None (Z)	L	L	L

H: logic high; L: logic low; X: don't care; Z: high impedance

3.3 HPD pins

The input pin HPD_SINK is 5 V tolerant, allowing direct connection to 5 V signals. The switch is able to pass both 0 V and 5 V signal levels. The HPD_SINK is an input pin while the A_HPD, B_HPD and C_HPD are open-drain outputs.

3.4 DDC channels

The DDC channels are designed with a bidirectional NMOS gate, providing 5 V signal tolerance. The 5 V tolerance allows direct connection to a standard I^2C bus, thus eliminating the need for a level shifter. There should be external pull-up resistors on either side of the device on both the SCL and SDA lines.

3.5 I^2C DDC line repeater

The device contains two identical bidirectional open-drain, non-inverting buffer circuits that enable I^2C DDC bus lines to be extended without degradation in system performance. The STDVE003A buffers both the serial data (DDC SDA) and serial clock (DDC SCL) on the I2C bus, while retaining all the operating modes and features of the I^2C system. This enables two buses of 400 pF bus capacitance to be connected in an I^2C application. These buffers are operational from a supply V of 3.0 V to 3.6 V.

The I^2C bus capacitance limit of 400 pF restricts the number of devices and bus length. The STDVE003A enables the system designer to isolate the two halves of a bus, accommodating more I^2C devices or longer trace lengths. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required. The STDVE003A can be used to run the I^2C bus at both 5 V and 3.3 V interface levels.

The S1, S2 and S3 (SEL) lines act as control signals for the corresponding A, B or C ports. Note that the SEL line has an internal pull-down resistor. The SEL line should not change state during an I^2C operation, because disabling during bus operation hangs the bus and enabling part way through a bus cycle could confuse the I^2C parts being enabled. The SEL input should change state only when the global bus and the repeater port are in idle state, to prevent system failures.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lock-up condition from occurring when the input low condition is released.

As with the standard I^2C system, pull up resistors are required to provide the logic high levels on the buffered bus. The STDVE003A has standard open collector configuration of the I^2C bus. The size of the pull up resistors depends on the system, but each side of the repeater must have a pull up resistor.

This part is designed to work with standard mode and fast mode I^2C devices. Standard mode I^2C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I^2C system where standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

3.6 Power-down condition

The OE_N is used to disable most of the internal circuitry of STDVE003A that puts the device in a low power mode of operation.

3.7 Bias

The bandgap reference voltage over the external R_{EXT} reference resistor sets the internal bias reference current. This current and its factors (achieved by employing highly accurate and well matched current mirror circuit topologies) are generated on-chip and used by several internal modules. The 10 mA current used by the transmitter block is also generated using this reference current. It is important to ensure that the R_{EXT} value is within the ±1% tolerance range of its typical value.

Table 6. Bias parameter

Parameter	Min	Typ	Max	Unit
Bandgap voltage	-	1.2	-	V

The output voltage swing depends on 3 components: supply voltage ($V_{supply)}$, termination resistor (R_T) and current drive (I_{drive}). The supply voltage can vary from 3.3 V ±5%, termination resistor can vary from 50 Ω ±10%.

The voltage on the output is given by:

$V_{supply} - I_{drive} \times R_T$.

The variation on I_{drive} must be controlled to ensure that the voltage on HDMI output is within the HDMI specification under all conditions.

This is achieved when:

400 mV $\leq I_{drive} \times R_T \leq$ 600 mV with typical value centered at 500 mV.

3.8 Timing between HPD and DDC

It is important to ensure that the I^2C DDC interface is ready by the time the HPD detection is complete.

As soon as the discovery is finished by the HPD detection, the configuration data is exchanged between a source and sink through the I^2C DDC interface. The STDVE003 Afs DDC interface is ready for communication as soon as the power supply to the chip is present and stable. When the desired port is enabled and the chip is out of shutdown mode, the I^2C DDC lines can be used for communication.

Thus, as soon as the HPD detection sequence is complete, the DDC interface can be readily used. There is no delay between the HPD detection and I^2C DDC interface to be ready.

4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to ground	-0.5 to +4.0	V
V_I	DC input voltage (TMDS ports)	1.7 to +4.0	V
	SEL (S1, S2, S3), OE_N	-0.5 to +4.0	V
	A_DDC_SDA, A_DDC_SCL, B_DDC_SDA, B_DDC_SCL, C_DDC_SDA, C_DDC_SCL,Y_DDC_SDA, Y_DDC_SCL, Y_HPD, A_HPD, B_HPD, C_HPD	-0.5 to +6.0	V
I_O	DC output current	120	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

Table 8. Thermal data

Symbol	Parameter	TQFP80	Unit
Θ_{JA}	Thermal coefficient (junction-ambient)	48	°C/W

4.1 Recommended operating conditions

4.2 DC electrical characteristics

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5% [a]

Table 9. Power supply characteristics

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3.135	3.3	3.465	V
I_{CC}	Supply current	All inputs/outputs are enabled. Inputs are terminated with 50 Ω to V_{CC}. V_{CC} = 3.465 V Data rate = 3.4 Gbps		280		mA

Table 10. DC specifications for TMDS differential inputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{TH}	Differential input high threshold (peak-to-peak)	V_{CC} = 3.465 V over the entire V_{CMR}		0	150	mV
V_{TL}	Differential input low threshold	V_{CC} = 3.465 V over the entire V_{CMR}	-150	0		mV
V_{ID}	Differential input voltage (peak-to-peak)(1)	V_{CC} = 3.465 V	150		1560	mV
V_{CMR}	Common mode voltage range		V_{CC} - 0.3		V_{CC} - 0.04	V
C_{IN}	Input capacitance	IN+ or IN- to GND F = 1 MHz		3.5		pF

1. Differential output voltage is defined as | (OUT+ - OUT-) |.
Differential input voltage is defined as | (IN+ - IN-) |.

a. Typical parameters are measured at V_{CC} = 3.3 V, T_A = +25 °C.

Table 11. DC specifications for TMDS differential ouputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{OH}	Single-ended high level output voltage		V_{CC}-10		V_{CC}+10	mV
V_{OL}	Single-ended low level output voltage		V_{CC}-600		V_{CC}-400	mV
V_{swing}	Single ended output swing voltage	V_{CC} = 3.3 V R_{TERM} = 50 Ω	400	500	600	mV
V_{OD}	Differential output voltage (peak-to-peak)(1)	V_{CC} = 3.3 V R_{TERM} = 50 Ω	800	1000	1200	mV
I_{OL}	Differential output low level current		8	10	12	mA
$\|I_{SC}\|$	Output driver short-circuit current (continuous)	OUT± = GND through a 50 Ω resistor. See *Figure 11*			12	mA
C_{OUT}	Output capacitance	OUT+ or OUT- to GND when tri-state F = 1 MHz		5.5		pF

1. Differential output voltage is defined as | (OUT+ - OUT-) |. Differential input voltage is defined as | (IN+ - IN-) |

Table 12. DC specifications for OE_N, EQ_BOOST, SEL (S1, S2, S3) inputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IH}	HIGH level input voltage	High level guaranteed	2.0			V
V_{IL}	LOW level input voltage	Low level guaranteed	-0.5		0.8	V
V_{IK}	Clamp diode voltage	V_{CC} = 3.465 V I_{IN} = -18 mA	-1.2	-0.8		V
I_{IH}	Input high current	V_{CC} = 3.465 V V_{IN} = V_{CC}	-5		+5	µA
I_{IL}	Input low current	V_{CC} = 3.465 V V_{IN} = GND	-5		+5	µA
C_{IN}	Input capacitance	Pin to GND F = 1 MHz		3.5		pF

Table 13. Input termination resistor

Symbol	Parameter	Test condition	Value			Unit
R_{TERM}	Differential input termination resistor on IN± channels relative to V_{CC}	I_{IN} = -10 mA	45	50	55	Ω

Table 14. External reference resistor

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
R_{EXT}	Resistor for TMDS compliant voltage swing range	Tolerance for R = ±1%		4.7		KΩ

Table 15. DDC I/O pins (switch)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{I(DDC)}$	Input voltage		GND		5.3	V

Table 15. DDC I/O pins (switch)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465 V A, B, C ports = 5.3 V Y port = 0.0 V Switch is isolated			6	µA
		V_{CC} = 3.465 V A, B, C ports = 3.3 V Y port = 0.0 V Switch is isolated			2	µA
$C_{I/O}$	Input/output capacitance	V_I=0 V F = 1 MHz Switch disabled		5		pF
		V_I=0 V F = 1 MHz Switch enabled		9		pF

Table 16. Status pins (Y_HPD)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IH}	High level input voltage	V_{CC} = 3.3 V High level guaranteed	2.0		5.3	V
V_{IL}	Low level input voltage	V_{CC} = 3.3 V Low level guaranteed	GND		0.8	V
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465 V Y = 5.3 V			4	µA
		V_{CC} = 3.465 V Y = 3.3 V			2	µA

Table 17. Status pins (A_HPD, B_HPD, C_HPD)(1)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V	Voltage		GND		5.3	V
$C_{I/O}$	Input/output capacitance	V_I = 0 V F = 1 MHz Switch disabled		5		pF
		V_I = 0 V F = 1 MHz Switch enabled		9		pF
V_{OL}	Output low voltage (open drain I/Os)	V_{CC} = 3.3 V I_{OL} = 8 mA			0.4	V

1. Typical parameters are measured at V_{CC} = 3.3 V, T_A = +25 °C.

4.3 DC electrical characteristics (I^2C repeater)

(T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%, GND = 0 V; unless otherwise specified)

Table 18. Supplies

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{CC}	DC supply voltage		3.135	3.3	3.465	V

Table 19. Input/output SDA, SCL

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IH}	High level input voltage		0.7 V_{CC}		5.3	V
V_{IL}	Low level input voltage(1)		-0.5		0.3 V_{CC}	V
V_{ILc}	Low level input voltage contention(1)		-0.5		0.4	V
V_{IK}	Input clamp voltage	I_I = -18 mA	–	–	-1.2	V
I_{IL}	Input current low (SDA, SCL)	Input current low (SDA, SCL)	–	–	1	µA
I_{IH}	Input current high (SDA, SCL)	V_I = 3.465 V (SDA, SCL)	–	–	10	µA
		V_I = 5.3 V (SDA, SCL)	–	–	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA			0.4	V
		I_{OL} = 6 mA			0.65	V
I_{OH}	Output high level leakage current	V_O = 3.6 V; driver disabled	–	–	10	µA
		V_O = 5.3 V; driver disabled	–	–	10	µA
C_I	Input capacitance	V_I = 3 V or 0 V	–	6	7(2)	pF

1. V_{IL} specification is for the first low level seen by the SDA/SCL lines. V_{ILc} is for the second and subsequent low levels seen by the SDA/SCL lines.
2. The SCL/SDA C_I is about 200 pF when V_{CC} = 0 V. The STDVE003A should be used in applications where power is secured to the repeater but an active bus remains on either set of the SDA/SCL pins.

4.4 Dynamic switching characteristics[b]

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%, R_{TERM} = 50 Ω ± 5%, C_L = 5 pF).

Typical values are at T_A = +25 °C and V_{CC} = 3.3 V.

Table 20. Clock and data rate

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
f_{CK}	Clock frequency (1/10th of the differential data rate)		25		340	MHz
D_{rate}	Signaling rate				3.4	Gbps

Table 21. Equalizer gain

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
G_EQ	Equalizer gain	At all frequencies (EQ_BOOST = L) for short cables		15		dB
		At all frequencies (EQ_BOOST = H) for long cables		20		dB

Table 22. Differential output timings

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_r	Differential data and clock output rise/fall times	20% to 80% of V_{OD}	75	150	240	ps
t_f		80% to 20% of V_{OD}	75	150	240	ps
t_{PLH}	Differential low to high propagation delay	Alternating 1 and 0 pattern at slow and fast data rates	250		800	ps
t_{PHL}	Differential high to low propagation delay	Measure at 50% V_{OD} between input to output	250		800	ps

b. The timing values in this section are tested during characterization and are guaranteed by design and simulation. Not tested in production.

Table 23. Skew times

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{SK(O)}$	Inter-pair channel-to-channel output skew				100	ps
$t_{SK(P)}$	Pulse skew	$\lvert t_{PLH} - t_{PHL} \rvert$		25	80	ps
$t_{SK(D)}$	Intra-pair differential skew				44	ps
$t_{SK(CC)}$	Output channel to channel skew	Difference in propagation delay (t_{PLH} or t_{PHL}) among all output channels		50	125	ps

Table 24. Turn-on and turn-off times

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{ON}	TMDS output enable time	Time from OE_N to OUT± change from tri-state to active		12	20	ns
t_{OFF}	TMDS output disable time	Time from OE_N to OUT± change from active to tri-state		6	10	ns

Table 25. DDC I/O pins

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
Refer to *Section 4.5*						

Table 26. Status pins (Y_HPD, A_HPD, B_HPD, C_HPD, SEL)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{PD(HPD)}$	Propagation delay (from Y_HPD to the active port of HPD)	C_L = 10 pF, R_{PU} = 1 KΩ		150		ns
$T_{ON/OFF}$	Switch time (from port select to the latest valid status of HPD)	C_L = 10 pF		50		ns

Table 27. Jitter

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{JIT}	Total jitter(1)	PRBS pattern at 1.6 Gbps (800 MHz)		35		ps (p-p)

1. Total jitter is measured peak-to-peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. Input differential voltage = V_{ID} = 500 mV, PRBS random pattern at 1.65 Gbps, t_r=t_f=50 ps (20% to 80%). Jitter parameter is not production-tested but guaranteed through characterization on a sample-to-sample basis.

4.5 Dynamic switching characteristics (I^2C repeater)

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%.

Typical values are at T_A = +25 °C and V_{CC} = 3.3 V.

Table 28. I^2C repeater(1)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
f_{SCL}	I^2C clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	Low duration on SCL pin	100 KHz See *Figure 19* Voltage on line = 5V Cmax=400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions.	4.7			µs
		400 KHz See *Figure 19* Voltage on line = 5V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions.	1.3			µs
t_{LOW}	Low duration on SCL pin	100 KHz See *Figure 19* Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions.	4.7			µs
		400 KHz See *Figure 19* Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions.	1.3			µs

Table 28. I^2C repeater(1) (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{HIGH}	High duration on SCL pin	100 KHz See *Figure 19* Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions	4.0			µs
		400 KHz See *Figure 19* Voltage on line = 5 V Cmax = 400 pF, Rmax=2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions	0.6			µs
t_{HIGH}	High duration on SCL pin	100 KHz Refer section 14.12, Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions	4.0			µs
		400 KHz See *Figure 19* Voltage on line = 3.3 V, Cmax=400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20% time intervals on both transitions	0.6			µs

Table 28. I^2C repeater(1) (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{PHL}	Propagation delay	400 KHz Waveform 1 (*Figure 17*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			250	µs
		400 KHz Waveform 1 (*Figure 17*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			300	µs
		400 KHz Waveform 1 (*Figure 17*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			250	ns
		400 KHz Waveform 1 (*Figure 17*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			450	ns
		100 KHz Waveform 1 (*Figure 17*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			250	ns
		100 KHz Waveform 1 (*Figure 17*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			300	ns
		100 KHz Waveform 1 (*Figure 17*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			250	ns
		100 KHz Waveform 1 (*Figure 17*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			450	ns
t_f	Output fall time	400 KHz Waveform 1 (*Figure 17*)(2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		400 KHz Waveform 1(2) Voltage on line = 3.3 V Cmax = 400pF, Rmax = 2 K			300	ns

Table 28. I^2C repeater(1) (continued)

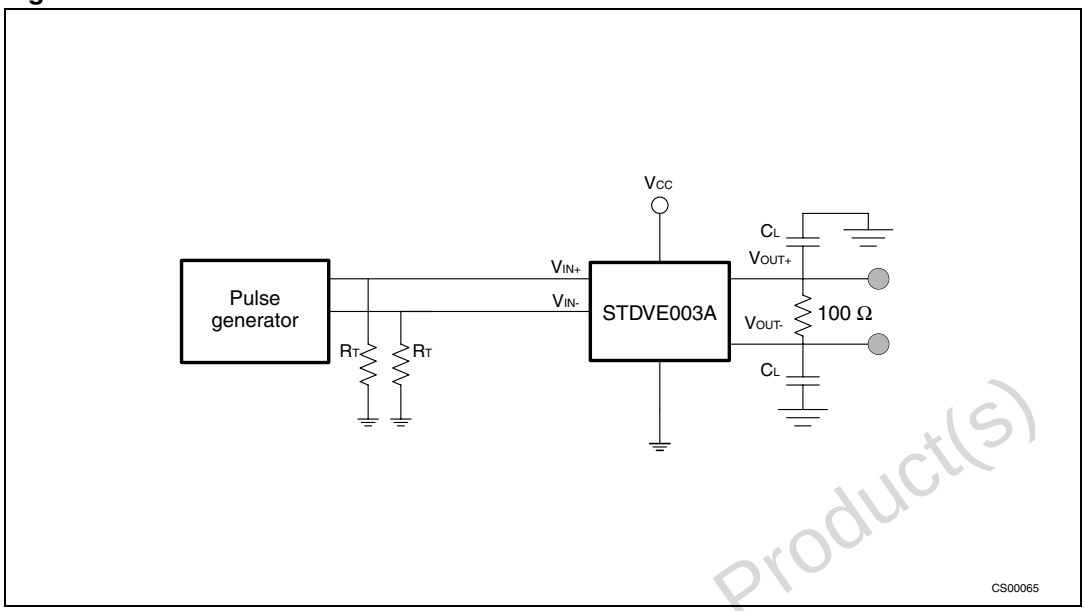
Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_f	Output fall time	100 KHz Waveform 1 (*Figure 17*) (2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		100 KHz Waveform 1 (*Figure 17*)(2) Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			300	ns
t_r	Output rise time	400 KHz Waveform 1 (*Figure 17*)(2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		400 KHz Waveform 1 (*Figure 17*)(2) Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			300	ns
t_r	Output rise time	100 KHz Waveform 1(2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			1000	ns
		100 KHz Waveform 1 (*Figure 17*)(2) Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			1000	ns

1. All the timing values are tested during characterization and are guaranteed by design and simulation. Not tested in production.
2. The t_r transition time is specified with maximum load of 2 kΩ pull-up resistance and 400 pF load capacitance. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times. Refer to *Figure 9*.

Table 29. ESD performance

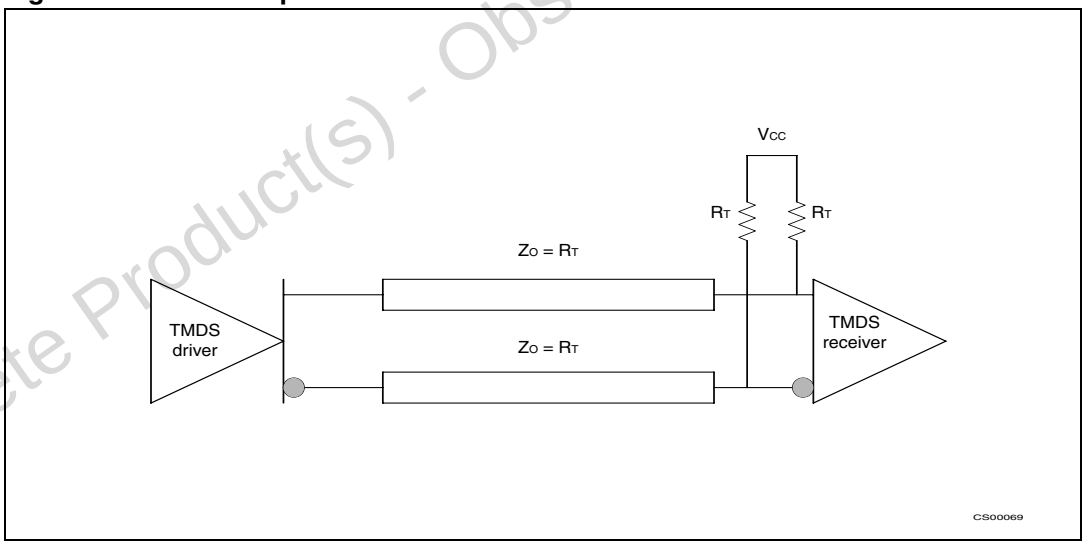
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD	TMDS I/Os	Human body model		±5		kV
	Other I/Os	Human body model		±2		kV

Figure 7. Test circuit for electrical characteristics



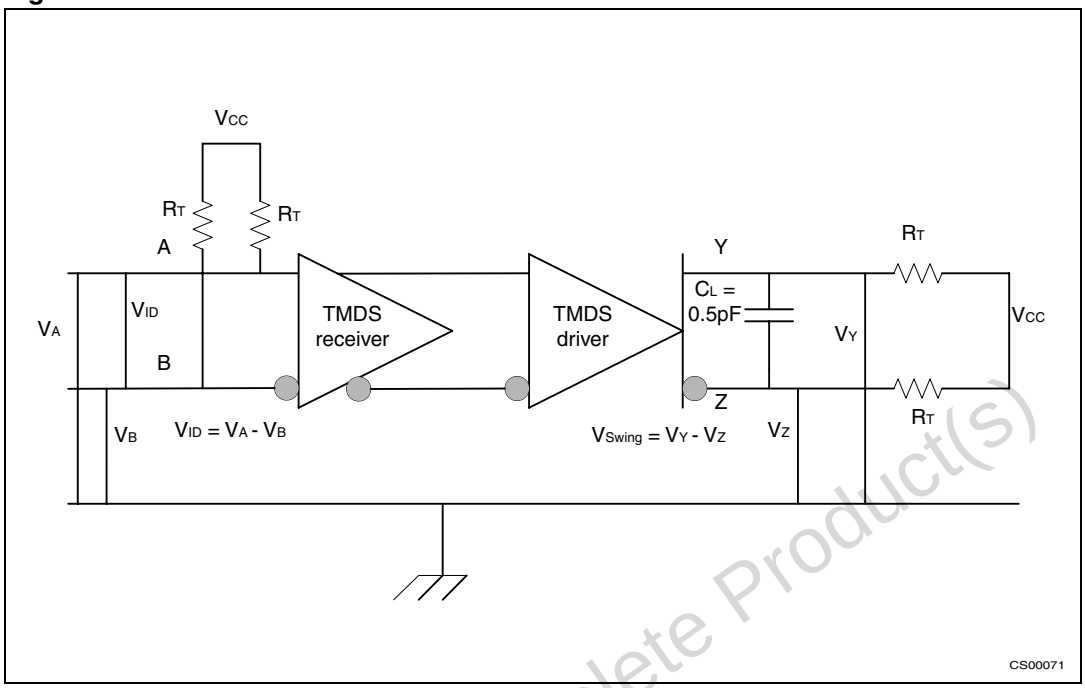
1. C_L = load capacitance: include jig and probe capacitance.
2. R_T = termination resistance; should be equal to Z_{OUT} of the pulse generator.

Figure 8. TMDS output driver



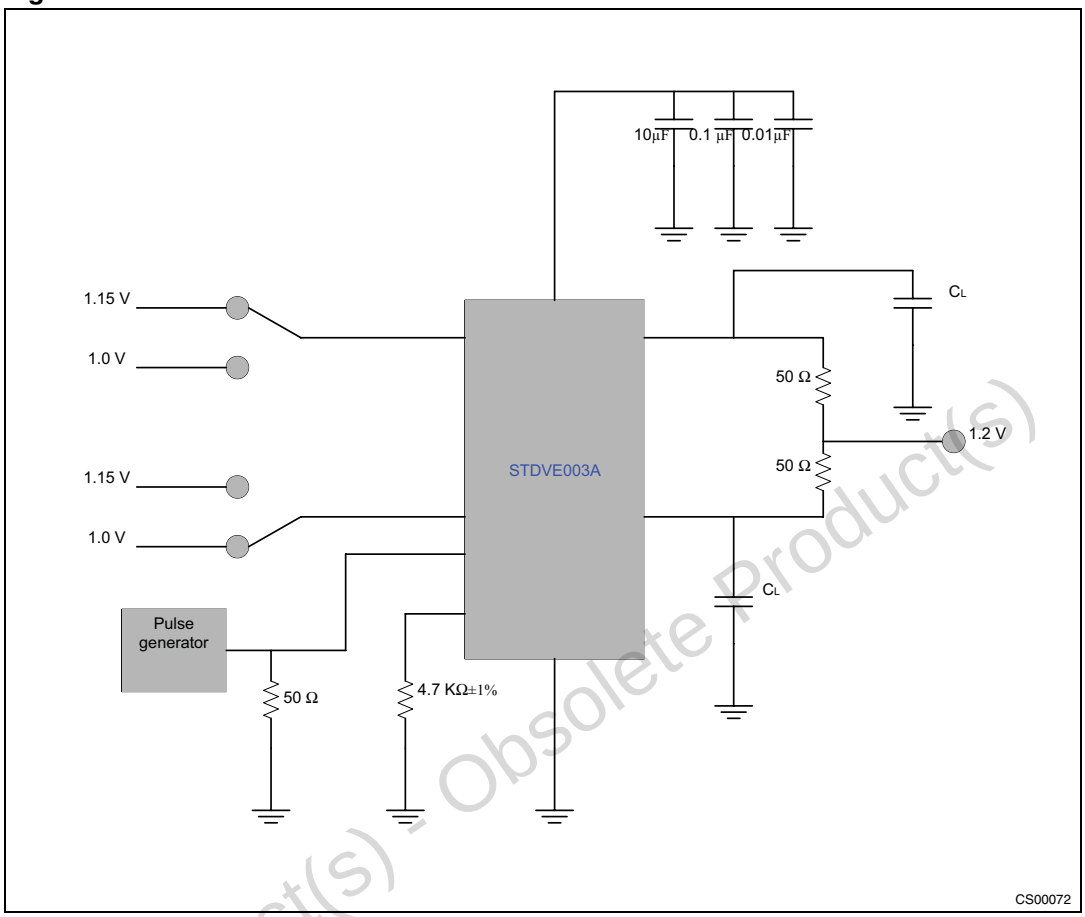
1. Z_O = characteristic impedance of the cable.
2. R_T = termination resistance: should be equal to Z_O of the cable. Both are equal to 50_W.

Figure 9. Test circuit for HDMI receiver and driver



1. $R_T = 50\ \Omega$

Figure 10. Test circuit for turn off and turn off times



1. C_L = 5 pF

Figure 11. Test circuit for short circuit output current

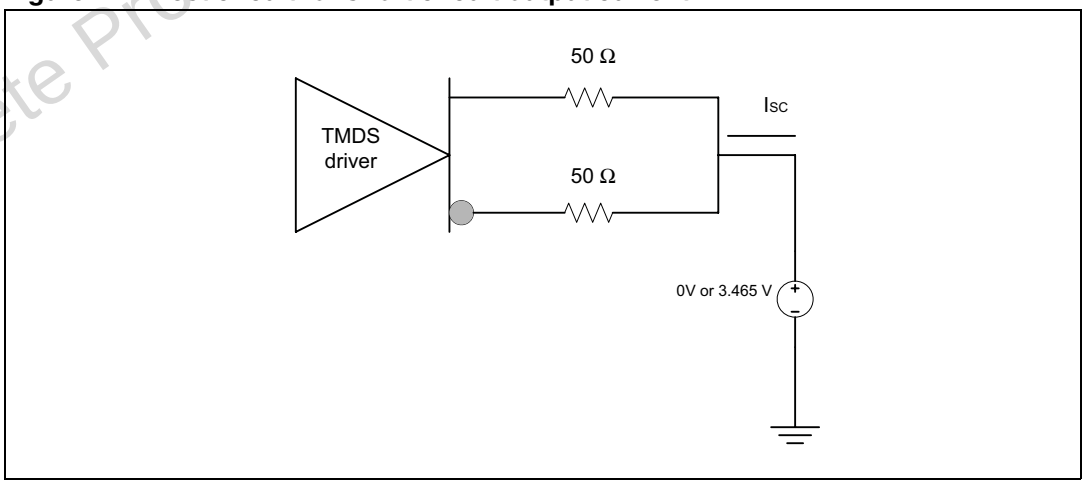


Figure 12. Propagation delays

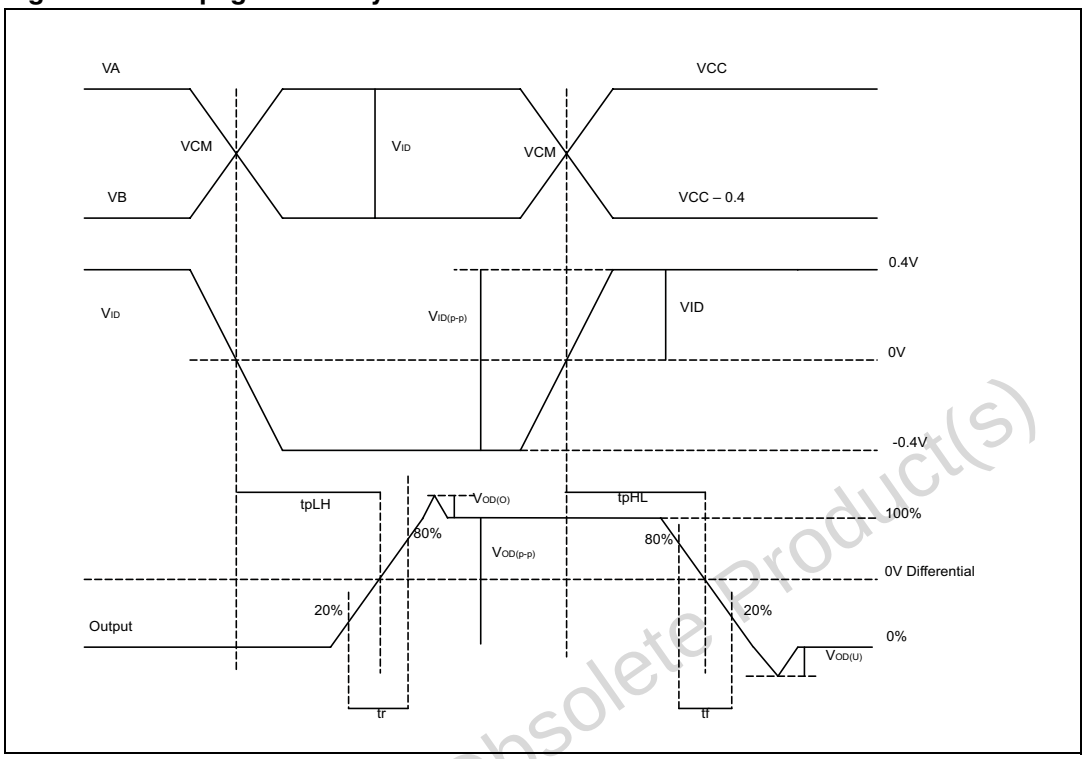


Figure 13. Turn-on and turn-off times

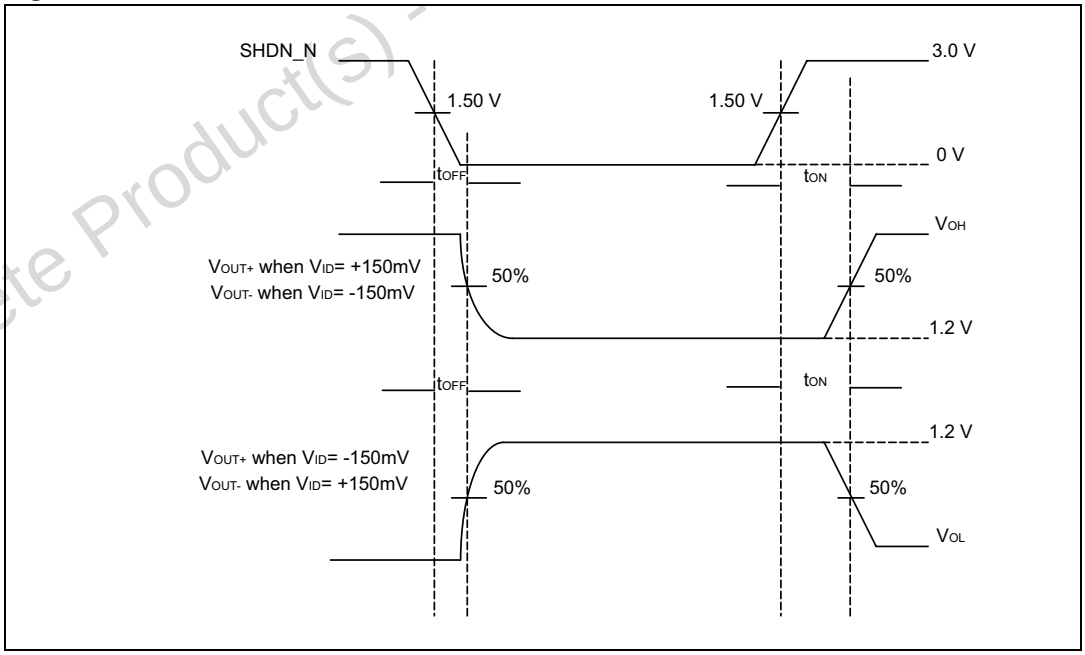


Figure 14. TSK(O)

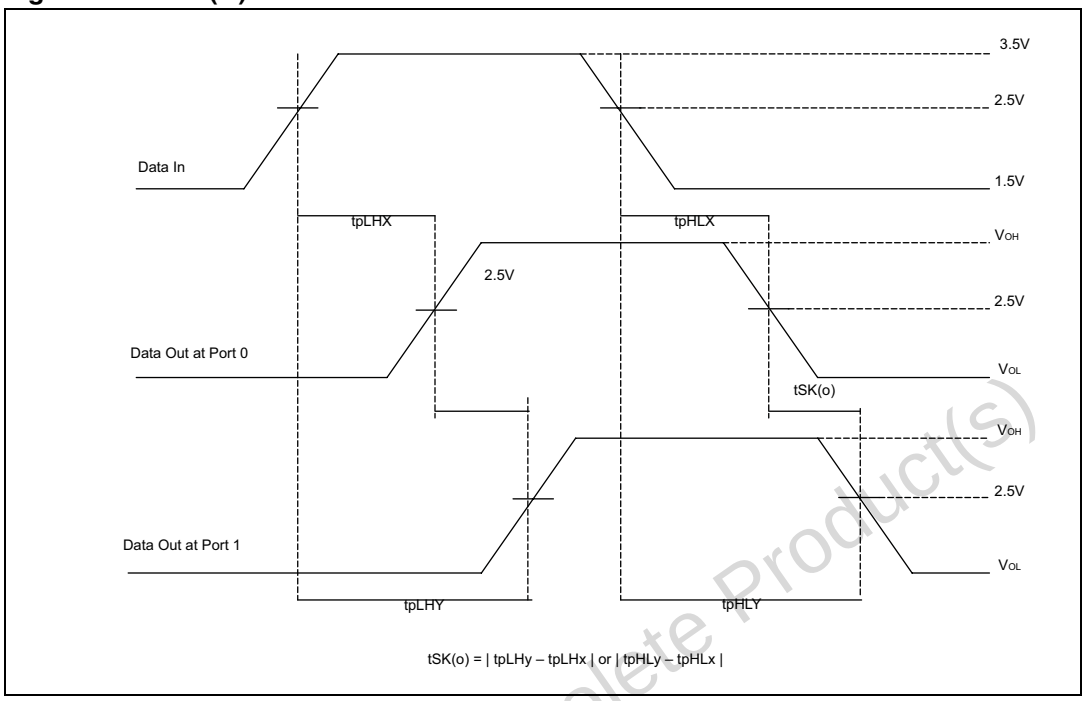


Figure 15. TSK(P)

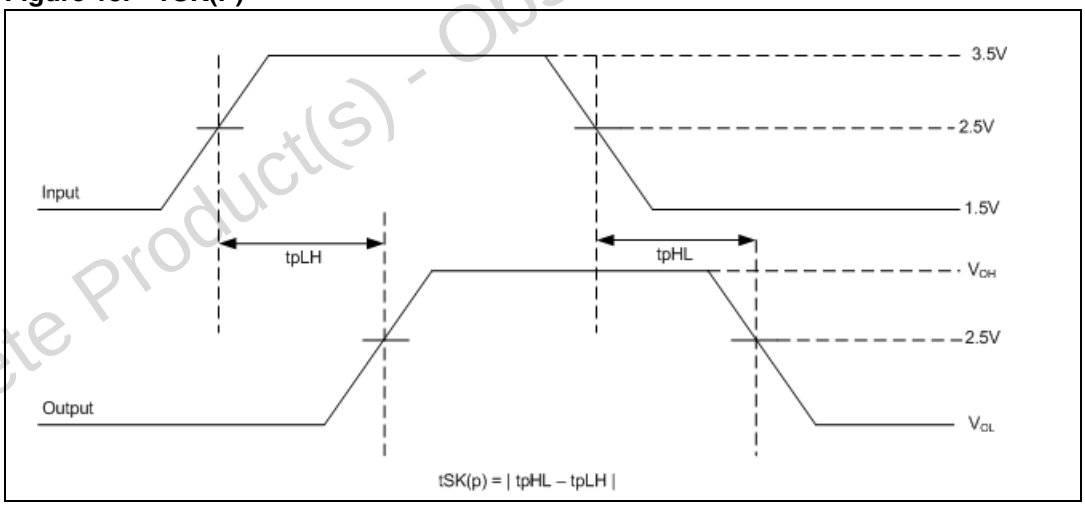


Figure 16. TSK(D)

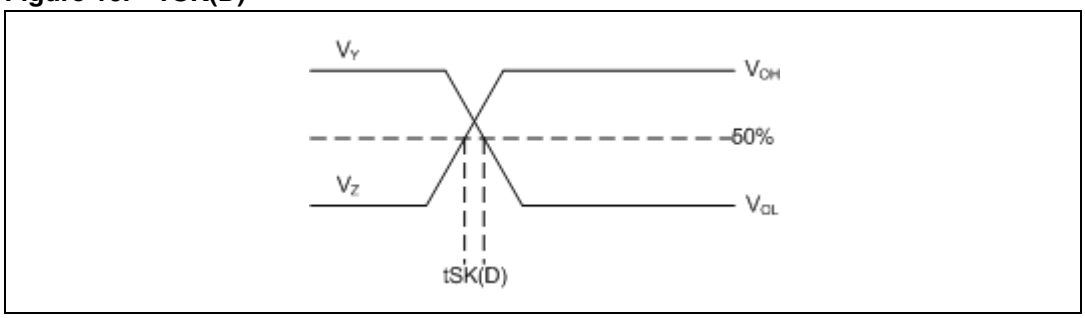


Figure 17. AC waveform 1 (I^2C lines)

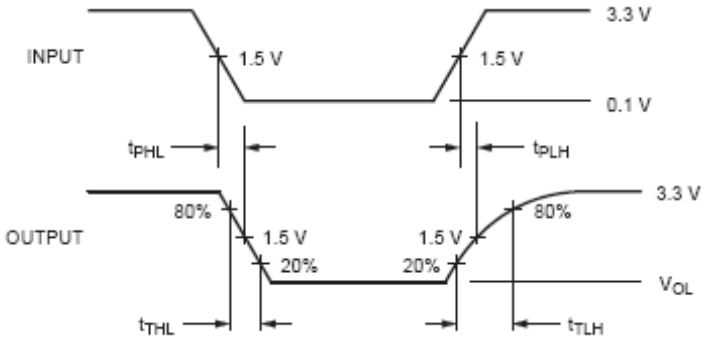
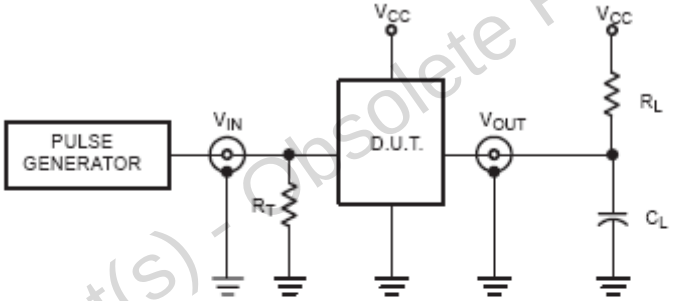


Figure 18. Test circuit for AC measurements (I^2C lines)



Test Circuit for Open Drain Outputs

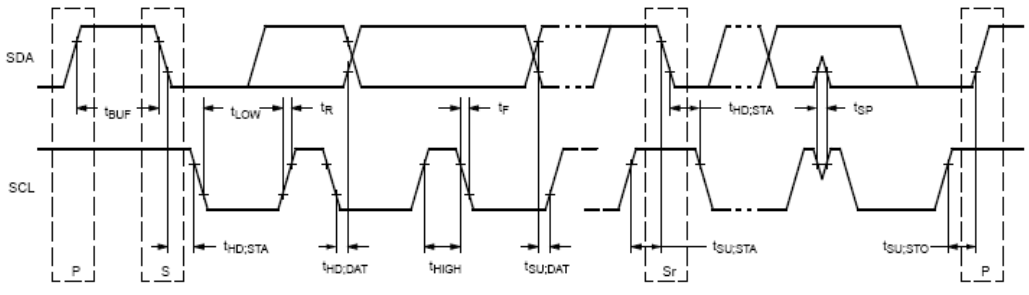
DEFINITIONS

R_L = Load resistor; 1.35 kΩ

C_L = Load capacitance includes jig and probe capacitance; 7 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 19. I^2C bus timing



5 Application information

5.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

5.2 Power supply requirements

Bypass each of the V_{CC} pins with 0.1 µF and 1 nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V_{CC} pin of the device as possible.

All V_{CC} pins can be tied to a single 3.3 V power source. A 0.01 µF capacitor is connected from each V_{CC} pin directly to ground to filter supply noise. The maximum power supply variation can only be ±5% as per the HDMI specifications.

The maximum tolerable noise ripple on 3.3 V supply must be within a specified limit.

5.3 Differential traces

The high-speed TMDS inputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

(a) Maintain 100-Ω differential transmission line impedance into and out of the STDVE003A.

(b) Keep an uninterrupted ground plane below the high-speed I/Os.

(c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.

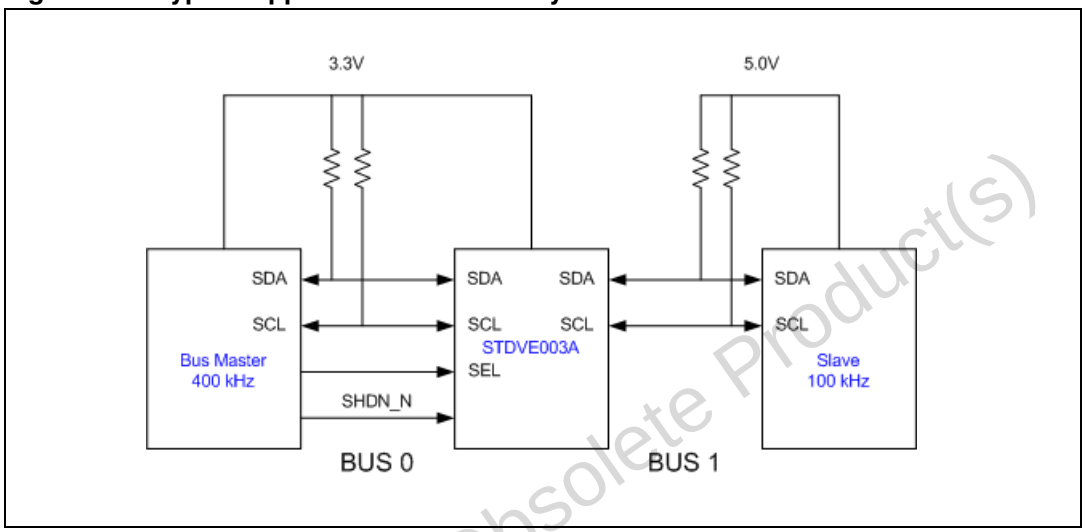
(d) Layout of the TMDS differential inputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STDVE003A. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

5.3.1 I²C lines application information

A typical application is shown in the figure below. In the example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

Figure 20. Typical application of I²C bus system



The STDVE003A DDC lines are 5 V tolerant; so it does not require any extra circuitry to translate between the different bus voltages.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 21. TQFP80 package outline

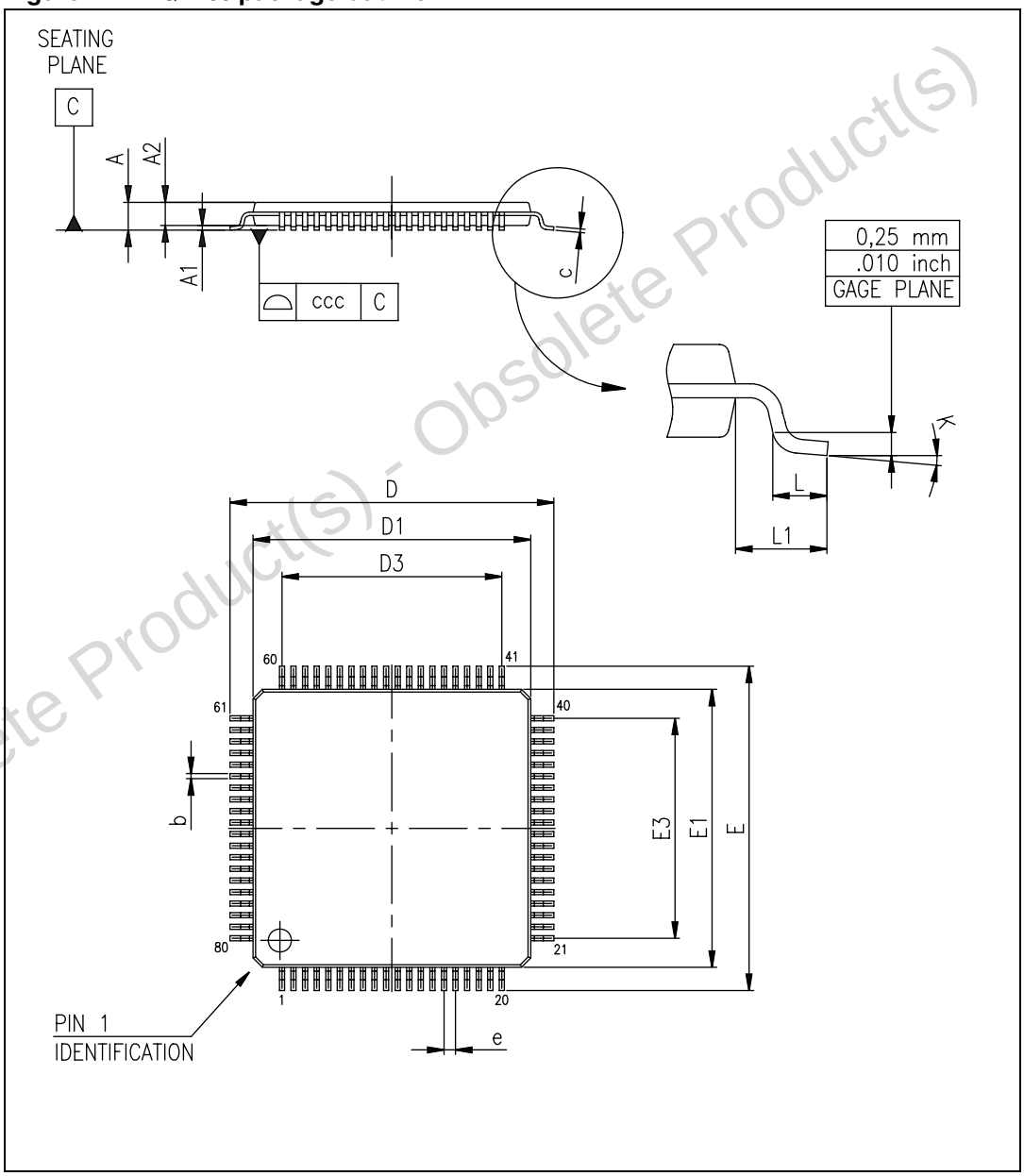
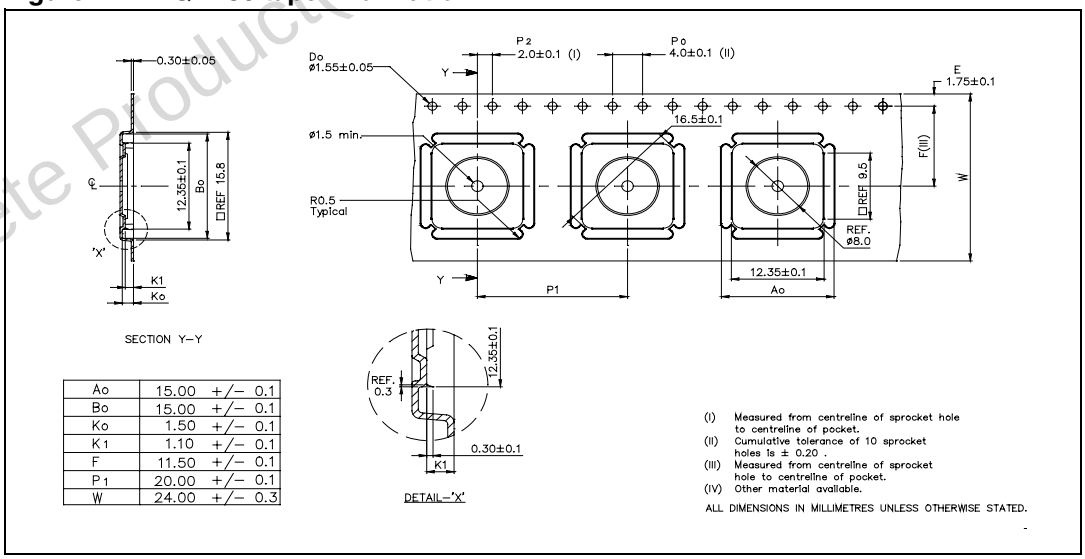


Table 30. TQFP80 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.950	1.000	1.050
b	0.170	0.220	0.270
c	0.090		0.200
D		14.000	
D1		12.000	
D2		9.500	
e		0.500	
E		14.000	
E1		12.000	
E2		9.500	
L	0.450	0.600	0.750
L1		1.000	
k	0°		7°
ccc		0.080	

Figure 22. TQFP80 tape information



Ao	15.00	+/− 0.1
Bo	15.00	+/− 0.1
Ko	1.50	+/− 0.1
K1	1.10	+/− 0.1
F	11.50	+/− 0.1
P1	20.00	+/− 0.1
W	24.00	+/− 0.3

Figure 23. Reel information

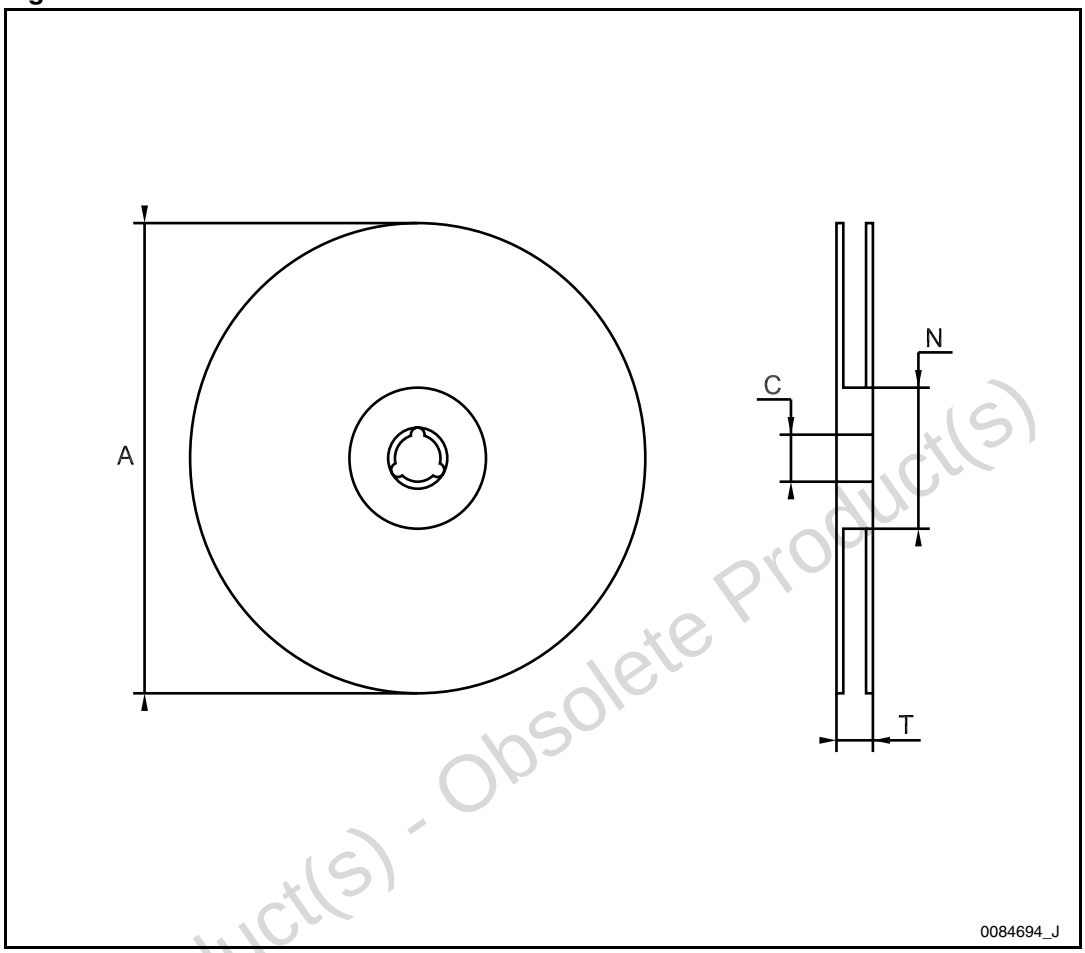


Table 31. Reel mechanical data (dimensions in mm)

A	C	N	T
330.2	13 ±0.25	178	24.4

7 Revision history

Table 32. Document revision history

Date	Revision	Changes
23-Apr-2008	1	Initial release.
26-May-2008	2	Minor updates: *Table 4*,*Table 7*, *Table 23* and *Table 29*.
21-Jul-2008	3	Added: Fully automatic adaptive equalizer feature Modified: title, features *Chapter 3.1* and *Figure 2* Removed: *Table 21.: Equalizer gain*
01-Dec-2008	4	Updated ESD information in the Features section and *Table 29: ESD performance on page 29*. Modified *Section 3.6: Power-down condition on page 14* and *Table 7: Absolute maximum ratings on page 16*.