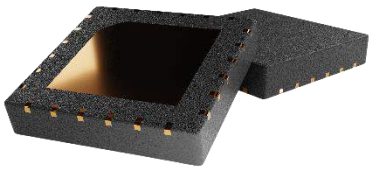
A NEW ARCHITECTURE FOR "ALWAYS EFFICIENT" POWER SUPPLIES

FEATURES

- Designed for high efficiency, low-cost, compact and lightweight AC/DC power supplies from 1-10kW+
- Universal Input AC85 – 305V
- High efficiency (99.5% peak) across the full load range
- Inrush current completely eliminated
- Compatible with any suitable DC/DC converter
- Meets EMC Class B
- Optional Active Bridge to further improve efficiency
- Suitable for a variety of high-volume consumer applications including Laptops, TV's, Battery Chargers, LED Lighting and Industrial Power Supplies.



Part Number	Power (W)	Package	Packaging
PSV-AD-150-Q24IvS	<150	QFN(24)	Small Tape & Reel
PSV-AD-150-Q24IvR	<150	QFN(24)	Large Tape & Reel
PSV-AD-250-Q24IvS	<250	QFN(24)	Small Tape & Reel
PSV-AD-250-Q24IvR	<250	QFN(24)	Large Tape & Reel
PSV-AD-10K-Q24IvS	250 – 10k	QFN(24)	Small Tape & Reel
PSV-AD-10K-Q24IvR	250 – 10k	QFN(24)	Large Tape & Reel

Table 0 - Device summary

OVERVIEW

The PSV-AD-xx controller family has been designed to make power supplies more sustainable while reducing overall system cost. This scalable solution delivers efficient AC/DC conversion using smaller, lower cost, and more robust system components. Pulsiv's unique switching architecture and intelligent control techniques have been combined to deliver consistent performance across the full load range and meet strict efficiency requirements at low power. The PSV-AD-xx circuit can interface with any compatible DC/DC converter to produce ultra-compact power supplies up-to and beyond 10kW.
Please note that the default system components recommended by Pulsiv in this document have been fully optimised for cost and customers have the freedom to replace any parts where performance takes priority.

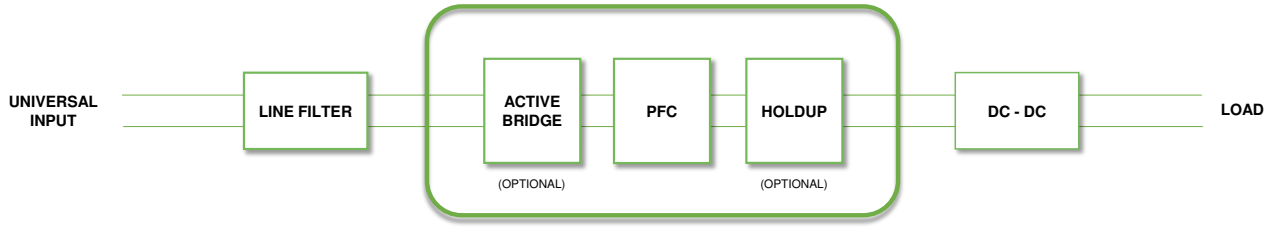


Figure 0a: PSV-AD-xx system block diagram

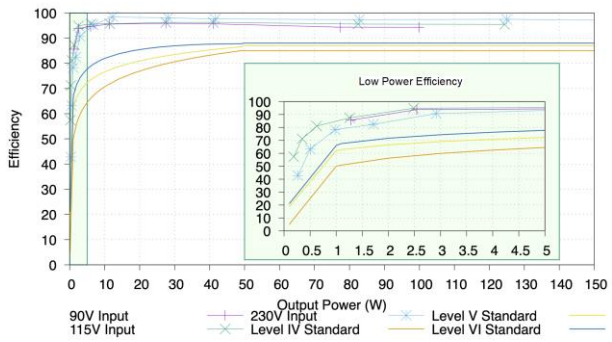


Figure 0b: System Efficiency* Measured on a PSV-AD-250-DS Development System

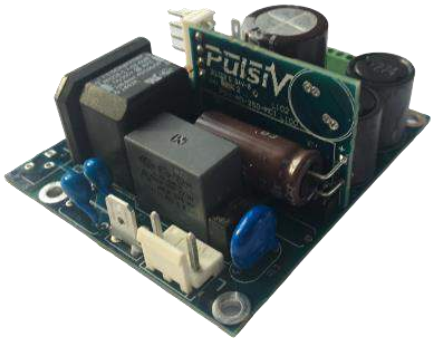


Figure 0c: PSV-AD-250-DS Development System

*Efficiency graph shows Pulsiv performance compared to the Energy Star standard (for external power supplies)

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1 DESCRIPTION

Pulsiv has developed a unique way of converting electricity from AC to DC by applying patented switching techniques and integrating many system functions into one controller. Regulating capacitor charging using switch S_1 and discharging with a diode switch S_2 delivers a number of system benefits that will be described later in this document.

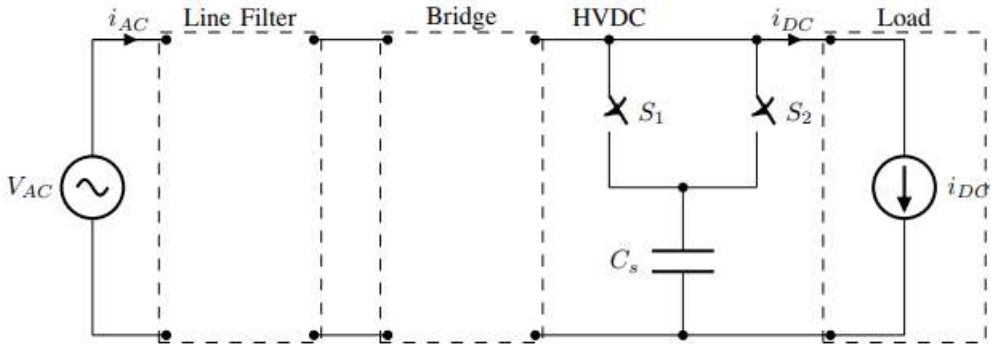

Figure 1a: Unique Switching Architecture

The normalised High Voltage DC (HVDC) line and typical normalised capacitor voltage illustrate Pulsiv's unique approach. Energy is stored in a Capacitor when the AC line is at a high voltage and used to supply the load when the AC line voltage is low. Designs can achieve 0.95 power factor and a peak efficiency of 99%.

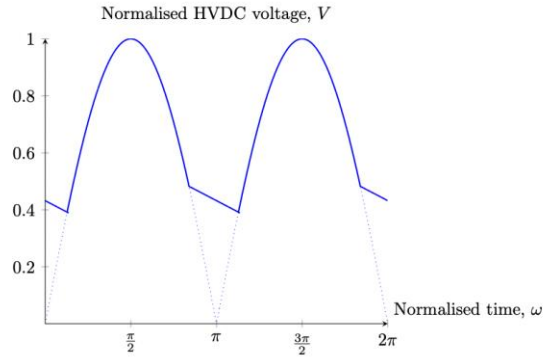

Figure 1b: Normalised HVDC Voltage (V)

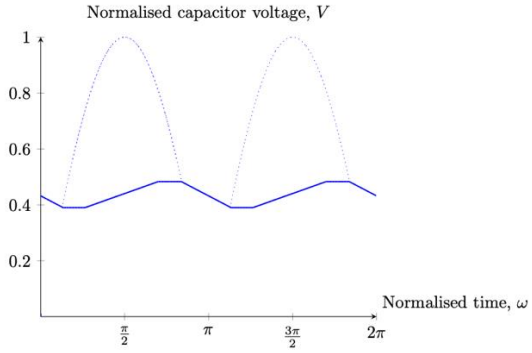

Figure 1c: Normalised C_s Voltage (V)

Standards like IEC61000-3-2, set limits on harmonic currents to improve power factor. Many technical solutions exist to help address this challenge, but none are like the PSV-AD-xx controller family. It delivers high power-factor and efficiency without using a switched PFC inductor; avoiding the need to boost the voltage into the power stage. This provides significant efficiency gains at low power and produces an inherent high efficiency across the power range.

A rich set of signals manage PFC switching, active bridge control, configurable HVDC voltage, X-capacitor discharge, configurable hold-up time, auxiliary power supply management and provides an early-warning if the grid supply fails. The device can be completely disabled and placed into a low-power mode.

The PSV-AD-xx controller regulates the charging of capacitor Cch by controlling the switching of Qch in a power supply system. Open-loop charging current is limited by Rch with inductor Lch selected to ensure sufficient charge is passed into Cch for the desired load requirements. Discharging Cch is achieved through Dd and controlled by the follow-on DC/DC converter or a load connected to HVDC. Diode Dch prevents Cch discharging through the body diode of Qch. Df is a freewheeling diode associated with Lch.

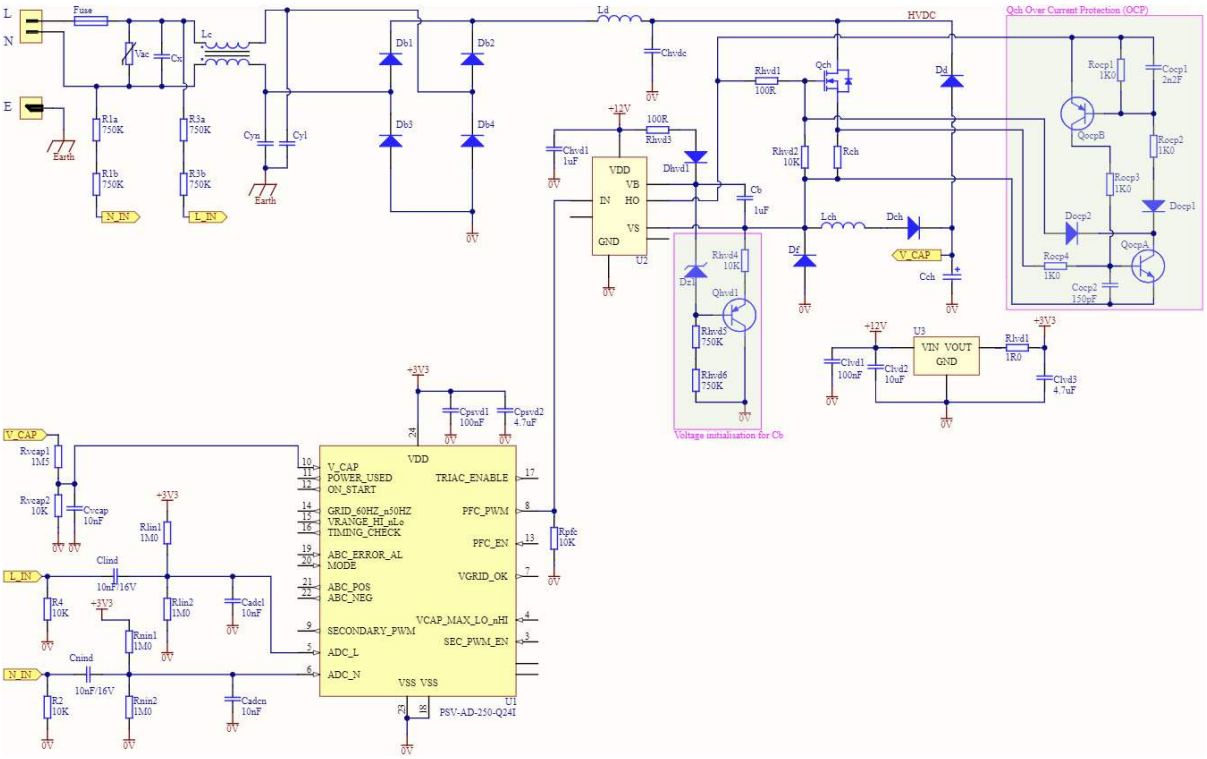

Figure 1b: PSV-AD-xx Controller Basic Functional Schematic

Description	Designator	Quantity	MANUF PN#1
IC MCP1799T-3302H LDO 3.3V 80mA -40/+150	U3	1	MCP1799T-3302H
RES 0603 TF 1R0 1% 0.25W -55/+155	Rlvd1	1	CRGP0603F1K0
CAP 0603 X7R 100NF 50V 10% -55/+125	Clvd1	1	CGA3E2X7R1H104K080AA
CAP 0805 X7R 4U7F 25V 10% -55/+125	Clvd3	1	CC0805KKX7R8BB475
CAP 1206 X7R 10UF 25V 10% -55/+125	Clvd2	1	TMK316B7106KL-TD
DIO RECTIFIER 600V 3A SMB	Db1, Db2, Db3, Db4	4	ES3JB-13-F
IND CHOKE 10mH@ 10kHz 1.4A 300V -40/+100	Lc	1	RN218-1-4-02-10M
CAP 1812 X7R 100NF 1KV 10% -55/+125	Chvdc	1	C1812X104KDRACTU
IND FER 68uH 2A 20% -40/+105	Ld	1	7447033
FUS PTH MINI 3.15A 250V	Fuse	1	0697A3150-01
VAR TVS 10MM DISC 3.5KV 275VAC	Vac	1	B72210S2271K101
CAP PTH PP 0.68uF 305VAC 10% -40/+110	Cx	1	B32922C3684K189
CAP PTH CER XY 1nF 250VAC 20% -20/+125	Cyl, Cyn	2	C901U102MYVDBA7317
PSV-AD-250 PFC CONTROLLER QFN-24	U1	1	PSV-AD-250-Q24I
CAP 0402 X7R 100NF 16V 10% -55/+125	Cpsvd1	1	GCM155R71C104KA55D
CAP 0805 X7R 4U7F 25V 10% -55/+125	Cpsvd2	1	CC0805KKX7R8BB475
CAP 0402 X7R 10NF 16V 10% -55/+125	Cadcl, Cadcn, Clind, Cnind, Cvcap	5	EMF105B7103KVHF
WE-PD4 SMT Power Inductor, Type X, 330µH, 1A, 0.56O	Lch	1	74458233
RES 1210 TF 0.22R 1% 500mW -55/+155	Rch	1	RL1210FR-070R22L
DIO RECTIFIER 600V 1A SOD-123FL	Dch	1	US1JFA
DIO RECTIFIER 600V 1A SOD-123FL	Dd	1	US1JFA
DIO RECTIFIER 600V 1A SOD-123FL	Df	1	US1JFA
RES 0402 TF 10K 1% 0.062W -55/+155	Rhvd2	1	CRCW040210K0FKEDC
RES 0603 TF 100R 1% 0.1W -55/+150	Rhvd1	1	RMCF0603FT100R
TRN MOSFET N-CH 600V 0R18 TO252-3 -40/+150	Qch	1	IPD60R180P7SAUMA1
RES 0402 TF 10K 1% 0.062W -55/+155	Rpfc	1	CRCW040210K0FKEDC

IC FAN73611 PWR MAN GATE DRIVER 20V SOP-8	U2	1	FAN73611MX
CAP 0805 X7R 1U0F 25V 10% -55/+125	Cb	1	C0805C105K3RECAUTO
DIO ZENER 12V 200mW SOD323FL	Dz1	1	MM3Z12VC
RES 0402 TF 10K 1% 0.062W -55/+155	Rhvd4	1	CRCW040210K0FKEDC
RES 0805 TF 750K 1% 0.25W -55/+155	Rhvd5, Rhvd6	2	SG73S2ATTD754G
TRN PNP 500V 150MA SOT23 -55/+150	Qhvd1	1	PBHV9050T,215
RES 0603 TF 100R 1% 0.1W -55/+150	Rhvd3	1	RMCF0603FT100R
DIO RECTIFIER 600V 1A SOD-123FL	Dhvd1	1	US1JFA
CAP 0805 X7R 1U0F 25V 10% -55/+125	Chvd1	1	C0805C105K3RECAUTO
WCAP-AT1H Aluminum Electrolytic Capacitor, Radial THT, D18xH35.5mm, 330uF, 200V	Cch	1	860241081001
CAP 0402 C0G 150PF 50V 5% -55/+125	Cocp2	1	C0402C151J5GACTU
CAP 0402 X7R 2.2NF 50V 10% -55/+125	Cocp1	1	0402B222K500CT
DIO GEN PURP 100V 2A SOD323-2 +150	Docp2	1	BAS16WS-E3-08
DIO GEN PURP 100V 2A SOD323-2 +150	Docp1	1	BAS16WS-E3-08
RES 0402 TF 1K0 1% 0.062W -55/+155	Rocp1, Rocp2, Rocp3, Rocp4	4	SFR01MZPF1001
TRN NPN/PNP GEN PURP X2 45V 0.1A SOT23-6	Qocp	1	BC847BPN,115
RES 0402 TF 10K 1% 0.062W -55/+155	R2, R4, Rvcap2	3	CRCW040210K0FKEDC
RES 0805 TF 750K 1% 0.25W -55/+155	R1a, R1b, R3a, R3b	4	SG73S2ATTD754G
RES 0805 TF 1.5M 1% 0.25W -55/+155	Rvcap1	1	RK73H2ATTD1504F
RES 0402 TF 1M0 1% 0.062W -55/+155	Rlin1, Rlin2, Rnin1, Rnin2	4	CRCW04021M00FKEDC

Figure 1c: PSV-AD-xx Controller Basic Functional Schematic Bill-of-Materials

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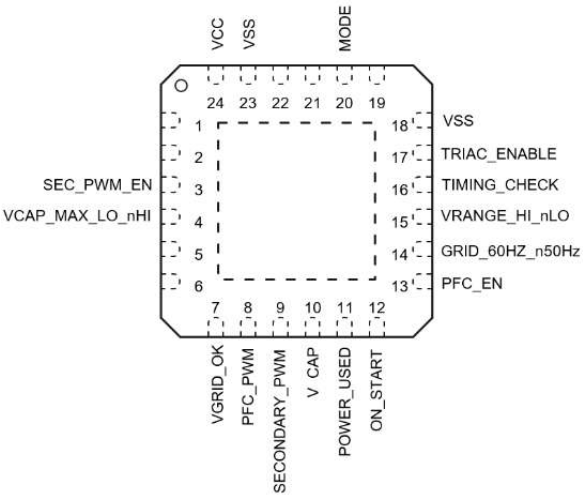
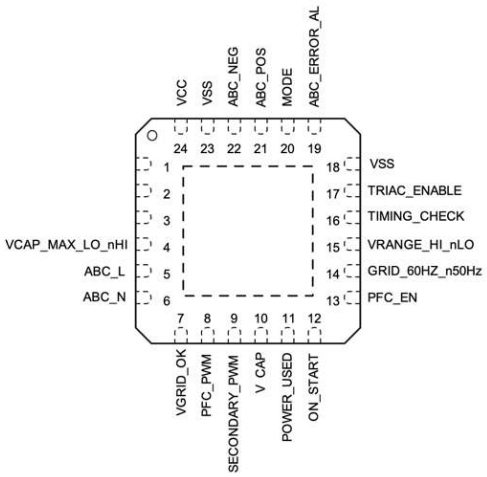
1.1 PSV-AD-xx Pin Connections (Top View)



PSV-AD-050-Q24lv &
PSV-AD-150-Q24lv



PSV-AD-250-Q24lv

Under Development

PSV-AD-10K-Q24lv

1.2 Pin Functions

#	Name	Type	Description
1	Not Connected		
2	Not Connected		
3	SEC_PWM_EN	Digital Input	Enables SECONDARY_PWM output (low to disable)
4	VCAP_MAX_LO_nHI	Digital Input	Set max Cch capacitor voltage (High=150V Low=180V)
5	ADC_L	ADC Input	Scaled line voltage
6	ADC_N	ADC Input	Scaled neutral voltage
7	VGRID_OK	Digital Output	High when grid voltage is above 50V, low otherwise
8	PFC_PWM	Digital Output	PWM control for PFC
9	SECONDARY_PWM	Digital Output	Additional PWM for an auxiliary power supply or boost stage
10	V_CAP	ADC Input	Scaled storage capacitor voltage
11	POWER_USED	Digital Output	Switching frequency indicates power consumption
12	ON_START	Digital Output	This signal and TIMING_CHECK indicate controller state
13	PFC_EN	Digital Input	Enable normal operation (low to disable)
14	GRID_60HZ_n50HZ	Digital Output	Grid frequency indicator (60Hz, high; 50Hz, low)
15	VRANGE_HI_nLO	Digital Output	Indicates Cch voltage setting (155V, high; 85V, low)
16	TIMING_CHECK	Digital Output	This signal and ON_START indicate controller state
17	TRIAC_ENABLE	Digital Output	Drives external thyristor holdup circuit (if required)
18	V_{ss}	Ground	
19	*ABC_ERROR_AL	Digital Input	Active Bridge error detected (low signals an error)
20	MODE	Digital Input	Enable X Capacitor discharge during shutdown (active high)
21	*ABC_POS	Digital Output	Active bridge waveform, positive cycle switch
22	*ABC_NEG	Digital Output	Active bridge waveform, negative cycle switch
23	V_{ss}	Ground	
24	V_{cc}	Power	Operating supply voltage

These pins indicate the status of the system
These pins control the behaviour of the system
These pins indicate analogue inputs to the system

Part Number	Power Rating (W)	Active Bridge Support	DC/DC intelligent control
PSV-AD-150-Q24IvS	150	No (use AD-250)	No
PSV-AD-150-Q24IvR	150	No (use AD-250)	No
PSV-AD-250-Q24IvS	250	Yes	No
PSV-AD-250-Q24IvR	250	Yes	No
PSV-AD-10K-Q24IvS	250 – 10K	Yes	Yes
PSV-AD-10K-Q24IvR	250 – 10K	Yes	Yes

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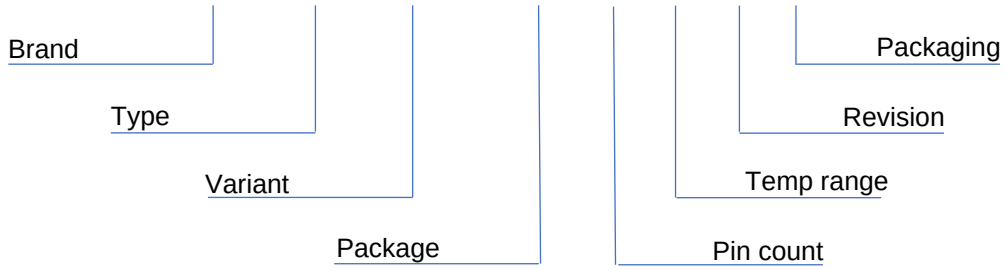
1.3 Numbering System

1.3.1 Integrated Circuit Numbering

PSV - AD - 150xx - Q 24 I V S



Descriptor	Meaning
Brand	PSV = Pulsiv
Type	AD = AC/DC controller
Variant	150 = Output power capability (W) xx Specific Feature set
Package	Q = QFN
Pin count	24
Temp range	-40 ◦C to 85 ◦C
Revision	
Packaging	S = Small reel R = Large Reel Blank = Tube or tray

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2 ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Min.	Max.	Unit
V_{ss}	Applied voltage to any pin except GND	-0.3	4.1	V
I_{max}	Current to any pin		±2	mA
T_{stg}	Storage temperature(2)	-40	125	°C
T_j	Maximum junction temperature		85	°C
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(3)		±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(4)		±2	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(3) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

3 THERMAL DATA

Symbol	Parameter	VQFN 24	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-to-Ambient	32.6	°C/W

4 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Nom.	Max.	Unit
V_{cc}	Supply voltage(1)(2)	1.8		3.6	V
V_{ss}	Supply voltage ground		0		V
T_A	Operating free-air temperature	-40		85	°C
T_J	Operating junction temperature	-40		85	°C
C_{DVCC}	Recommended capacitor at V_{cc} (3)	4.7	10		µF

(1) Supply voltage changes faster than 0.2 V/µs can trigger a reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor CDVCC limits the slopes accordingly.
(2) Pulsiv recommends that power to the DVCC pin must not exceed the limits specified in Recommended Operating Conditions. Exceeding the specified limits can cause malfunction of the device.
(3) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimetres) to the respective pin pair.

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4.1 Digital Inputs

Parameter		Test Conditions	Vcc	Min	Typ.	Max	Unit
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (VIT+ – VIT–)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: VIN = VSS For pulldown: VIN = VCC		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	VIN = VSS or VCC			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analogue functions	VIN = VSS or VCC			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current	See (1) (2)	2 V, 3 V	–20		20	nA

(1) The leakage current is measured with VSS or VCC applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

4.2 Digital Outputs

Parameter		Test Conditions	Vcc	Min	Typ.	Max	Unit
V_{OH}	High-level output voltage	I(OHmax) = –3 mA(1)	2 V	1.4		2.0	V
		I(OHmax) = –5 mA(1)	3 V	2.4		3.0	
V_{OL}	Low-level output voltage	I(OLmax) = 3 mA(1)	2 V	0.0		0.60	V
		I(OHmax) = 5 mA(1)	3 V	0.0		0.60	

(1) The maximum total current, I(OHmax) and I(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies

4.3 ADC Power Supply and Input Range Conditions

Parameter		Test Conditions	Vcc	Min	Typ.	Max	Unit
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analogue input voltage range	All ADC pins		0		DV_{CC}	V
C_I	Input capacitance		2.2 V		1.6	2.0	pF

5 DESIGN GUIDE

Depending upon power requirements, the basic PSV-AD-xx system is configured by selecting Cch, Lch and Qch. Please note that any capacitance from a follow-on DC/DC converter will interact with the PSV-AD-xx. Typically, the capacitance of the follow-on DC/DC should be kept to a minimum (for 120W, it should be less than 0.5uF).

5.1 Capacitor Selection (Cch)

The storage capacitor selection is determined by output power requirements. Care should be taken so that the capacitor meets the ripple current required by the load during the discharge phase. The capacitor selection assumes a constant power discharge, and sufficient capacitance must be provided to ensure a minimum holdup voltage for the DC/DC converter stage. The storage capacitor is charged based on the value of the input voltage (95V in 115VAC systems and 155V in 220VAC systems). With constant power loads, the potential across a capacitor at a given elapsed time, t, is given by the initial holdup voltage, V_h, the power drawn, P, and capacitance, C:

$$V_c(t) = \sqrt{V_h^2 - 2\frac{P}{C}t}$$

The discharge time of the capacitor determines the minimum voltage reached and is approximated by solving for time in this equation:

$$\sqrt{2}V_{RMS}(2\pi ft) - V_h = \sqrt{V_h^2 - 2\frac{P}{C}t}$$

This gives a simple upper limit of:

$$t \leq \frac{V_h}{\pi f \sqrt{2} V_{RMS}}$$

For common grid voltages and frequencies, this equates to a discharge time of approximately 3mS and the minimum required capacitance is given by:

$$C = \frac{P}{(V_h - V_{min})(V_h + V_{min})} 6 \cdot 10^{-3}$$

For universal input designs, 160V rated capacitors can be used. The relationship between power and capacitance is linear; so sufficient capacitance should be selected. Typical values are provided in Table 5.1a. Ripple current rating for the capacitor will depend on the DC/DC converter stage. The typical capacitor current waveshape is shown by Figure 5.1a; with the capacitor charge being equal (in steady state conditions) during the charge and discharge cycles. The RMS current rating of the capacitor needs to be reviewed based on the current drawn by the DC/DC stage. A simple guide is to use the discharge voltage difference and discharge time to determine the average discharge current.

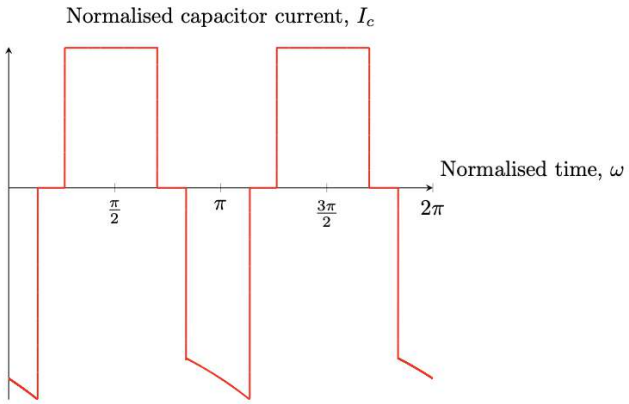


Figure 5.1a – Typical Current Waveshape For Cch

The RMS capacitor current can be determined by analysing the capacitor voltage waveform, which shows a constant current charge and constant power discharge. Assuming a typical charge time of 5mS and a discharge time of 3mS; the RMS capacitor current can be estimated as shown in the table below. The actual RMS current needs to be determined once the charge and discharge currents have been estimated as these will be a function of the DC/DC converter used. Typically, the discharge current will be the dominant term in the capacitor RMS current calculation, and this is determined by the DC/DC converter used.

Capacitance (uF)	Max Power (W)	Min. Voltage (V)	RMS current (A)
90	70	50	0.7
75	70	40	0.8
127	100	50	1.0
107	100	40	1.1
190	150	50	1.5
160	150	40	1.6
230	180	50	1.7
192	180	40	1.9

Table 5.1a – Recommended Capacitor Values and RMS current for Cch (Capacitor Holdup Voltage of 95V for universal input)

Pin 4 on the controller can be used to set the maximum voltage stored on the capacitor. If pin 4 is left open, the maximum capacitor voltage is 150V (enabling the use of a 160V rated capacitor). With the pin pulled to ground, the maximum capacitor voltage is 180V (enabling the use of a 200V rated capacitor). Using a higher rated capacitor provides a higher power factor with 230VAC mains.

The Mean Time Between Failure for Cch is given by:

Parameter	Min		Unit	Notes and conditions
Mean Time Between Failure	19000		Khrs	MIL-HDBK-217F, Notice 2, Style: CE CU CUR, 55°C, Non-Established Reliability, G_B

The measured capacitor temperature (180W electronic load) is 45°C with convection cooling at 30°C ambient. The data was calculated using 55°C, assuming heat from the DC/DC converter increases the capacitor temperature by a further 10°C. This represents a worst-case scenario. The actual MTBF will depend on components used and temperatures of the components.

5.2 Inductor Selection (Lch)

To ensure that the capacitor charging current is properly regulated and to help EMC compliance, the charging circuit includes an inductor. The peak current is limited in hardware, and the switching frequency used to regulate the current dithers around 45kHz using an open-loop control system. The duty cycle is controlled by the PSV-AD-xx to ensure a current-profile that maximises power factor.

As the power requirement changes, Lch can be selected to ensure sufficient charge is stored in Cch during the minimum line voltage condition. With a suitable Cch selected (see section 5.1), the charge required is determined by q = Cch (85 – Vmin), where Vmin is the minimum voltage the DC/DC converter will operate from. The typical charging time is 3mS, and using the charge, and assuming the current in the inductor is in critical conduction mode, the peak current is given by

$$i_{pk} = \frac{2}{3 \times 10^{-3}} C_{ch}(85 - V_{in\_min})$$

The value of Rch is selected using this peak current as a limit. The potential developed across Rch will switch-on the Over Current Protection circuit to limit the peak current. For example, with a minimum DC/DC voltage of 65V, and Cch=220uF, ipk is calculated as 2.9A.
The value of Lch is given using the expression below

$$L_{ch} = \frac{(V_{AC\_pk} - V_{in\_min})}{i_{pk} \cdot f} D$$

Where D=0.7 and f=45kHz are set by the PSV-AD-xx and $V_{AC\_pk}=115\sqrt{2}$ is a typical requirement. With a peak current of 2.9A, and Vin_min = 65 for example, this equates to Lch being 500uH. The expression for Lch assumes charging at the peak of the input line, Cch is at the minimum voltage and current is at critical conduction. It should be noted that the inductor can operate in continuous conduction mode as well; as long as the peak current is below ipk. Various combinations of ipk and Lch can be used.

At the maximum intended power, ipk and Lch can be optimised to ensure that Cch is charged to its maximum value. Suitable starting points for this are provided in the table below.

Max Power (W)	Min Voltage (V)	Min Cch (uF)	ipk (A)	Rch (Ohm)	Typical Lch (uH)
30	65	60	0.80	0.88	1898
60	65	120	1.60	0.44	949
110	65	220	2.93	0.24	518
150	65	300	4.00	0.18	380
180	65	360	4.80	0.15	316
200	65	400	5.33	0.13	285
220	65	440	5.87	0.12	259
250	65	500	6.67	0.11	228

A suitable inductor can be designed to maximise efficiency or minimise cost. The current-limiting hardware can be changed by modifying Rch and the associated circuit in Figure 1b.

5.3 MOSFET Selection (Qch)

Only conduction loss and switching loss are considered in selecting suitable MOSFETs. The nomograms in Appendix A.1 can be used to determine suitable MOSFETs using RDS(on) and rise/fall switching times. Actual losses depend on charging time, HVDC voltage and capacitor voltage; however suitable MOSFETs include:

Device	RDS(on)	t_r (nS)	t_f (nS)
IPN60R1K0CEATMA1	1.10	8	13
IPN60R600P7SATMA1	0.60	6	19
IPN60R360P7SATMA1 (fitted)	0.36	7	10

Table 5.3a – Recommended MOSFET for Qch

5.4 Hold-up Circuit (optional) and Capacitor Selection

For applications that require hold up, an optional circuit can be used. The connection marked BULK_EN should be connected as shown in Figure 5.4a.

The circuit ensures that when the HVDC goes below a threshold (determined by the 3 x 2M2 resistor network) a Thyristor will be enabled so that the response to a loss in HVDC potential is controlled by hardware rather than software. This setup can cause an inrush current during initialisation when the HVDC potential is low. To control the Thyristor during initialisation, the PSV-AD-xx includes a means of inhibiting this inrush current.

A suitable capacitance value can be determined by calculating the energy required during the holdup phase, the peak grid voltage, the desired holdup time and load power. The minimum operating voltage of the DC/DC converter is also required to calculate the capacitance. For example, if the required power is 120W and the required holdup time is 12mS, this equates to an energy requirement of 120W x 12mS = 1.44J. Assuming the DC/DC converter can operate from a minimum of 35V, and assuming the grid is at 115V RMS, which equates to $115\sqrt{2}$ V maximum; this gives the required capacitance as
C = 2 x Energy Required / ($V_{max}^2 - V_{min}^2$) = 2 x 1.44 / (115 x 115 x 2 – 35 x 35) = 115 uF

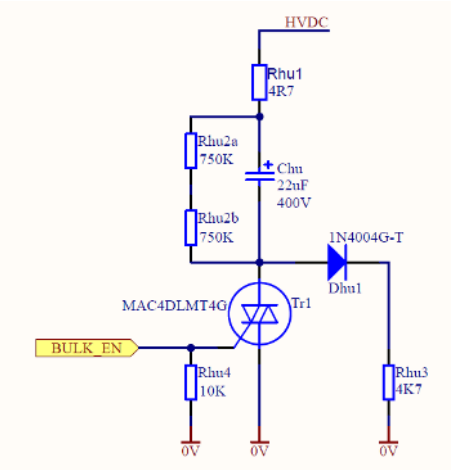


Figure 5.4a - External Components for the PSV-AD-xxx Circuit to Provide System Holdup

5.5 Active Bridge (optional)

The active bridge signals provided by the PSV-AD-xx controller can be used to drive a high-side low-side MOSFET configuration that increases overall efficiency by up to 1.4% (90VAC line input). This is increasingly important at higher power levels and a half active bridge provides efficiency improvement using only two MOSFET's as shown below (ideal for 150-200W designs). A full active bridge can be implemented with very few additional components (please contact Pulsiv for details).

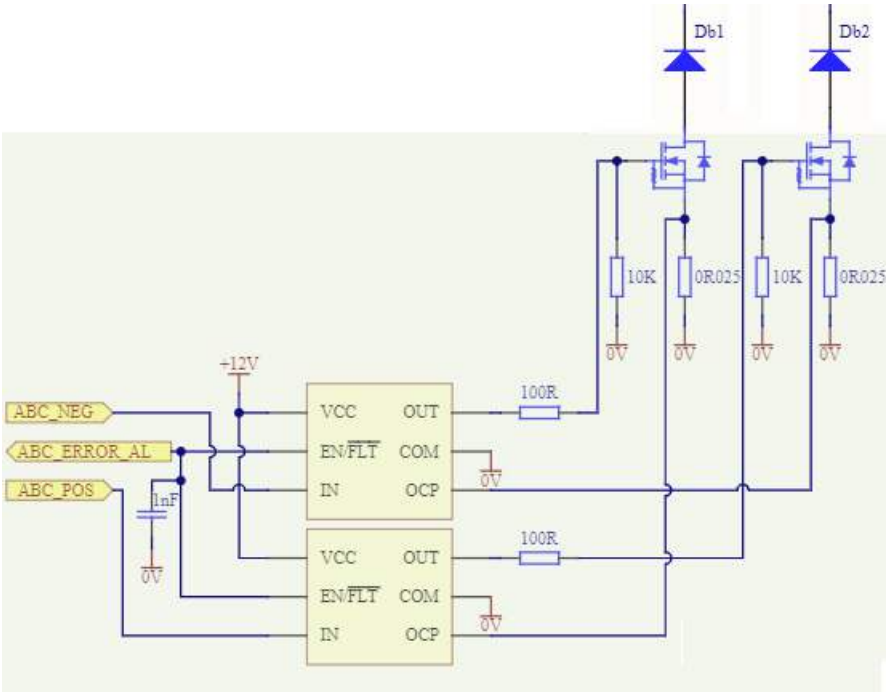


Figure 5.5a - PSV-AD-xx System Active Bridge Circuit

The operation of the PSV-AD-xx provides a natural deadtime of approximately 3mS, enabling robust and safe switching to prevent shoot through. Fitting the active bridge automatically provides the X-capacitor discharge function without requiring additional circuitry.

5.6 Power Used

The POWER_USED pin displays real-time power consumption by toggling at a fixed rate.

Our method does not require expensive current measurement techniques, but performs a calculation $(\text{Vcap charged})^2$ - $(\text{Vcap discharged})^2$ during each grid cycle, which is directly proportional to the power.

Using the recommended value of Cch:
Low power = 0-25% of the rated power = 1.5Hz POWER_USED output frequency
Medium power 26-75% of the rated power = 4Hz POWER_USED output frequency
High power = 76-100% of the rated power= 12Hz POWER_USED output frequency

Choosing a different value of Cch to those recommended will require POWER_USED to be characterised.

5.7 Using SECONDARY_PWM

The SECONDARY_PWM output can be used to drive an auxiliary supply for systems that need power when the DC-DC converter is switched off. Please contact Pulsiv for details as the supporting components will depend on specific power requirements.

5.8 State Machine of PSV-AD-xx

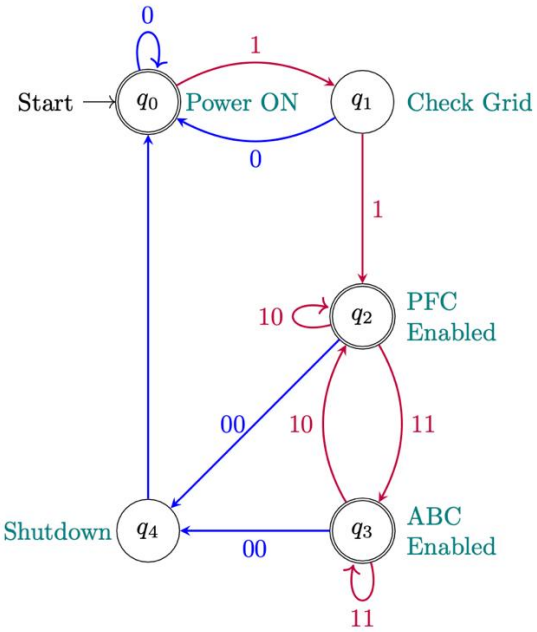
The controller provides all essential sequencing for safe operation of the PFC, active bridge, and hold-up circuits.

$$AD_{150FB} = (Q, \Sigma, \delta, q_0, F)$$

Where The states are Q = {q_0, q_1, q_2, q_3, q_4}. The states are defined by the following pins

Name	In/Out (Pin #)
V_GRID_OK	Digital out (7)
PFC_PWM	PWM out (8)
SECONDARY_PWM	PWM out (9)
GRID_60HZ_n50HZ	Digital out (14)
VRANGE_HI_nLO	Digital out (15)
TIMING_CHECK	Digital out (16)
TRIAC_ENABLE	Digital out (17)
ABC_POS	Digital out (21)
ABC_NEG	Digital out (22)
POWER_USED	Digital out (11)
ON_START	Digital out (12)

The PFC system is controlled by a finite state machine which is updated at a regular sampling rate of 2.4kHz. The state transitions are described by the diagram below.



q_0 is “Power ON” which sets the controller’s output pins to their resting, or inactive conditions. It also initialises various internal counter and timer values.

It then provides a short delay to ensure all hardware set-up conditions have completed before requesting the transition to state q_1. On entry it sets the following pins

V_GRID_OK	Low
PFC_PWM	Off
SECONDARY_PWM	Off
GRID_60HZ_n50HZ	Low
VRANGE_HI_nLO	Low
POWER_USED	Low
ABC_POS	Low
ABC_NEG	Low
TIMING_CHECK	Low
ON_START	**High**
TRIAC_ENABLE	Low

The controller stays in this state for 20 sample intervals, and only proceeds if the PFC_EN pin is high and a 20-sample time has elapsed.

State q_1 evaluates the incoming AC grid frequency. On entry it sets ON_START to low and TRIAC_INHIBIT_AL to high. If either a 50Hz or 60Hz grid is detected over a 2-grid cycle period, the relevant configuration data is selected and the transition to state q_2 is requested. The state sets the following pins

V_GRID_OK	Low
PFC_PWM	Off
SECONDARY_PWM	Off
GRID_60HZ_n50HZ	Low
VRANGE_HI_nLO	Low
POWER_USED	Low
ABC_POS	Low
ABC_NEG	Low
TIMING_CHECK	Low
ON_START	**Low**
TRIAC_ENABLE	Low

If no valid grid is detected the transition to q_0 is requested and the initialisation process is repeated.

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State q_2 activates the PFC control outputs, the grid condition output and indicated actual power consumption.

V_GRID_OK	**High**
PFC_PWM	**Operating**
SECONDARY_PWM	**Operating**
GRID_60HZ_n50HZ	**Operating**
VRANGE_HI_nLO	**Operating**
POWER_USED	**Operating**
ABC_POS	Low
ABC_NEG	Low
TIMING_CHECK	**High**
ON_START	Low
TRIAC_ENABLE	**High**

It then checks PFC_Enable input and the Active Bridge Control Error input.

If PFC is disabled, the transition to state q_4 is requested.

If PFC is enabled and no ABC error is indicated the transition to q_3 is requested.

Otherwise, no state transition is required, the state remains at q_2.

The PFC, grid condition and power consumption outputs are continually updated.

State q_3 sets the active bridge signals. The state is defined as

V_GRID_OK	High
PFC_PWM	Operating
SECONDARY_PWM	Operating
GRID_60HZ_n50HZ	Operating
VRANGE_HI_nLO	Operating
POWER_USED	Operating
ABC_POS	**Operating**
ABC_NEG	**Operating**
TIMING_CHECK	**Low**
ON_START	Low
TRIAC_ENABLE	High

If an ABC error is detected (the ABC Error input becomes active) the ABC outputs are deactivated and a state transition to q_2 is requested.

If PFC Enable becomes inactive a transition to q_4 is requested.

Otherwise, no state transition is required, and the state remains at q_3.

State q4 disables the PFC control outputs, power display and ABC outputs and attempts to maintain synchronisation with the input grid.

If the MODE input indicates that immediate restart is required, the transition to q_0 is requested.

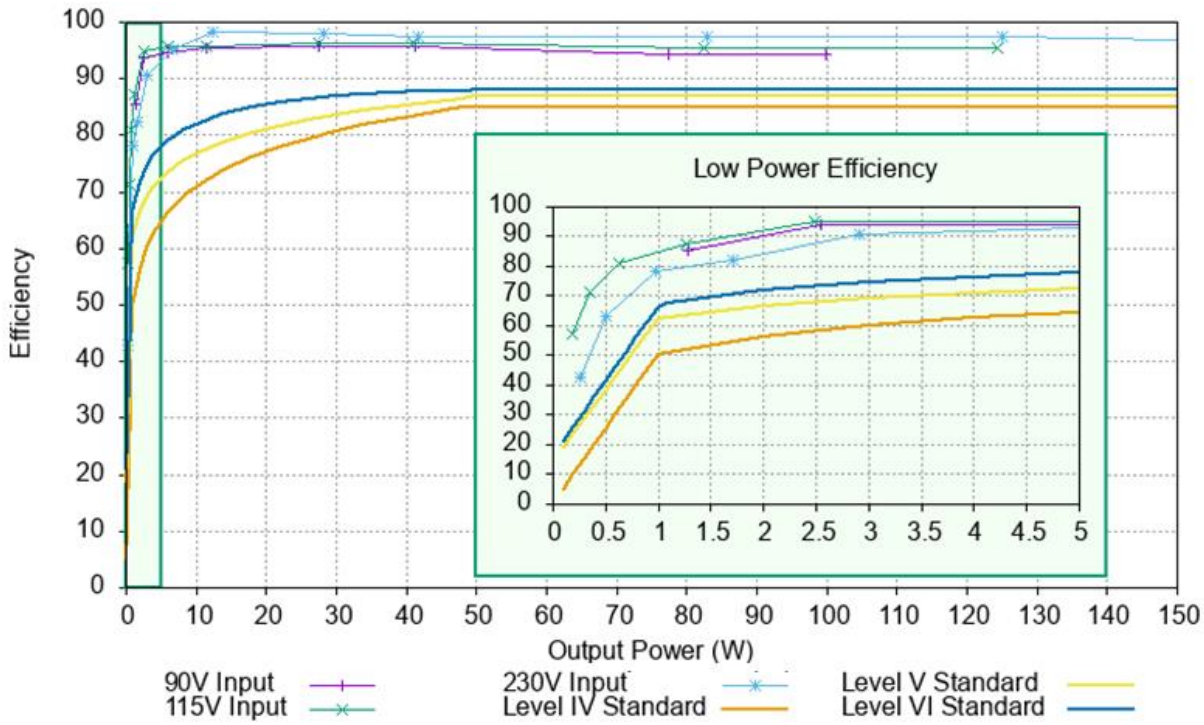
Otherwise, if the grid is no longer detectable, the ABC outputs are pulsed for 20uS to create a short circuit to discharge the X Capacitor and a transition to q_0 is requested.

If the grid is still detected the ABC outputs remain inactive and a short delay is introduced before transitioning to q_0.

6 SYSTEM PERFORMANCE DATA

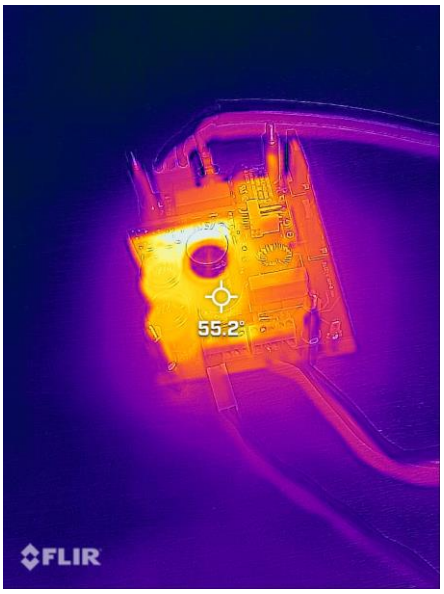
6.1 Efficiency

Measured on a PSV-AD-250-DS development system connected to a 150W flyback DC-DC converter with a 48V output.

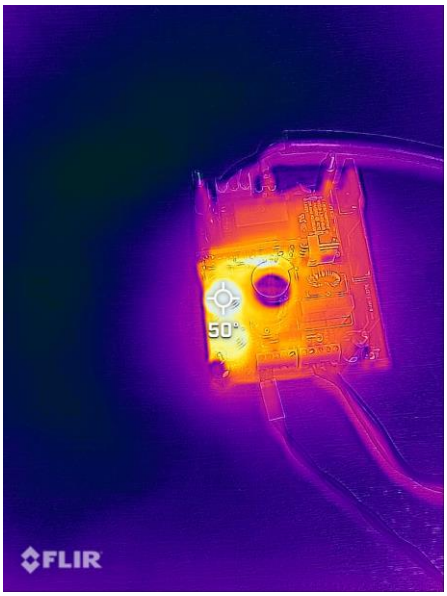


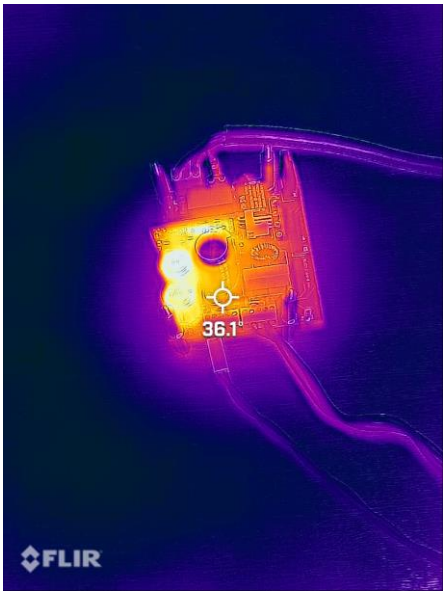
6.2 Thermal Performance

To showcase thermal performance, an image of the PSV-AD250-DS (with active bridge) is shown below for a Flyback load running at 113W with a 115V supply. The hot-spot at 76 Celsius is Q102; which has no heatsink or thermal vias. The calculated loss of Q102 is approximately 1W which has an expected thermal rise of 60 degrees. The capacitor temperature is 55 Celsius.



Running at 113W from a 230V supply, the capacitor temperatures are reduced from 55 Celsius to 36 Celsius and the MOSFET temperature is reduced from 76 Celsius to 50 Celsius. The losses move from the MOSFET to the bobbin chokes. By using lower Rdson MOSFETs or a customised choke, these losses can be reduced and efficiencies increased.





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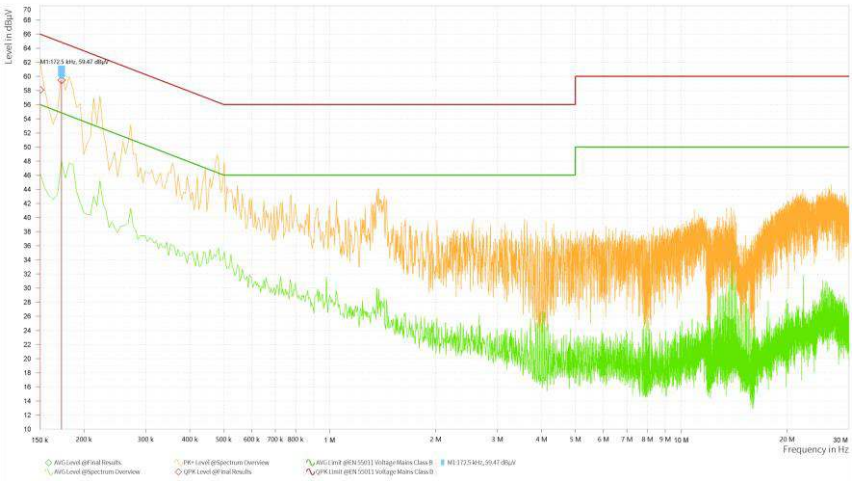
6.3 Conducted Emissions of the PSV-AD-250-DS Development System

CE_Mule_Rev2_PFC_1__based on EN 5011_13-5V_170W_electronic_load

Passed

ROHDE&SCHWARZ

EMI Test Report



EMI Final Results (1/2)

Rg	Frequency [MHz]	QPK Level [dBµV]	QPK Limit [dBµV]	QPK Margin [dB]	QPK Level [dBµV]	AVG Level [dBµV]	AVG Limit [dBµV]	AVG Margin [dB]	AVG Level [dBµV]	Correction [dB]	Line	Meas. BW [kHz]	Meas. Time [ms]	Time of Meas.
1	0.150	58.08	66.00	7.92						11.00	L1	9.000	2,000.000	11:06:19
1	0.173	59.47	64.84	5.37						11.00	L1	9.000	2,000.000	11:06:23

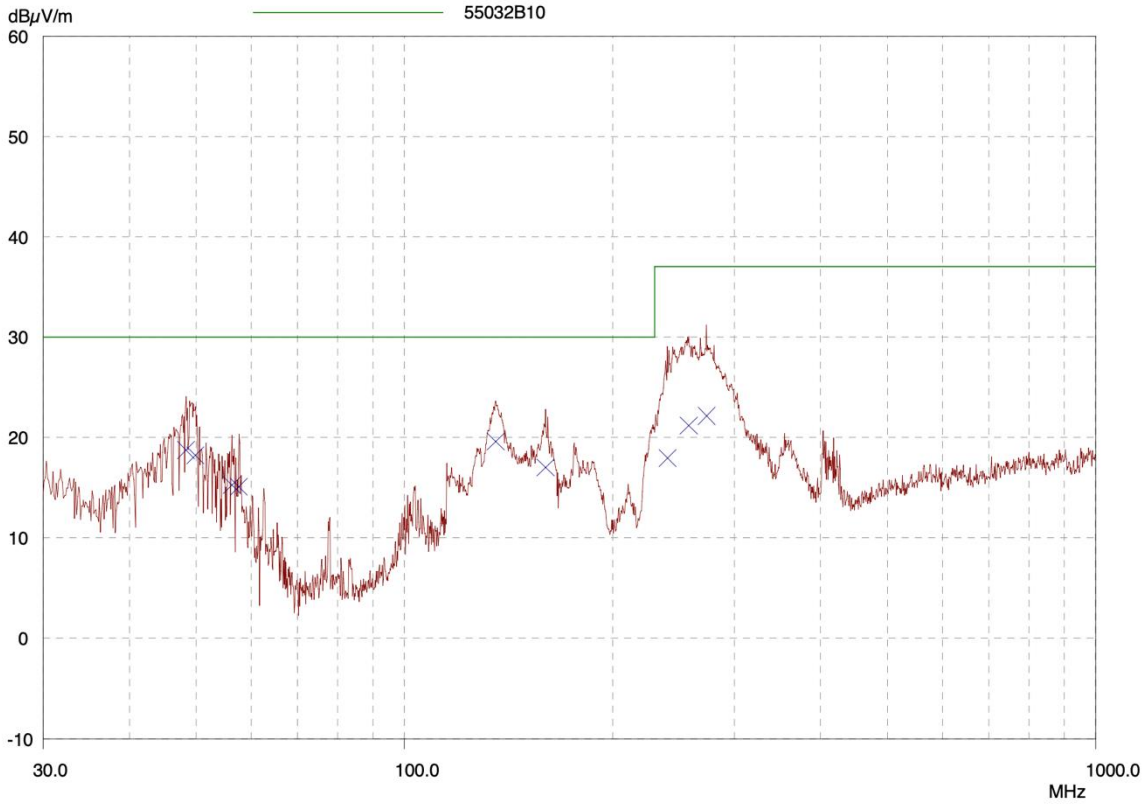
EMI Final Results (2/2)

Rg	Frequency [MHz]	Source
1	0.150	Critical Points
1	0.173	Critical Points

25/02/2022 / 11:07

1 / 1

6.4 Radiated Emissions of the PSV-AD-250-DS Development System



Scan Settings (1 Range)

Frequencies			Receiver Settings				
Start	Stop	Step	IF BW	Detector	M-Time	Atten	OpRge
30MHz	1000MHz	110kHz	120kHz	PK	20msec	Auto	60dB

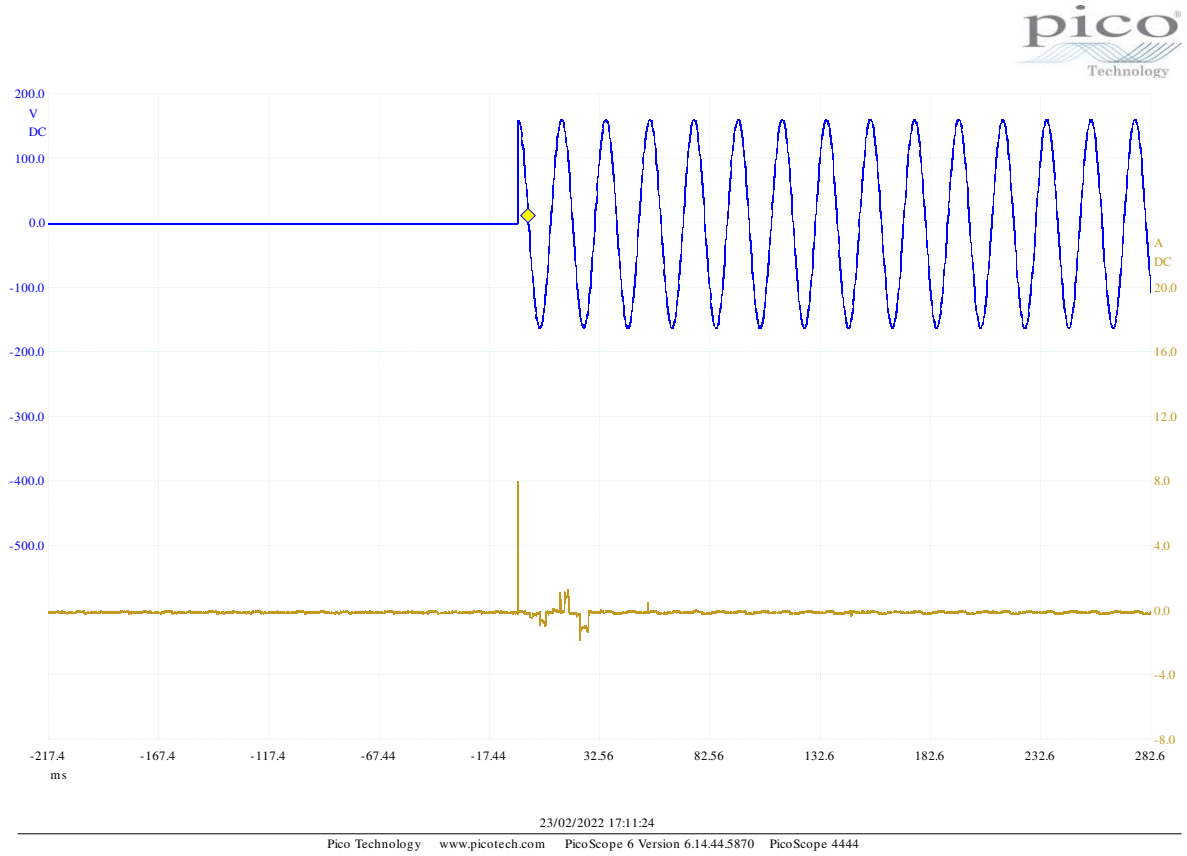
Transducer	No.	Start	Stop	Name
5	20	10MHz	1000MHz	CBLB046
	21	10MHz	1000MHz	B108AMP
	22	30MHz	1000MHz	B158_ANT

Final Measurement:		
	Detector:	X QP
	Meas Time:	2sec
	Subranges:	50
	Acc Margin:	25 dB

Final Measurement Results

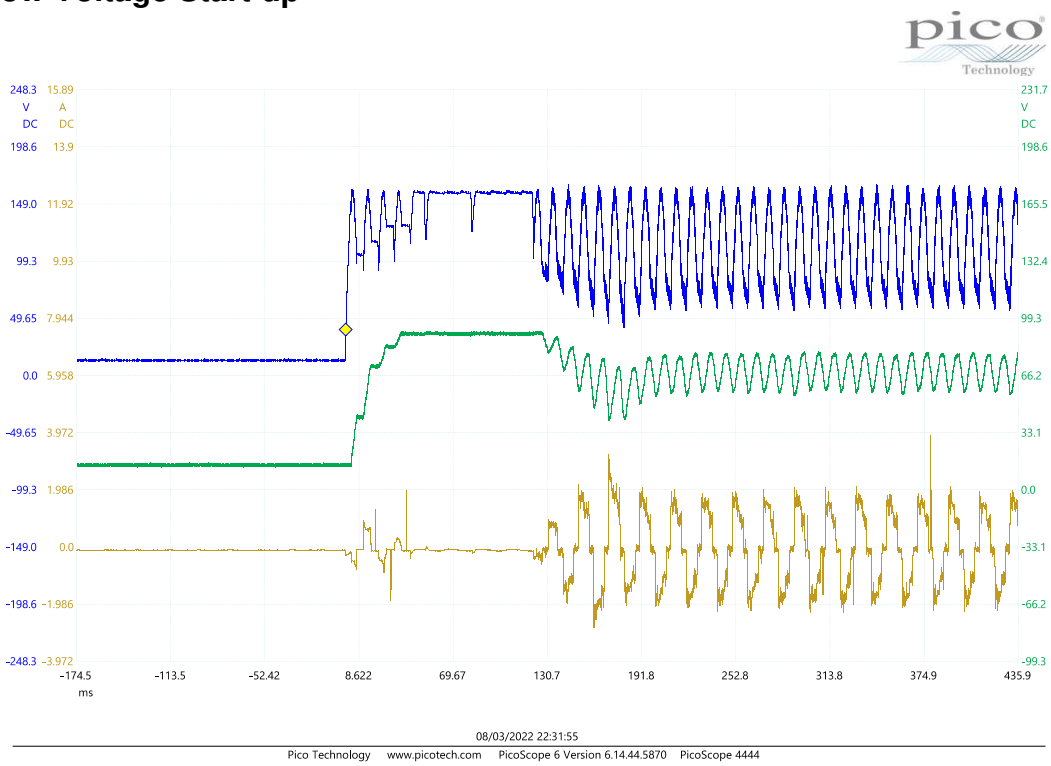
Frequency MHz	QP Level dBµV/m	QP Limit dBµV/m	QP Delta dB
273.32	22.14	37.00	14.86
257.48	21.18	37.00	15.82
135.27	19.60	30.00	10.40
48.26	18.74	30.00	11.26
49.8	18.23	30.00	11.77
239.99	17.97	37.00	19.03
160.02	17.00	30.00	13.00
56.18	15.27	30.00	14.73
57.61	15.11	30.00	14.89

6.5 No Inrush Current



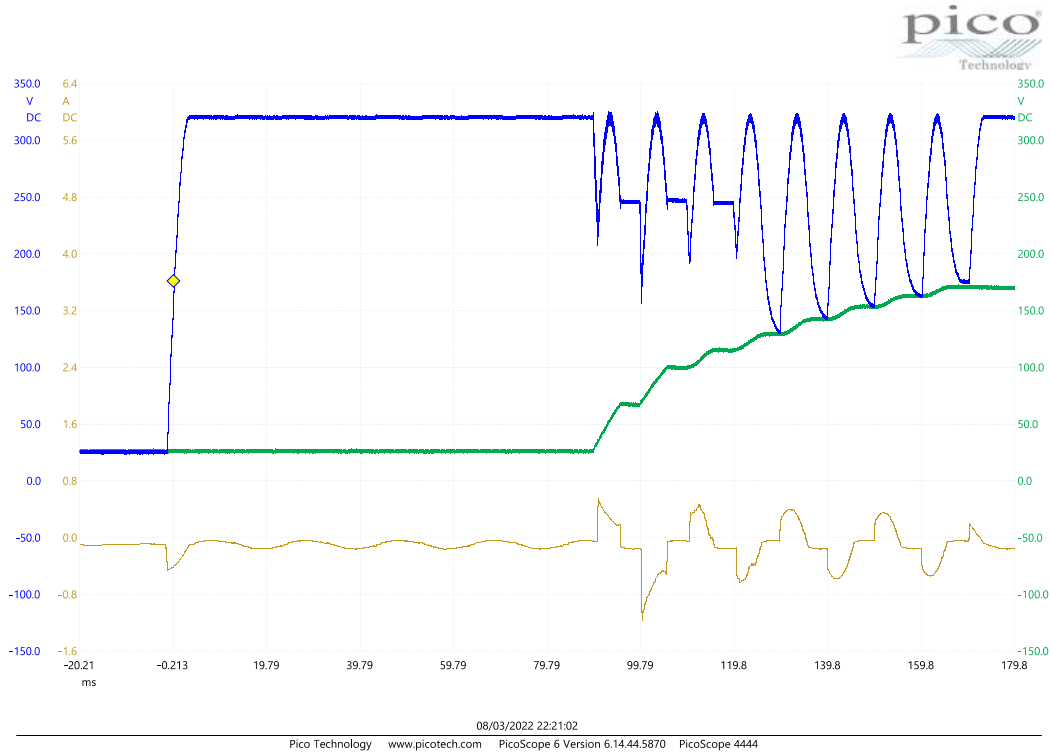
The small current spike shown here is caused by the X capacitor and voltage slew-rate of the test equipment. Accepted standards ignore below measurements below 100uS in duration, so the PSV-AD-xx system is considered to be free of inrush current.

6.6 Low Voltage Start-up



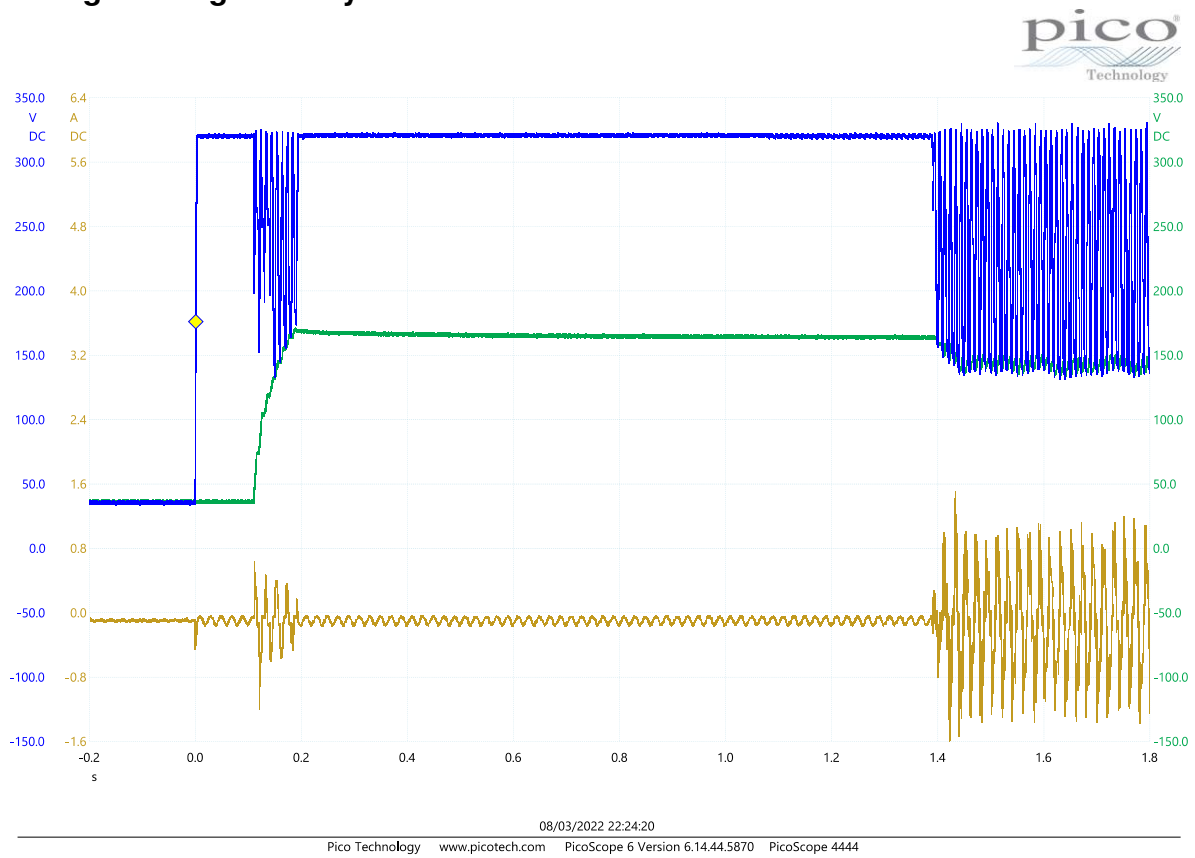
Blue is HVDC; Green is the potential difference on Cch and Brown is the line current

6.7 High Voltage Start-up



Blue is HVDC; Green is the potential difference on Cch and Brown is the line current

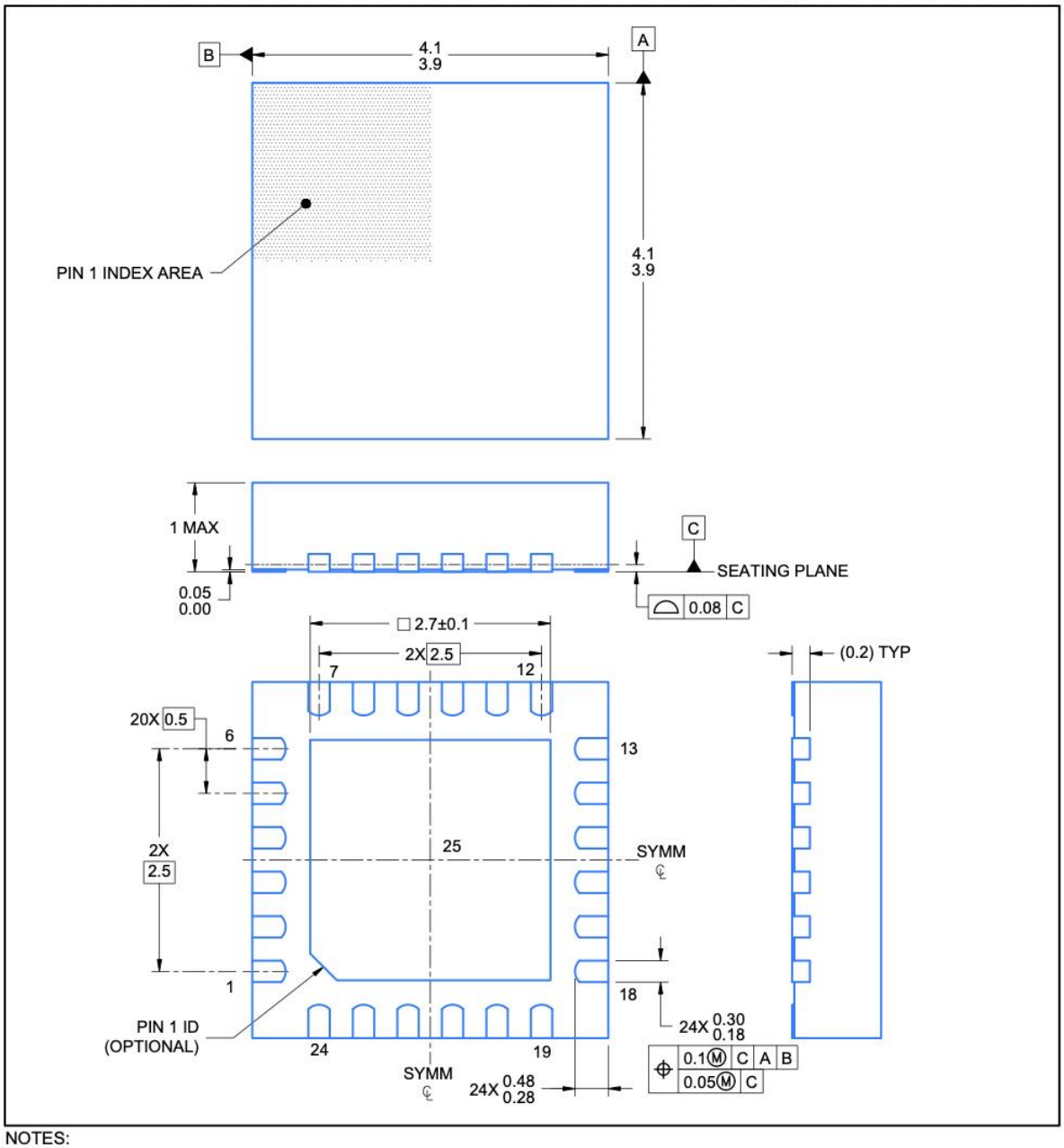
6.8 High Voltage Steady State



Blue is HVDC; Green is the potential difference on Cch and Brown is the line current

7 PACKAGE MECHANICAL DATA

PLASTIC QUAD FLATPACK- NO LEAD

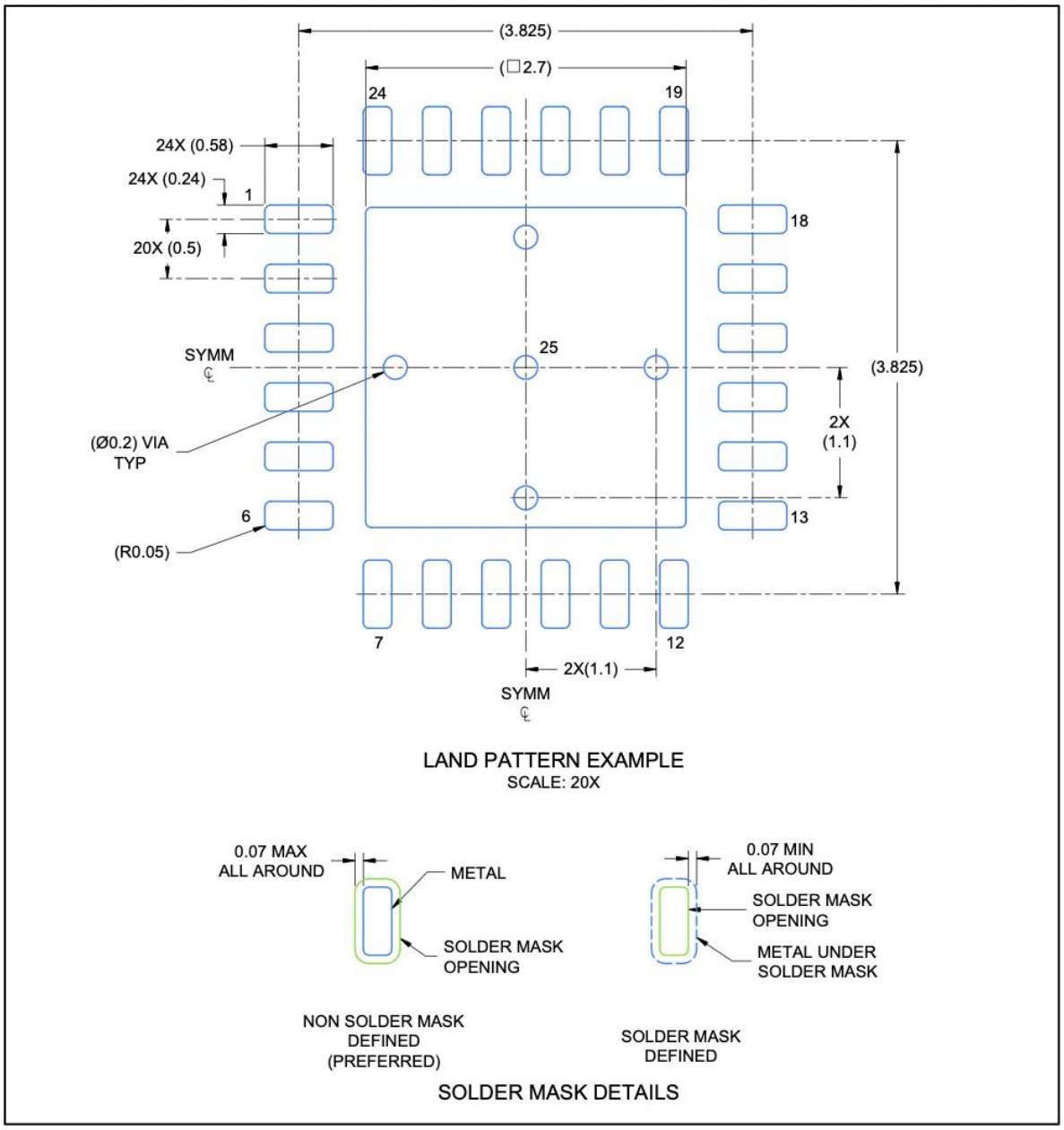


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

7.1 Recommended PCB Footprint

PLASTIC QUAD FLATPACK- NO LEAD



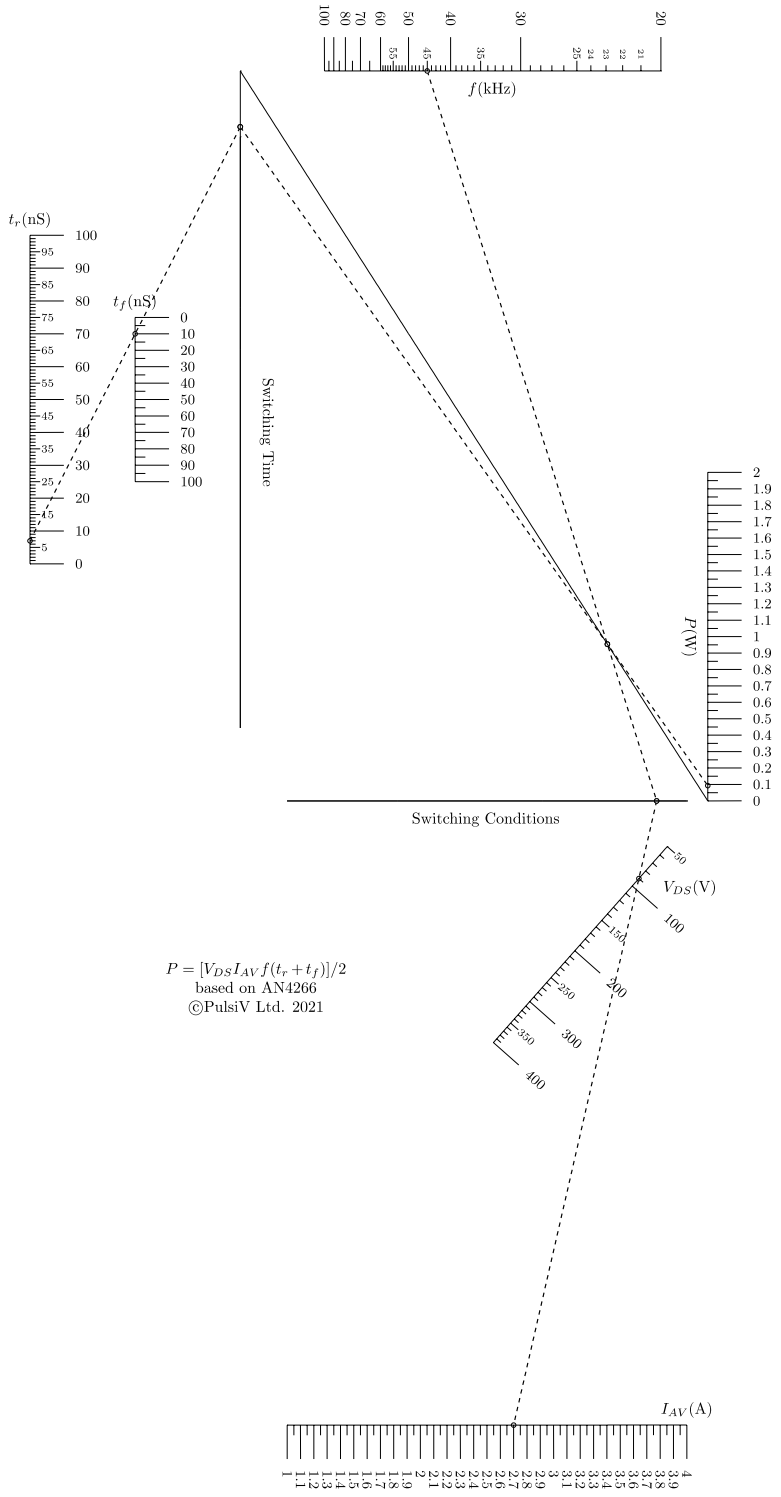
NOTES: (continued)

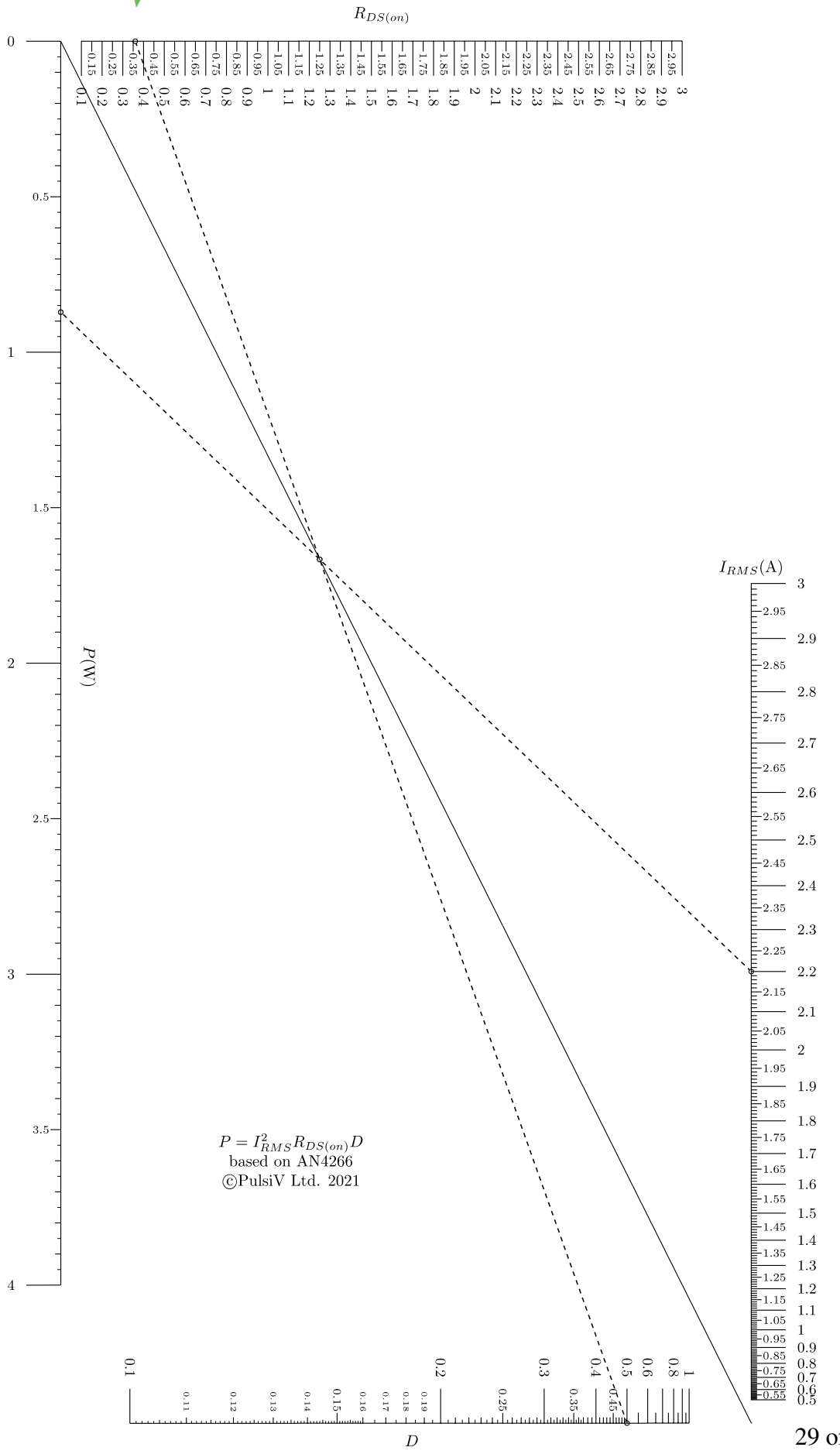
4. This package is designed to be soldered to a thermal pad on the board.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

APPENDIX A

Appendix A.1 MOSFET Selection Nomograms

This example shows the losses for MOSFET IPN60R360P7SATMA1.





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