Freescale Semiconductor
Technical Data

Document Number: MRFE6S9046N
Rev. 0, 5/2009

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRFE6S9046NR1
MRFE6S9046GNR1

920-960 MHz, 35.5 W CW, 28 V
GSM, GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

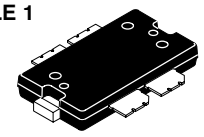
Designed for GSM and GSM EDGE base station applications with frequencies from 920 to 960 MHz. Suitable for CDMA and multicarrier amplifier applications.

- Typical GSM Performance: V_{DD} = 28 Volts, I_{DQ} = 300 mA, P_{out} = 35.5 Watts CW, f = 960 MHz
  - Power Gain — 19 dB
  - Drain Efficiency — 57%
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 940 MHz, 70 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point ≃ 45 Watts CW
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ} = 285 mA, P_{out} = 17.8 Watts Avg., Full Frequency Band (920-960 MHz)
  - Power Gain — 19 dB
  - Drain Efficiency — 42.5%
  - Spectral Regrowth @ 400 kHz Offset = -62.5 dBc
  - Spectral Regrowth @ 600 kHz Offset = -72 dBc
  - EVM — 2.1% rms

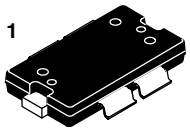
Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

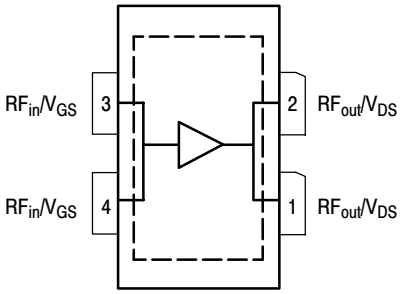
CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRFE6S9046NR1



CASE 1487-05, STYLE 1
TO-270 WB-4 GULL
PLASTIC
MRFE6S9046GNR1



PARTS ARE SINGLE-ENDED



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 45 W CW, 28 Vdc, I_{DQ} = 300 mA Case Temperature 80°C, 18 W CW, 28 Vdc, I_{DQ} = 300 mA	$R_{\theta JC}$	 1.3 1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 66 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	1	2.2	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 300 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	3.1	4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.1	0.3	0.4	Vdc
Dynamic Characteristics (3)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.6	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	318	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	120	—	pF

Functional Tests (4) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 35.5 W CW, I_{DQ} = 300 mA, f = 960 MHz

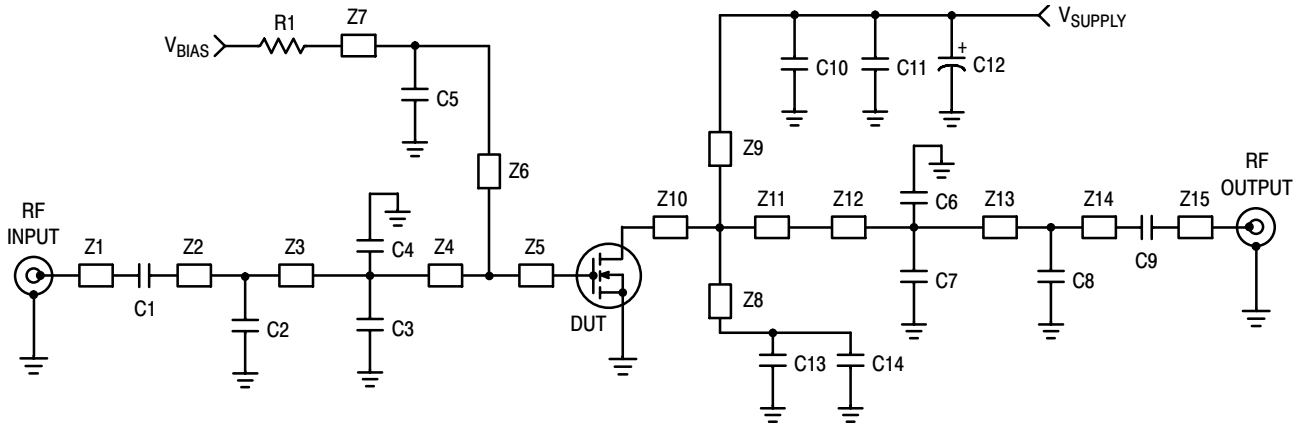
Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	17.5	19	—	dB
Drain Efficiency	η_D	54	57	—	%
Input Return Loss	IRL	—	-13	-7	dB

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
3. Part internally matched both on input and output.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale GSM EDGE Reference Design Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 300 mA, 920-960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point	P1dB	—	45	—	W
IMD Symmetry @ 44 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	55	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	65	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 35.5 W CW	G_F	—	0.2	—	dB
Average Deviation from Linear Phase in 40 MHz Bandwidth @ P_{out} = 45 W CW	Φ	—	0.9	—	°
Average Group Delay @ P_{out} = 45 W CW, f = 940 MHz	Delay	—	3.1	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 45 W CW, f = 940 MHz, Six Sigma Window	$\Delta\Phi$	—	20	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.021	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.006	—	dBm/°C
Typical GSM EDGE Performances (In Freescale GSM EDGE Reference Design Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 285 mA, P_{out} = 17.8 W Avg., 920-960 MHz EDGE Modulation					
Power Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	42.5	—	%
Error Vector Magnitude	EVM	—	2.1	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-62.5	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-72	—	dBc



Z1	0.200″ x 0.044″ Microstrip	Z10	0.040″ x 0.450″ Microstrip
Z2	0.196″ x 0.044″ Microstrip	Z11	0.321″ x 0.450″ Microstrip
Z3	0.380″ x 0.044″ Microstrip	Z12	0.080″ x 0.280″ Microstrip
Z4	0.321″ x 0.450″ Microstrip	Z13	0.372″ x 0.044″ Microstrip
Z5	0.039″ x 0.450″ Microstrip	Z14	0.124″ x 0.044″ Microstrip
Z6*	0.281″ x 0.040″ Microstrip	Z15	0.200″ x 0.044″ Microstrip
Z7	0.892″ x 0.051″ Microstrip	PCB	Rogers R04350, 0.020″, ε_r = 3.66
Z8* Z9*	0.751″ x 0.040″ Microstrip		

* Line length includes microstrip bends

Figure 2. MRFE6S9046NR1(GNR1) Test Circuit Schematic — GSM EDGE Reference Design

Table 6. MRFE6S9046NR1(GNR1) Test Circuit Component Designations and Values — GSM EDGE Reference Design

Part	Description	Part Number	Manufacturer
C1, C9	56 pF Chip Capacitors	ATC600F560BT500XT	ATC
C2	2.4 pF Chip Capacitor	ATC600F2R4BT500XT	ATC
C3, C4	6.8 pF Chip Capacitors	ATC600F6R8BT500XT	ATC
C5, C11, C14	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C6, C7	3.3 pF Chip Capacitors	ATC600F3R3BT500XT	ATC
C8	4.7 pF Chip Capacitor	ATC600F4R7BT500XT	ATC
C10, C13	39 pF Chip Capacitors	ATC600F390BT500XT	ATC
C12	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	4.7 KΩ, 1/4 W Chip Resistor	CRCW12064701FKEA	Vishay

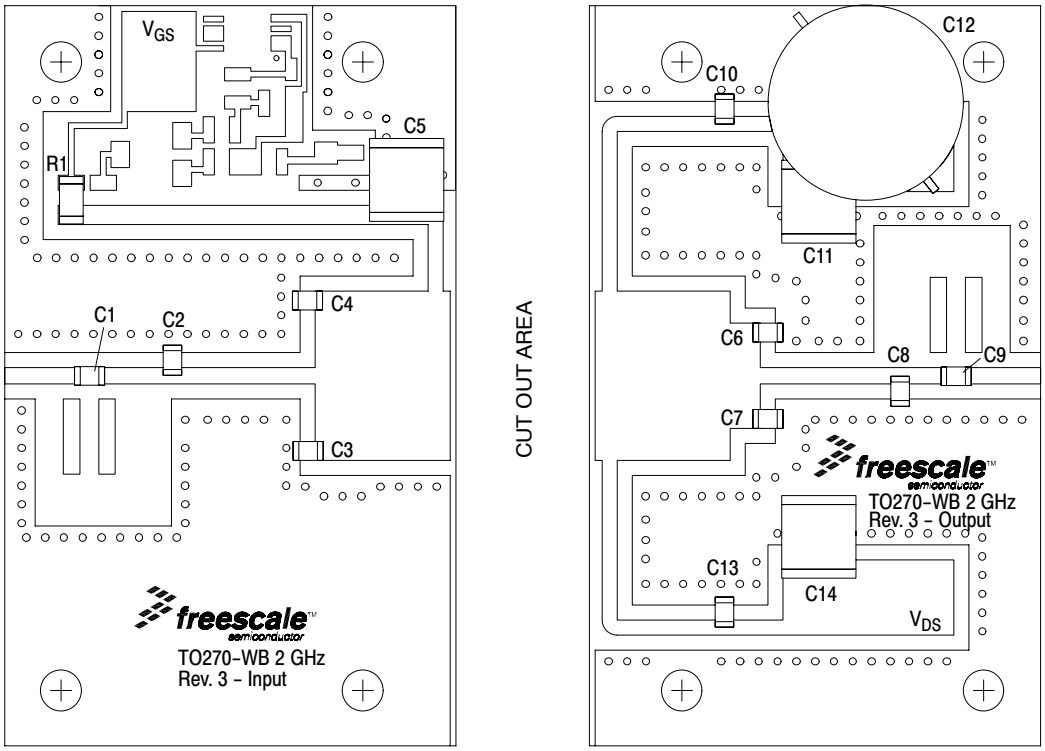


Figure 3. MRFE6S9046NR1(GNR1) Test Circuit Component Layout — GSM EDGE Reference Design

TYPICAL CHARACTERISTICS

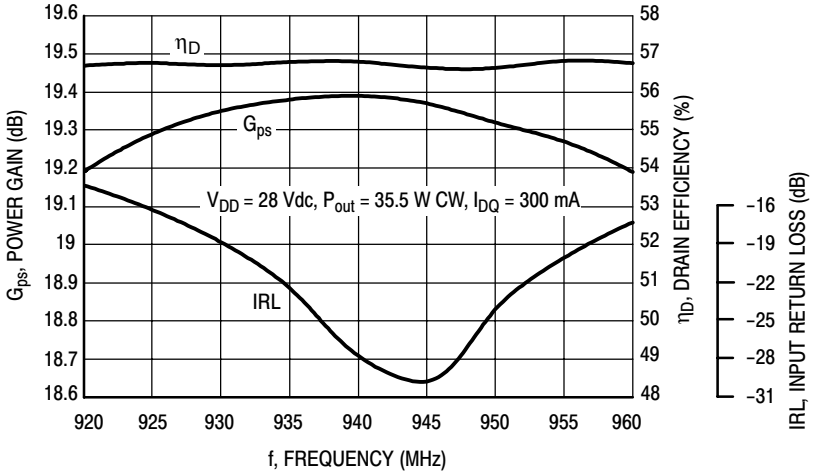


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P_{out} = 35.5 Watts CW

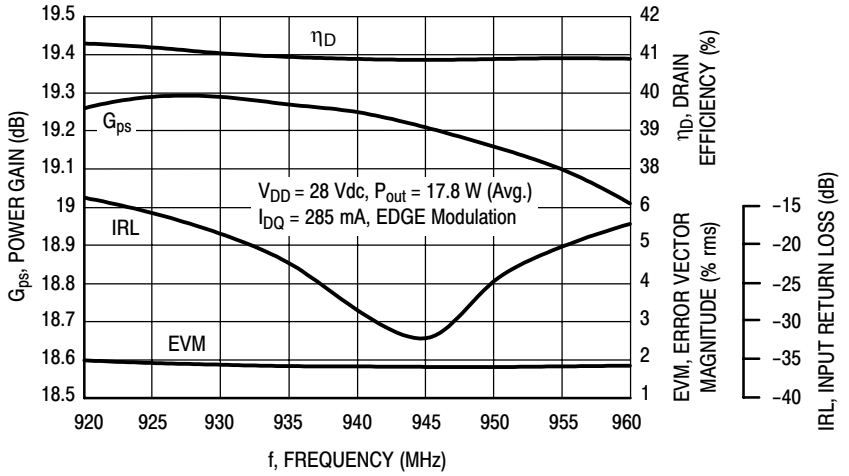


Figure 5. Power Gain, Input Return Loss, EVM and Drain Efficiency versus Frequency @ P_{out} = 17.8 Watts Avg.

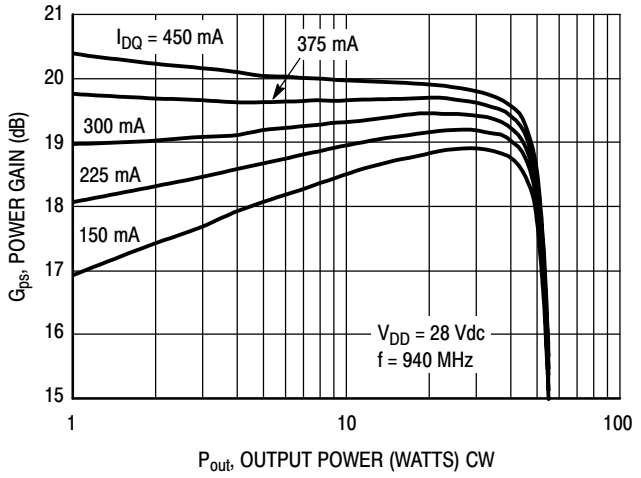


Figure 6. Power Gain versus Output Power

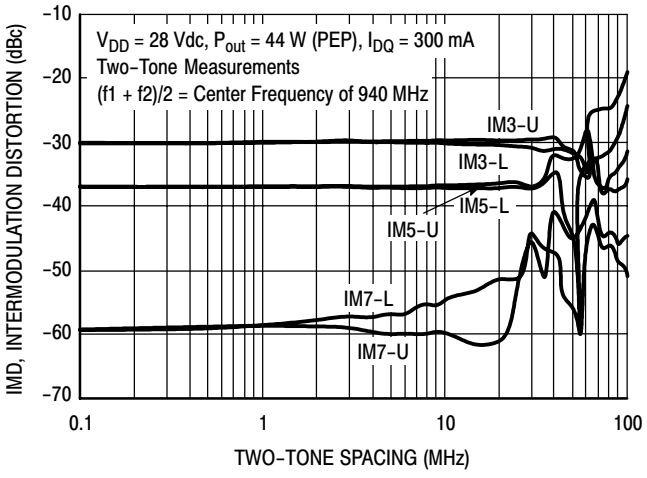


Figure 7. Intermodulation Distortion Products versus Two-Tone Spacing

TYPICAL CHARACTERISTICS

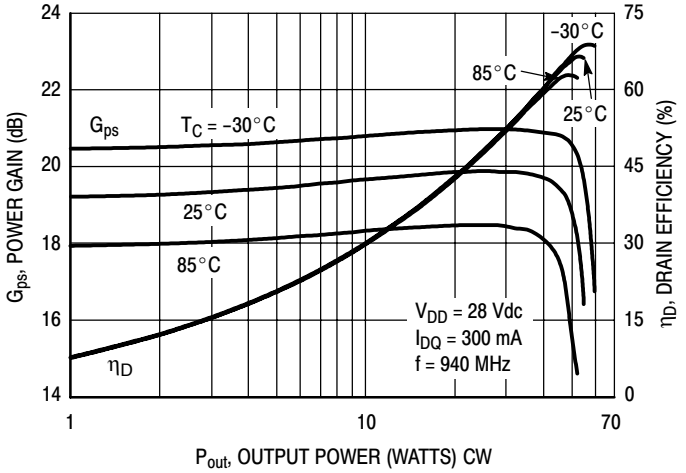


Figure 8. Power Gain and Drain Efficiency versus Output Power

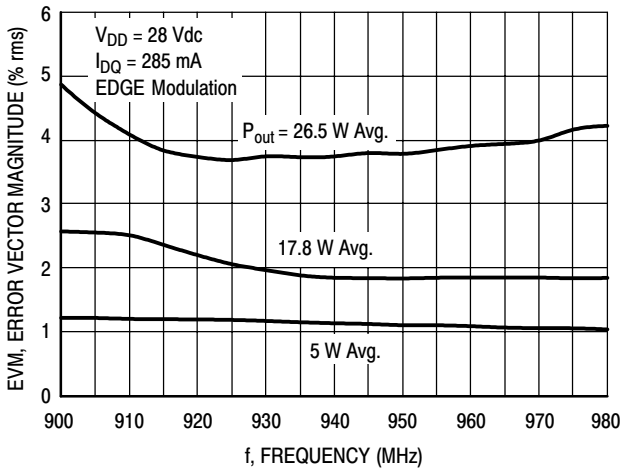


Figure 9. EVM versus Frequency

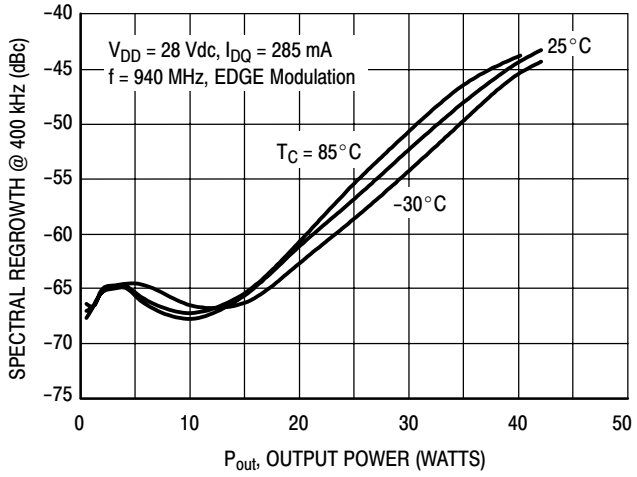


Figure 10. Spectral Regrowth at 400 kHz versus Output Power

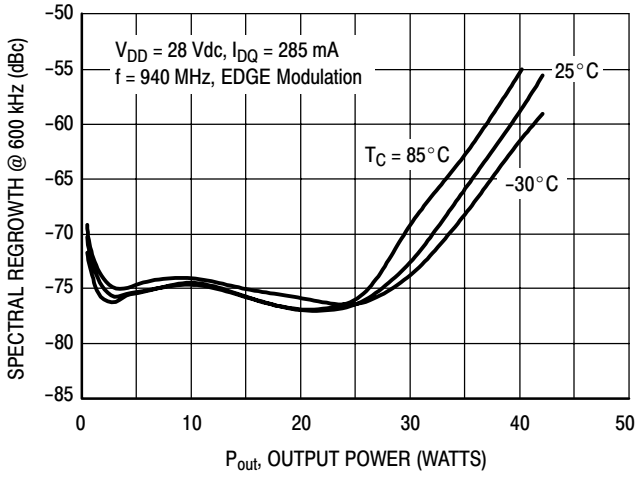


Figure 11. Spectral Regrowth at 600 kHz versus Output Power

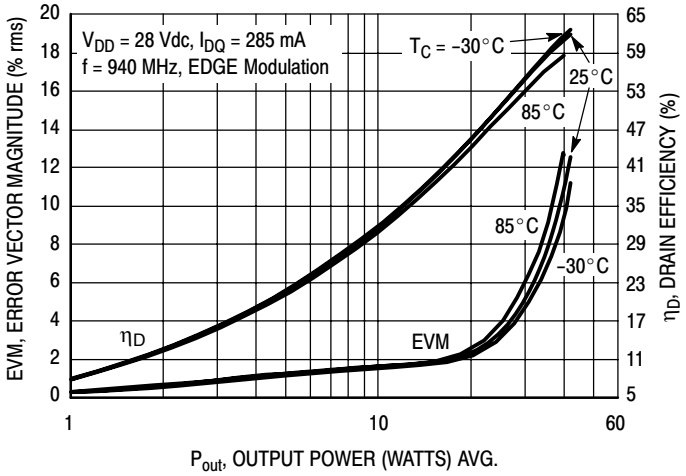


Figure 12. EVM and Drain Efficiency versus Output Power

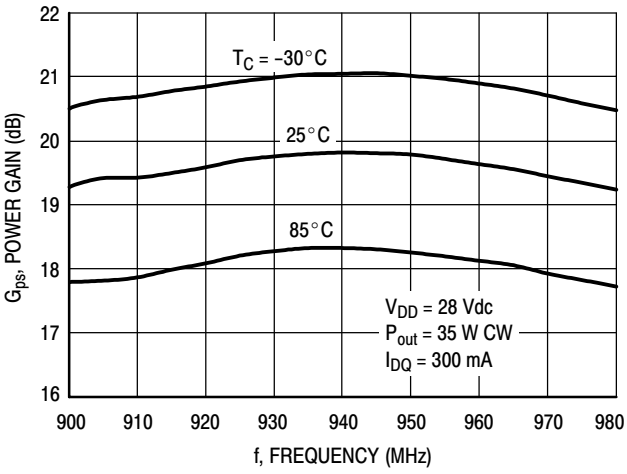


Figure 13. Power Gain versus Frequency

TYPICAL CHARACTERISTICS

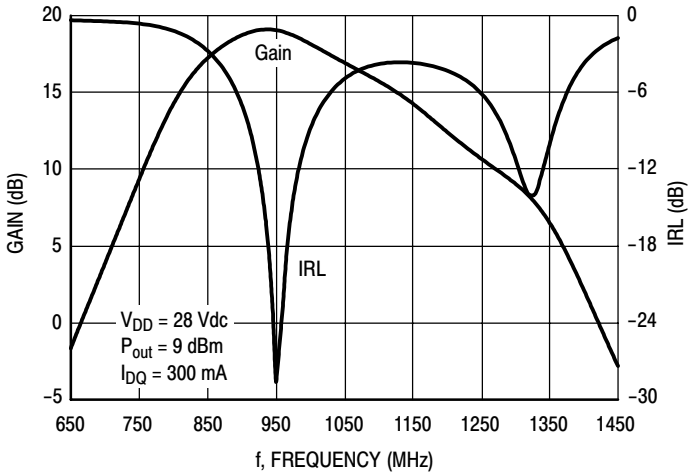
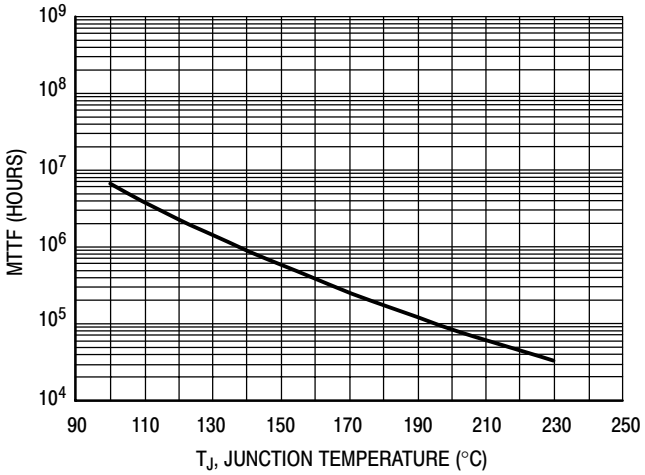


Figure 14. Broadband Frequency Response



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 35.5 W CW, and η_D = 57%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 15. MTTF versus Junction Temperature

GSM TEST SIGNAL

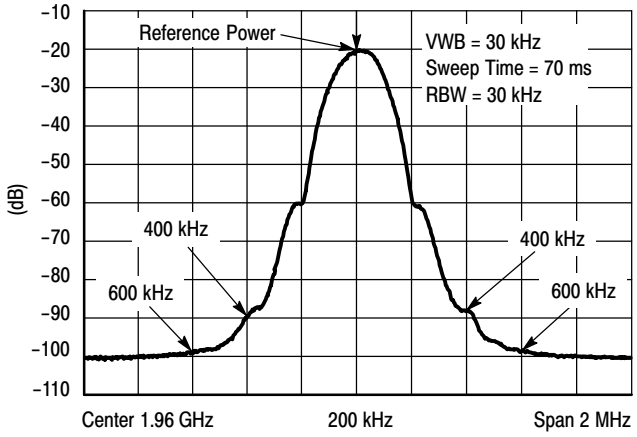
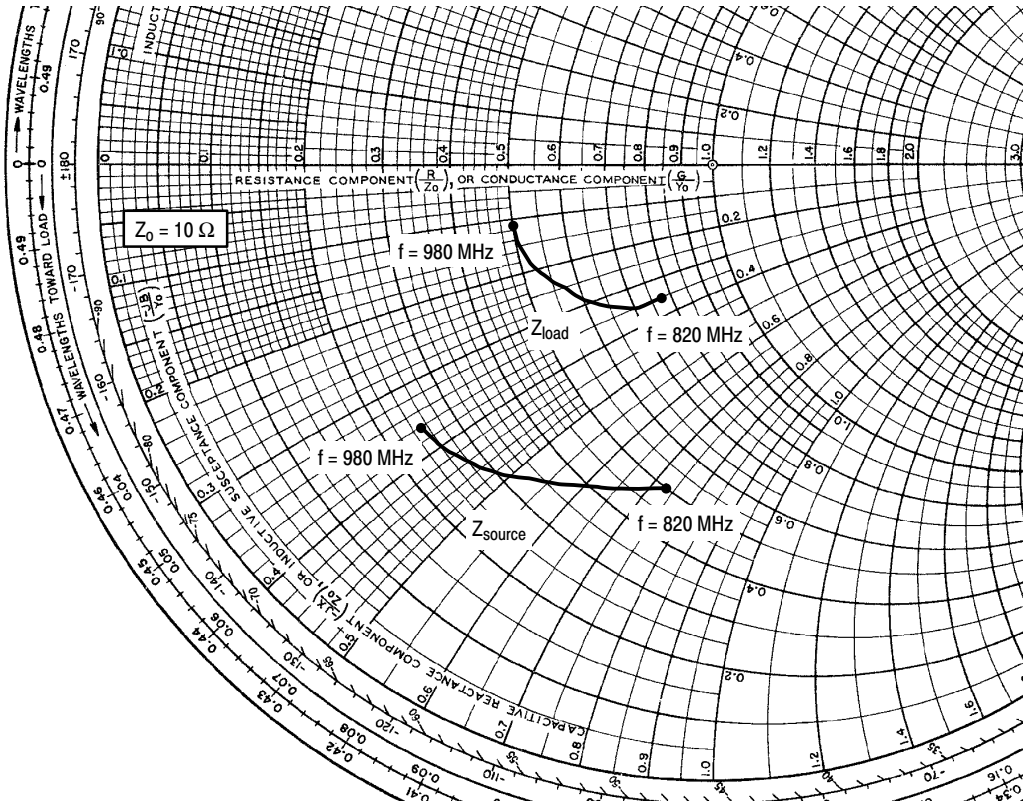


Figure 16. EDGE Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 285 mA, P_{out} = 17.8 W Avg.

f (MHz)	Z_{source} Ω	Z_{load} Ω
820	5.03 - j7.29	7.68 - j3.45
840	4.46 - j6.69	6.97 - j3.53
860	4.00 - j6.11	6.42 - j3.20
880	3.62 - j5.64	5.98 - j2.87
900	3.29 - j5.18	5.65 - j2.52
920	3.03 - j4.75	5.40 - j2.17
940	2.80 - j4.36	5.21 - j1.82
960	2.61 - j3.99	5.09 - j1.47
980	2.46 - j3.64	5.03 - j1.12

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

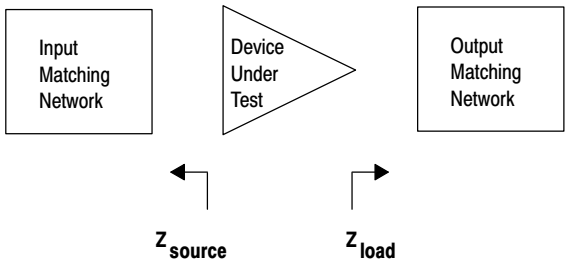
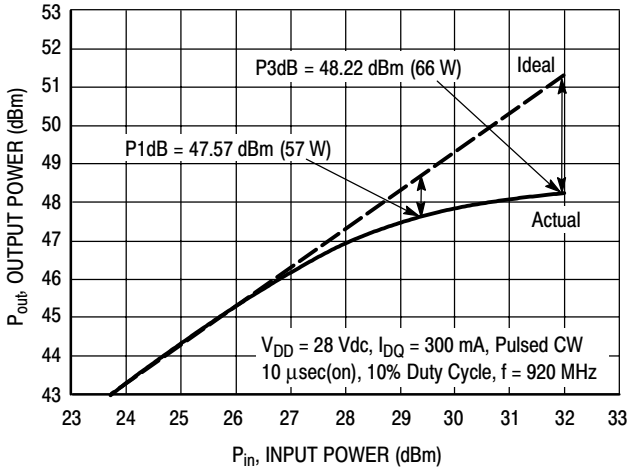


Figure 17. Series Equivalent Source and Load Impedance — GSM EDGE Reference Design

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

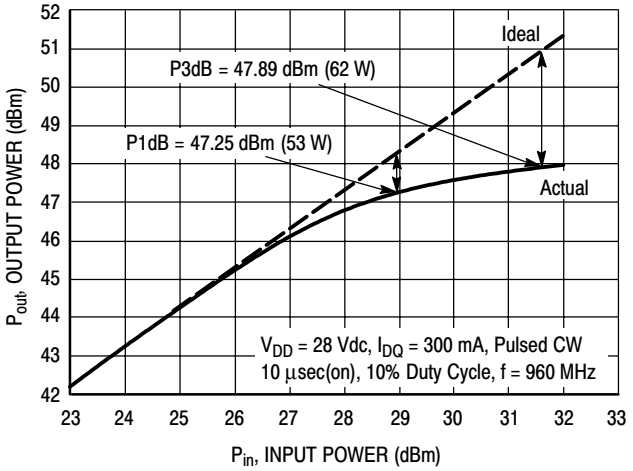


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	7.83 - j2.01	1.25 - j0.52

Figure 18. Pulsed CW Output Power versus Input Power @ 28 V @ 920 MHz

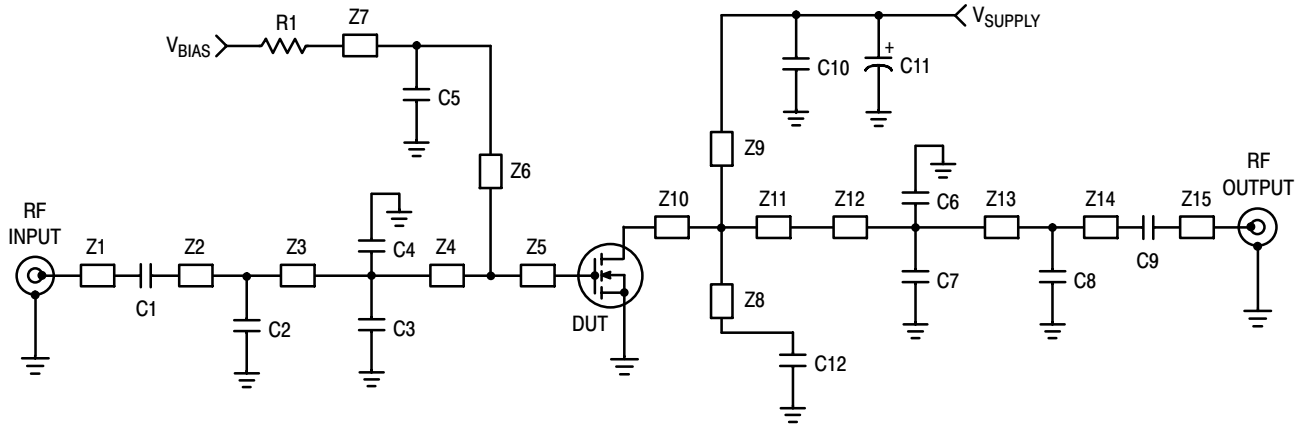


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	3.79 - j6.51	4.30 - j2.52

Figure 19. Pulsed CW Output Power versus Input Power @ 28 V @ 960 MHz



Z1	1.320″ x 0.044″ Microstrip	Z10	0.040″ x 0.450″ Microstrip
Z2	0.020″ x 0.044″ Microstrip	Z11	0.321″ x 0.450″ Microstrip
Z3	0.378″ x 0.044″ Microstrip	Z12	0.080″ x 0.280″ Microstrip
Z4	0.321″ x 0.450″ Microstrip	Z13	0.371″ x 0.044″ Microstrip
Z5	0.039″ x 0.450″ Microstrip	Z14	0.124″ x 0.044″ Microstrip
Z6*	0.306″ x 0.040″ Microstrip	Z15	1.332″ x 0.044″ Microstrip
Z7	0.708″ x 0.051″ Microstrip	PCB	Rogers R04350, 0.020″, ε_r = 3.66
Z8*, Z9*	0.738″ x 0.040″ Microstrip		

* Line length includes microstrip bends

Figure 20. MRFE6S9046NR1(GNR1) Test Circuit Schematic — Production Test Fixture

Table 7. MRFE6S9046NR1(GNR1) Test Circuit Component Designations and Values — Production Test Fixture

Part	Description	Part Number	Manufacturer
C1, C9	56 pF Chip Capacitors	ATC600F560BT500XT	ATC
C2	3.9 pF Chip Capacitor	ATC600F2R4BT500XT	ATC
C3, C4	6.8 pF Chip Capacitors	ATC600F6R8BT500XT	ATC
C5	0.01 μF Chip Capacitor	C1825C103K1GAC	Kemet
C6, C7	3.3 pF Chip Capacitors	ATC600F3R3BT500XT	ATC
C8	5.1 pF Chip Capacitor	ATC600F4R7BT500XT	ATC
C10, C12	39 pF Chip Capacitors	ATC600F390BT500XT	ATC
C11	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	4.7 KΩ, 1/4 W Chip Resistor	CRCW12064K70FKEA	Vishay

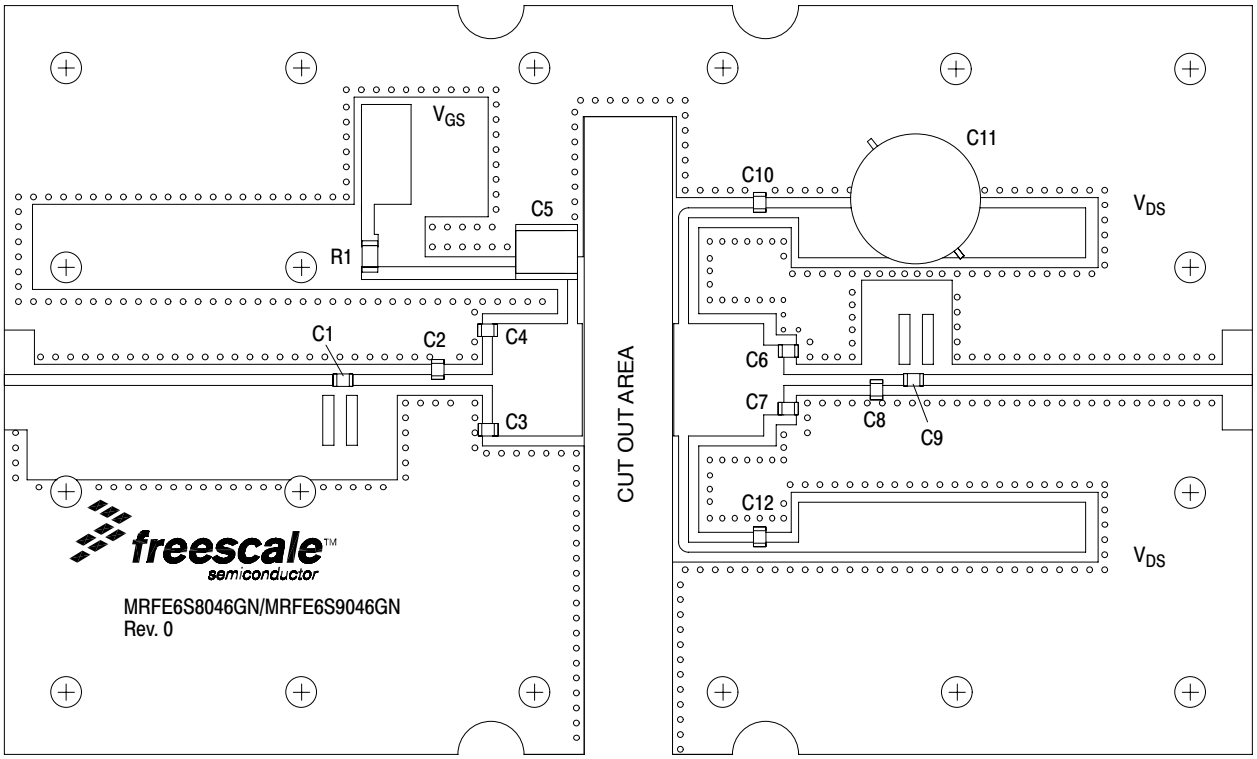
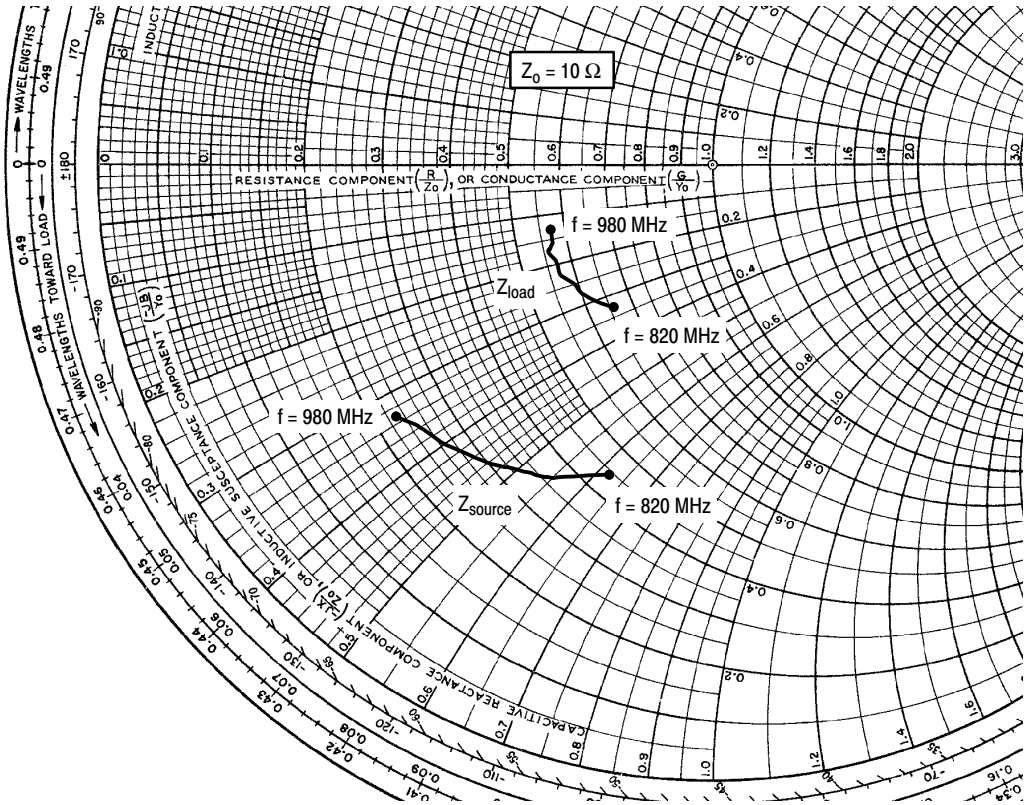


Figure 21. MRFE6S9046NR1(GNR1) Test Circuit Component Layout — Production Test Fixture



V_{DD} = 28 Vdc, I_{DQ} = 300 mA, P_{out} = 35.5 W CW

f (MHz)	Z_{source} Ω	Z_{load} Ω
820	4.37 - j6.23	6.55 - j3.27
840	3.95 - j5.76	6.26 - j2.98
860	3.60 - j5.53	6.02 - j2.72
880	3.29 - j4.95	5.86 - j2.48
900	3.04 - j4.59	5.74 - j2.24
920	2.83 - j4.24	5.68 - j1.98
940	2.63 - j3.92	5.64 - j1.74
960	2.45 - j3.62	5.65 - j1.49
980	2.31 - j3.33	5.70 - j1.26

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

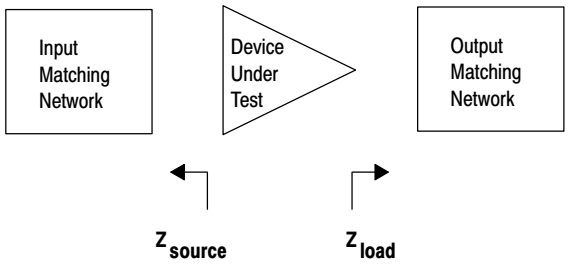
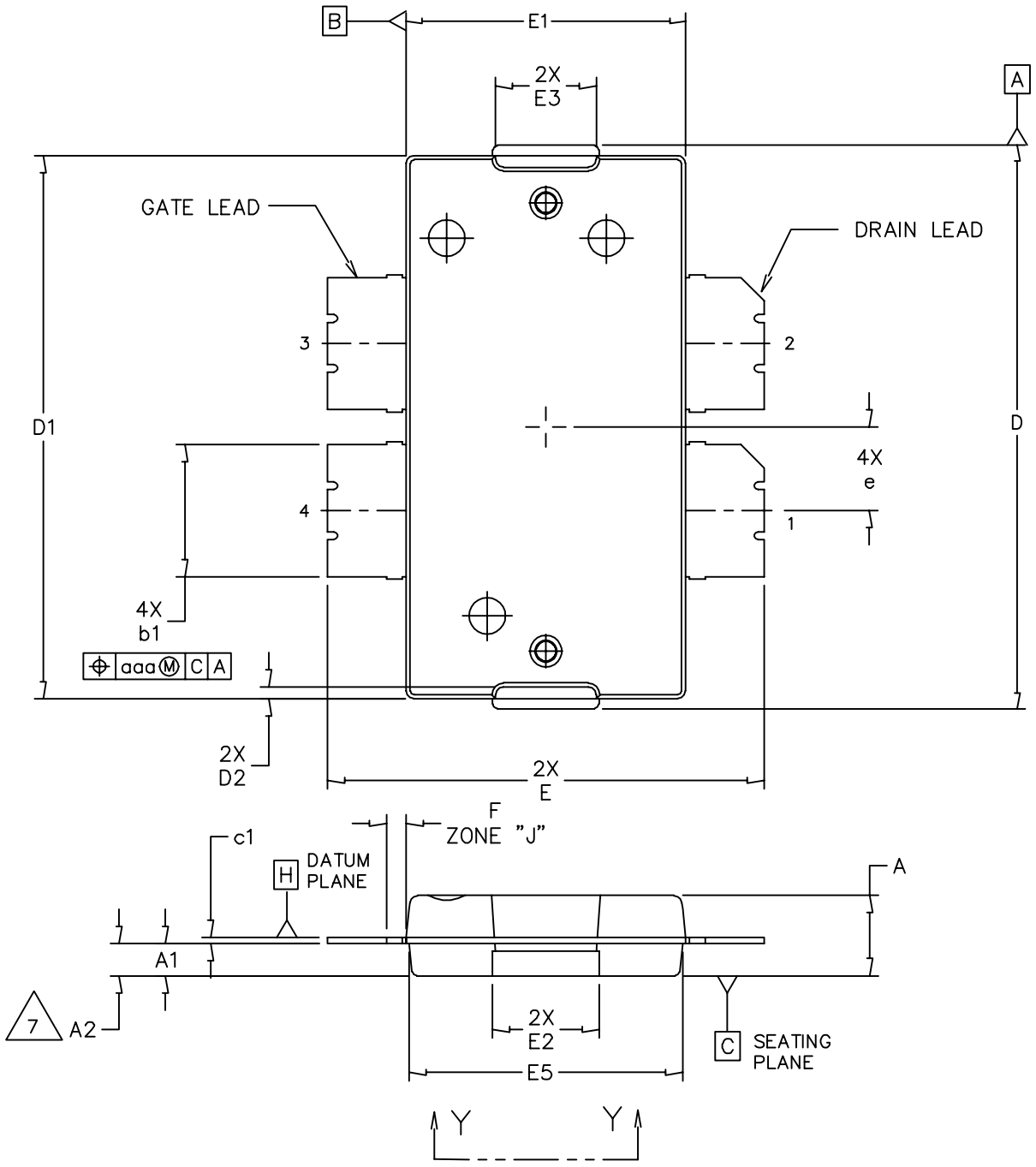


Figure 22. Series Equivalent Source and Load Impedance — Production Test Fixture

PACKAGE DIMENSIONS



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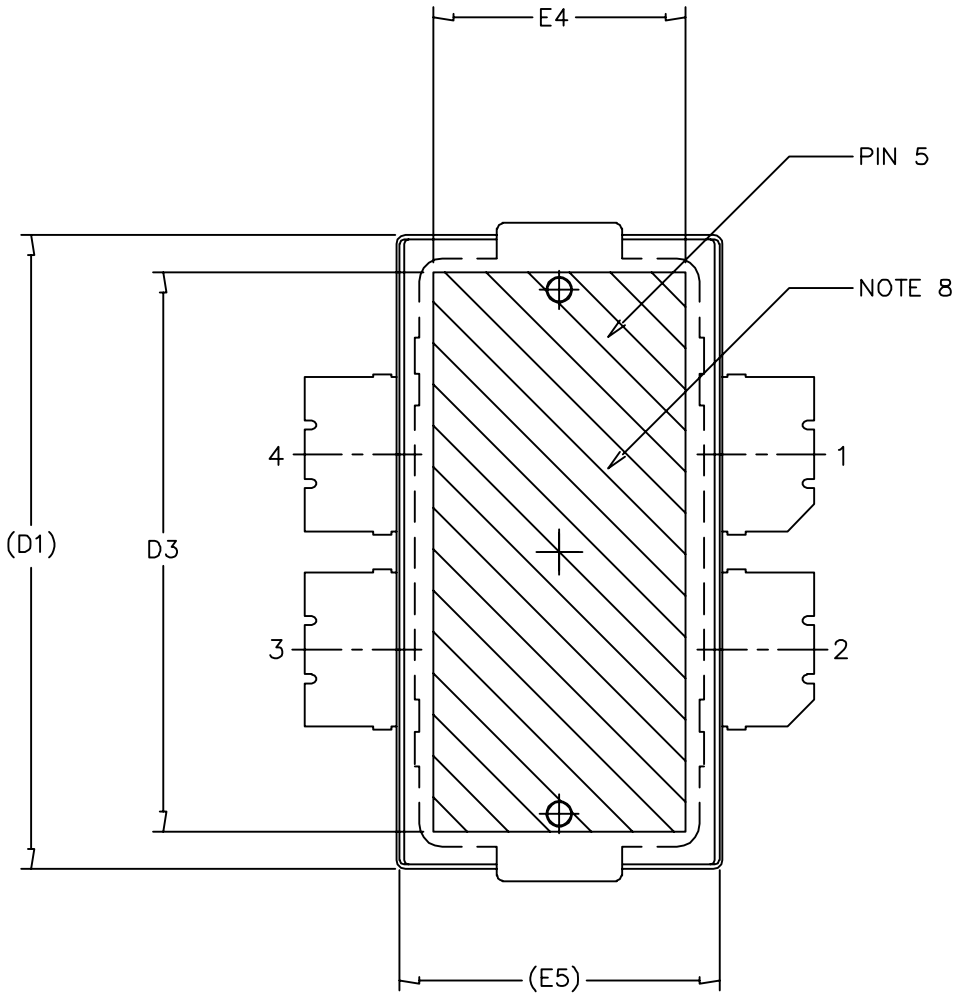
	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	



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	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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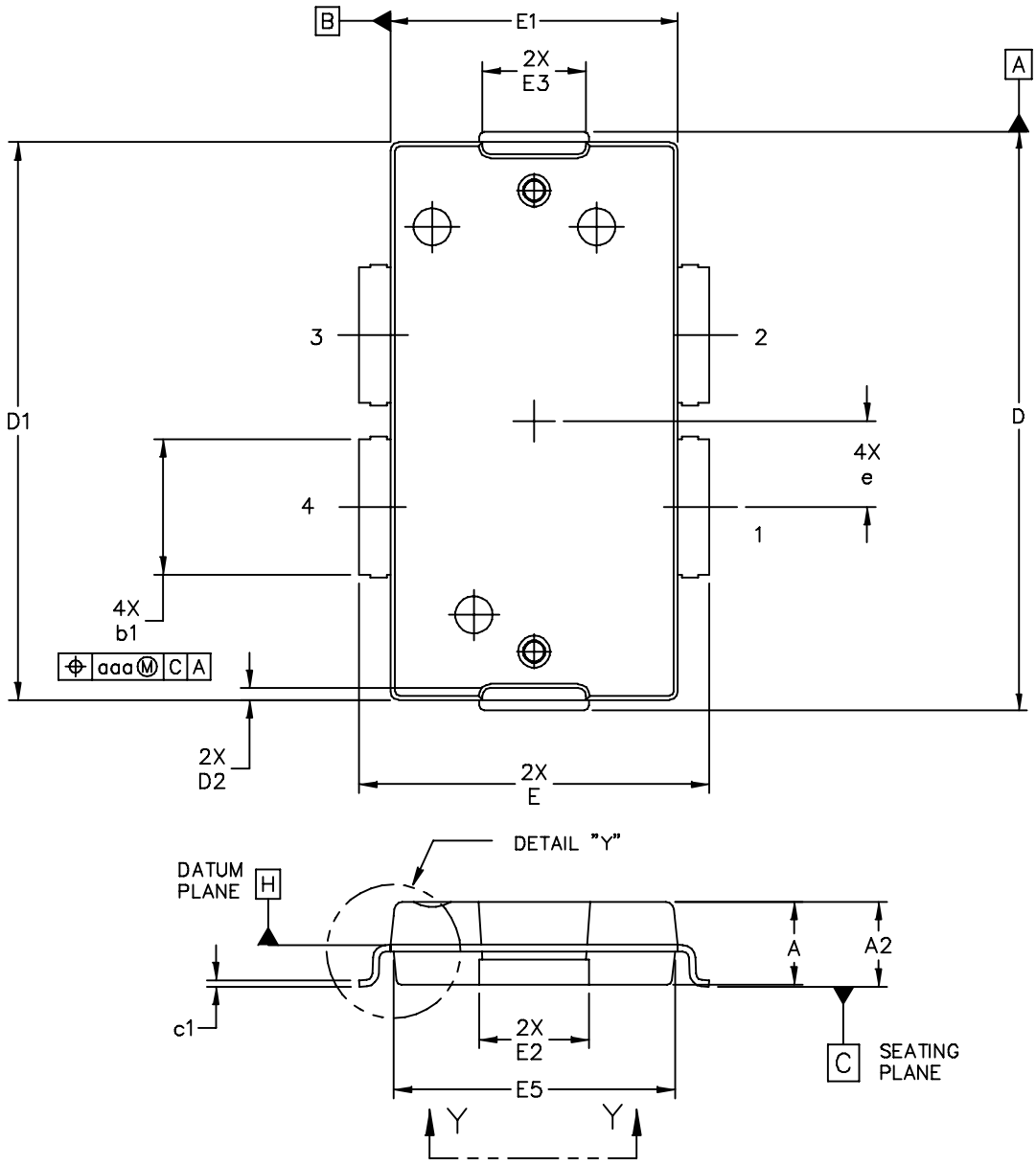

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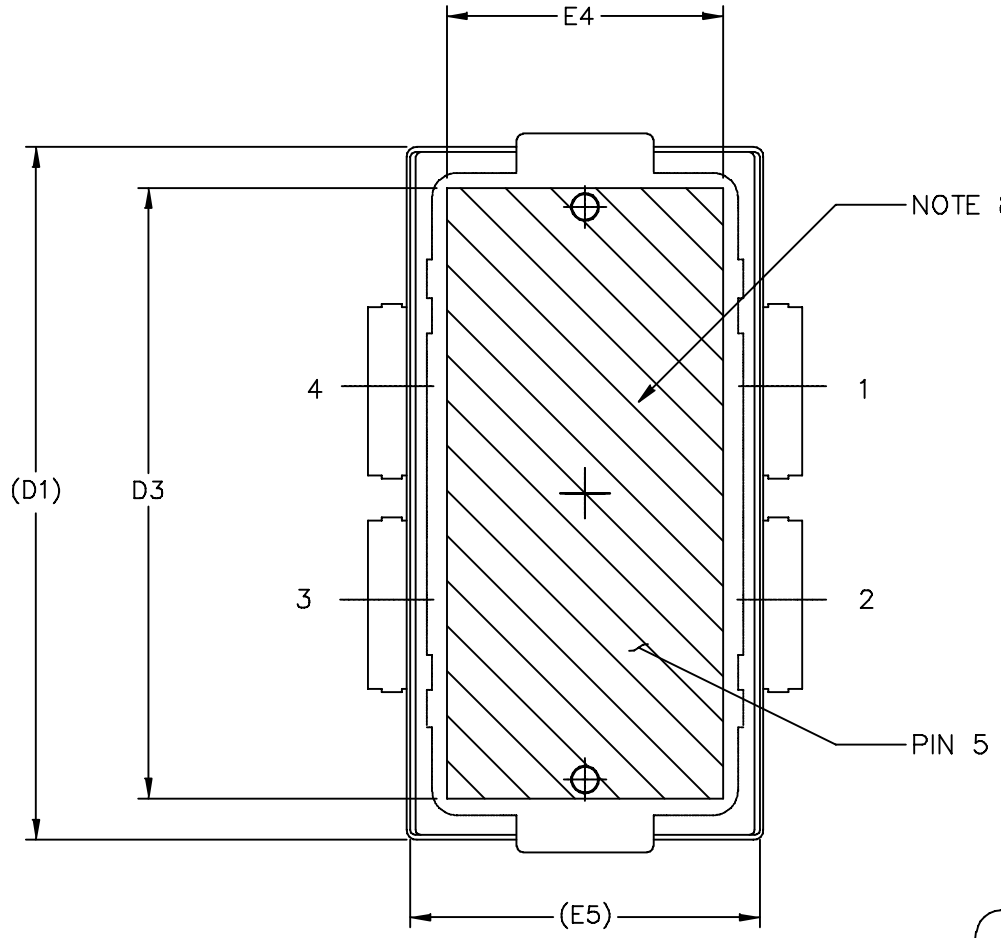
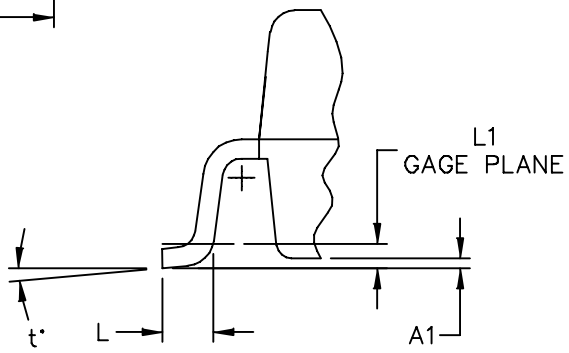
	CASE NUMBER: 1487−05	03 AUG 2007	
	STANDARD: JEDEC TO−270 BB		



VIEW Y–Y



DETAIL "Y"

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	STANDARD: JEDEC TO–270 BB	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 − DRAIN
PIN 2 − DRAIN
PIN 3 − GATE
PIN 4 − GATE
PIN 5 − SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.01 BSC		0.25 BSC	
A2	.101	.108	2.56	2.74	b1	.164	.170	4.17	4.32
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.106 BSC		2.69 BSC	
D2	.011	.019	0.28	0.48	t	2°	8°	2°	8°
D3	.600	----	15.24	----	aaa	.004		0.1	
E	.429	.437	10.90	11.10					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	----	6.86	----					
E5	.346	.350	8.79	8.89					

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	STANDARD: JEDEC TO−270 BB	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2009	• Initial Release of Data Sheet

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