ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4511B & NTE4511BT
Integrated Circuit
CMOS, BCD–to–Seven Segment Latch/Decoder/Driver

Description:

The NTE4511B (16–Lead DIP) and NTE4511BT (SOIC–16) BCD–to–seven segment latch/decoder/drivers are constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4–bit storage latch, an 8421 BCD–to–seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn–off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven–segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.), display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features:

- Low Logic Circuit Power Dissipation
- High–Current Sourcing Outputs (Up to 25mA)
- Latching Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on All Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3Vcd to 10Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 10mA
Maximum Output Drive Current (Source) Per Output, I_{OH}max 25mA
Maximum Continuous Output Power (Source) Per Output (Note 2), P_{OH}max 50mW
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Due to the sourcing capability of these circuits, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Absolute Maximum Ratings)
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Note 2. $P_{OH}max = I_{OH} (V_{DD} - V_{OH})$

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
V_{in} = 0 or V_{DD}		10	9.1	–	9.1	9.58	–	9.1	–	Vdc
		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
Input Voltage (Note 5) "0" Level	V_{IL}									
(V_O = 3.8 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 8.8 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.8 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 3.8Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 8.8Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.8Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Voltage Source	V_{OH}									
(I_{OH} = 0mAdc)		5.0	4.10	–	4.10	4.57	–	4.1	–	Vdc
(I_{OH} = 5.0mAdc)			–	–	–	4.24	–	–	–	Vdc
(I_{OH} = 10mAdc)			3.90	–	3.90	4.12	–	3.5	–	Vdc
(I_{OH} = 15mAdc)			–	–	–	3.94	–	–	–	Vdc
(I_{OH} = 20mAdc)			3.40	–	3.40	3.75	–	3.0	–	Vdc
(I_{OH} = 25mAdc)			–	–	–	3.54	–	–	–	Vdc
(I_{OH} = 0mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0mAdc)			–	–	–	9.26	–	–	–	Vdc
(I_{OH} = 10mAdc)			9.00	–	9.00	9.17	–	8.6	–	Vdc
(I_{OH} = 15mAdc)			–	–	–	9.04	–	–	–	Vdc
(I_{OH} = 20mAdc)			8.60	–	8.60	8.90	–	8.2	–	Vdc
(I_{OH} = 25mAdc)			–	–	–	8.75	–	–	–	Vdc
(I_{OH} = 0mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0mAdc)			–	–	–	14.27	–	–	–	Vdc
(I_{OH} = 10mAdc)			14.0	–	14.0	14.18	–	13.6	–	Vdc
(I_{OH} = 15mAdc)			–	–	–	14.07	–	–	–	Vdc
(I_{OH} = 20mAdc)			13.6	–	13.6	13.95	–	13.2	–	Vdc
(I_{OH} = 25mAdc)			–	–	–	13.80	–	–	–	Vdc

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

Note 5. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 6. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD}f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Electrical Characteristics (Cont'd): (Voltages referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Drive Current Sink (V_{OL} = 0.4Vdc)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on All Outputs, All Buffers Switching Note 4, Note 6)	I_T	5.0	$I_T = (1.9\mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.8\mu A/kHz)\ f + I_{DD}$							µAdc
		15	$I_T = (6.7\mu A/kHz)\ f + I_{DD}$							µAdc

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Note 4. The formulas given are for the typical characteristics only at +25°C.

Note 5. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 6. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (1.5ns/pf) C_L + 50ns	t_{TLH},	5.0	–	40	80	ns
t_{TLH} = (0.75ns/pf) C_L + 37.5ns		10	–	30	60	ns
t_{TLH} = (0.55ns/pf) C_L + 37.5ns		15	–	25	60	ns
Output Fall Time t_{THL} = (1.5ns/pf) C_L + 50ns	t_{THL}	5.0	–	125	250	ns
t_{THL} = (0.75ns/pf) C_L + 37.5ns		10	–	75	150	ns
t_{THL} = (0.55ns/pf) C_L + 37.5ns		15	–	65	130	ns
Data Propagation Delay Time t_{PLH} = (0.40ns/pf) C_L + 620ns	t_{PLH}	5.0	–	640	1280	ns
t_{PLH} = (0.25ns/pf) C_L + 237.5ns		10	–	250	500	ns
t_{PLH} = (0.20ns/pf) C_L + 165ns		15	–	175	350	ns
t_{PHL} = (1.3ns/pf) C_L + 655ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60ns/pf) C_L + 260ns		10	–	290	580	ns
t_{PHL} = (0.35ns/pf) C_L + 182.5ns		15	–	200	400	ns

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics (Cont'd): (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Blank Propagation Delay Time t_{PLH} = (0.30ns/pf) C_L + 305ns	t_{PLH}	5.0	–	600	750	ns
t_{PLH} = (0.25ns/pf) C_L + 117.5ns		10	–	200	300	ns
t_{PLH} = (0.15ns/pf) C_L + 92.5ns		15	–	150	220	ns
t_{PHL} = (0.85ns/pf) C_L + 442.5ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45ns/pf) C_L + 177.5ns		10	–	200	400	ns
t_{PHL} = (0.35ns/pf) C_L + 142.5ns		15	–	160	320	ns
Lamp Test Propagation Delay Time t_{PLH} = (0.45ns/pf) C_L + 290.5ns	t_{PLH}	5.0	–	313	625	ns
t_{PLH} = (0.25ns/pf) C_L + 112.5ns		10	–	125	250	ns
t_{PLH} = (0.20ns/pf) C_L + 80ns		15	–	90	180	ns
t_{PHL} = (1.3ns/pf) C_L + 248ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45ns/pf) C_L + 102.5ns		10	–	125	250	ns
t_{PHL} = (0.35ns/pf) C_L + 72.5ns		15	–	90	180	ns
Setup Time	tsu	5.0	180	90	–	ns
		10	76	38	–	ns
		15	40	20	–	ns
Hold Time	th	5.0	0	–90	–	ns
		10	0	–38	–	ns
		15	0	–20	–	ns
Latch Enable Pulse Width	t_{WL}	5.0	520	260	–	ns
		10	220	110	–	ns
		15	130	65	–	ns

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

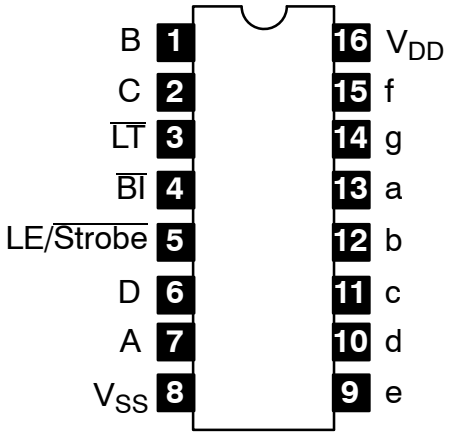
Truth Table:

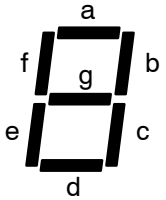
Inputs							Outputs							
LE	**$\overline{BI}$**	**$\overline{LT}$**	**D**	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't Care

* Depends upon the BCD code previously applied when LE = 0

Pin Connection Diagram





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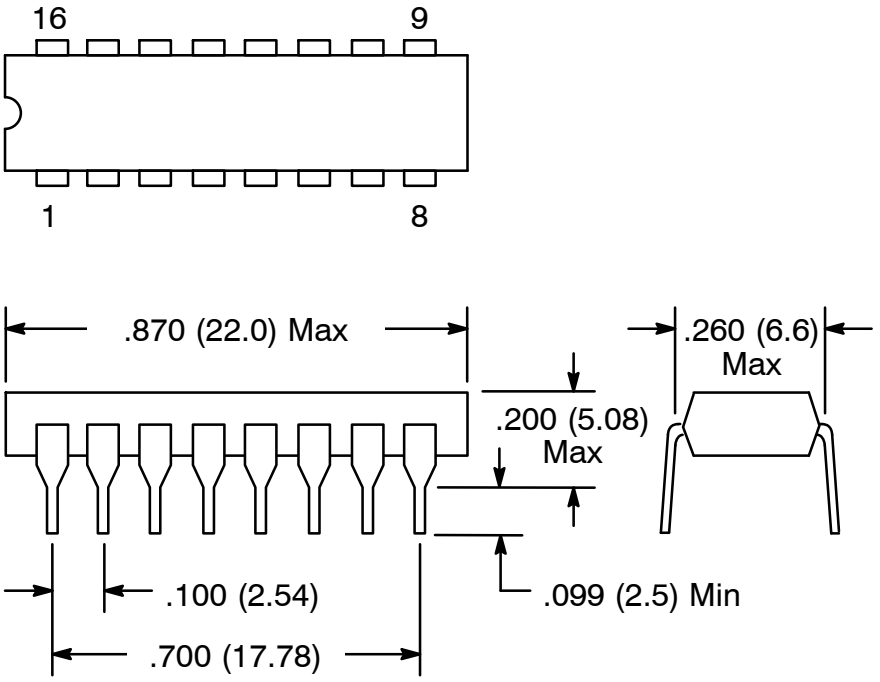
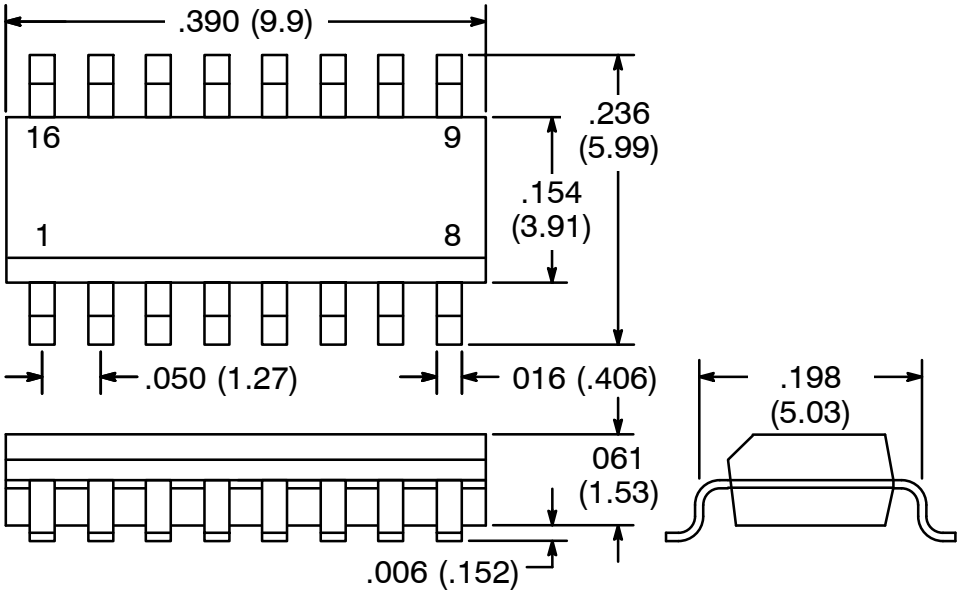


NTE4511BT



NOTE: Pin1 on Beveled Edge