AN-EVAL ICE3AR2280VJZ

20 W 5 V SMPS Evaluation Board with ICE3AR2280VJZ

Application Note

About this document

Scope and purpose

This document is an engineering report that describes universal input 20 W 5 V off-line flyback converter using Infineon CoolSET™ F3R80 family, ICE3AR2280VJZ. The converter is operated in Discontinuous Conduction Mode, 100 kHz fixed frequency, very low standby power and various mode of protections for a high reliable system. This evaluation board is designed to evaluate the performance of ICE3AR2280VJZ in ease of use.

Intended audience

This document is intended for users of the ICE3AR2280VJZ who wish to design low cost and high reliable systems of off-line SMPS for enclosed adapter or open frame auxiliary power supply of white goods, PC, server, DVD, TV, Set-top box, etc.

Table of Contents

1 Abstract

This document is an engineering report of a universal input 20 W 5 V off-line flyback converter power supply utilizing F3R80 CoolSET™ ICE3AR2280VJZ. The application evaluation board is operated in Discontinuous Conduction Mode (DCM) and is running at 100 kHz switching frequency. It has a single output voltage with secondary side control regulation. It is especially suitable for small power supply such as DVD player, set-top box, game console, charger and auxiliary power of white goods, server, PC and high power system, etc. The ICE3AR2280VJZ is the latest version of the CoolSET™. Besides having the basic features of the F3R CoolSET™ such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for major fault (V_{CC} over voltage, V_{CC} under voltage, adjustable input OVP, over temperature, over-load, open loop and short opto-coupler), it also has the BiCMOS technology design, selectable entry and exit burst mode level, adjustable AC line input over voltage protection feature, built-in soft start time, built-in and extendable blanking time and frequency jitter feature, etc. The particular features are the Best-in-Class low standby power and the good EMI performance.

2 Evaluation board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

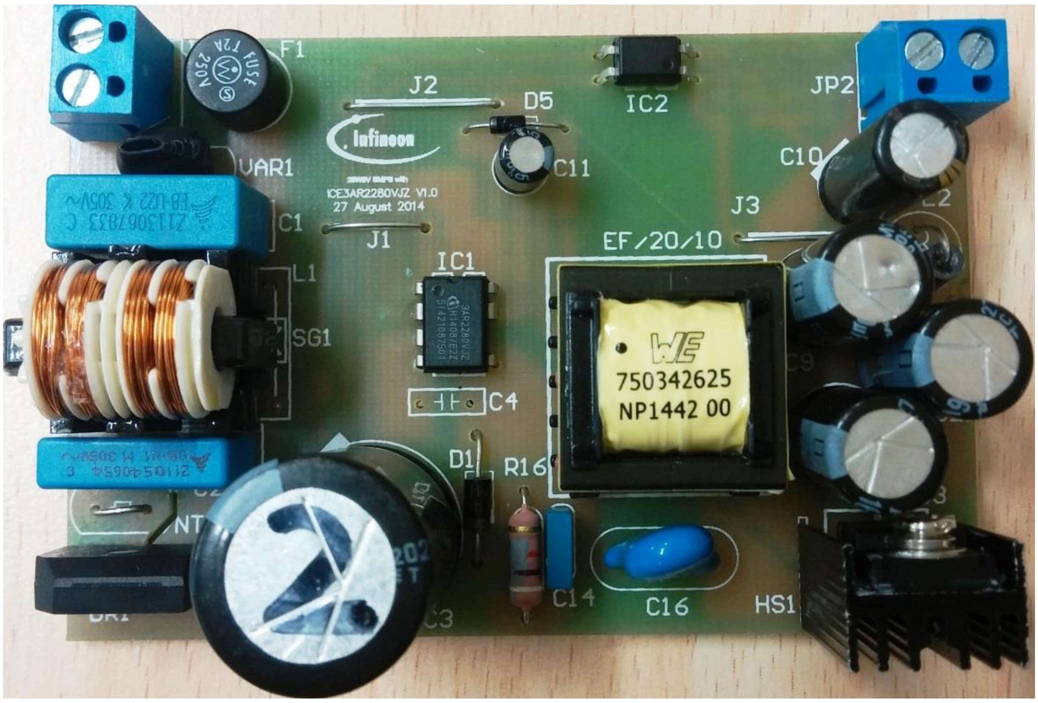


Figure 1 EVAL ICE3AR2280VJZ

3 Specifications of evaluation board

Table 1 Specifications of EVAL ICE3AR2280VJZ

Input voltage	85 V_{AC}~265 V_{AC}
Input frequency	50~60 Hz
Output voltage	5 V
Output current	4 A
Output power	20 W
Steady state output ripple voltage (±1% of norminal output voltage)	$V_{ripple\_P\_P}$< 50 mV
Dynamic load response undershoot and overshoot (±3% of norminal output voltage)	$V_{ripple\_P\_P}$< 200 mV
Active mode four point average efficiency (25%,50%,75% and 100%load) (EU CoC Version 5, Tier 1) Active mode at 10% load efficiency (EU CoC Version 5, Tier 1)	>82% at 115 V_{AC} and 230 V_{AC} >74%
No-load power consumption (EU CoC Version 5, Tier 2)	< 75 mW
Maximum input power(Peak Power) for universal input range (<±5% of average maximum input power)	<±3% of average maximum input power
Form factor case size (L x W x H)	90 mm x 60 mm x 35 mm (3.54" x 2.36" x 1.37")

4 Features of ICE3AR2280VJZ

Table 2 Features of ICE3AR2280VJZ

800 V avalanche rugged CoolSET™ with startup cell
Active Burst Mode for lowest standby power
Selectable entry and exit burst mode level
100kHz internally fixed switching frequency with jittering feature
Auto restart protection for over load, open Loop, V_{CC} under voltage and over voltage and over temperature
Over temperature protection with 50 °C hysteresis
Built-in 10 ms soft start
Built-in 20 ms and extendable blanking time for short duration peak power
Propagation delay compensation for both maximum load and burst mode
Adjustable input OVP
Overall tolerance of current limiting < ±5%
BiCMOS technology for low power consumption and wide V_{CC} voltage range
Soft gate drive with 50 Ω turn-on resistor

5 Circuit description

5.1 Introduction

The EVAL ICE3AR2280VJZ evaluation board is a low cost off-line flyback switch mode power supply (SMPS) using the ICE3AR2280VJZ integrated power IC from the CoolSET™-F3R80 family. The circuit shown in Figure 2 details a 5 V, 20 W power supply that operates from an AC line input voltage range of 85 V_{AC} to 265 V_{AC} and line input OVP detect/reset voltage is 300/282 V_{AC}, suitable for applications in enclosed adapter or open frame auxiliary power supply for different system such as white goods, PC, server, DVD, LED TV, Set-top box, etc.

5.2 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L1, X-capacitors C1, C2 and Y-capacitor C16 act as EMI suppressors. Optional spark gap device SG1, SG2 and varistor VAR can absorb high voltage stress during lightning surge test. After the bridge rectifier BR1 and the input bulk capacitor C3, a voltage of 90 to 424 V_{DC} is present which depends on input line voltage.

5.3 Line input over voltage protection

The AC line input OVP mode is detected by sensing the voltage level at BV pin through the resistors divider from the bulk capacitor. Once the voltage level at BV pin hits above 1.98V, the controller stops switching and enters into input OVP mode. When the BV voltage drops to 1.91V and the Vcc hits 17V, the input OVP mode is released.

5.4 Start up

Since there is a built-in startup cell in the ICE3AR2280VJZ, no external start up resistor is required. The startup cell is connecting the drain pin of the IC. Once the voltage is built up at the Drain pin of the ICE3AR2280VJZ, the startup cell will charge up the V_{CC} capacitor C11 and C7. When the V_{CC} voltage exceeds the UVLO at 17 V, the IC starts up. Then the V_{CC} voltage is bootstrapped by the auxiliary winding to sustain the operation.

5.5 Operation mode

During operation, the V_{CC} pin is supplied via a separate transformer winding with associated rectification D5 and buffering C11 and C7.In order not to exceed the maximum voltage at V_{CC} pin due to poor coupling of transformer winding, an external zener diode ZD1 and resistor R8 can be added.

5.6 Soft start

The soft start is a built-in function and is set at 10ms.

5.7 RCD clamper circuit

While turns off the CoolMOS™, the clamper circuit R21, C14 ,R16 and D1 absorbs the current caused by transformer leakage inductance once the voltage exceeds clamp capacitor voltage. Finally drain to source voltage of CoolMOS™ is lower than maximum break down voltage ($V_{(BR)DSS}$ = 800 V) of CoolMOS™.

5.8 Peak current control of primary current

The CoolMOS™ drain source current is sensed via external shunt resistors R1 and R2 which determine the tolerance of the current limit control. Since ICE3AR2280VJZ is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle. Besides, the patented propagation delay compensation is implemented to ensure the maximum input power can be controlled in an even tighter manner. The evaluation board shows approximately +/-2.43% of average maximum input power (refer to Figure 11).

5.9 Output stage

On the secondary side the power is coupled out by a schottky diode D3. The capacitor C8, C9, C21 provides energy buffering following with the LC filter L2 and C18 to reduce the output voltage ripple considerably. Storage capacitors C8, C9, C21 are selected to have a very small internal resistance (ESR) to minimize the output voltage ripple.

6 Circuit diagram

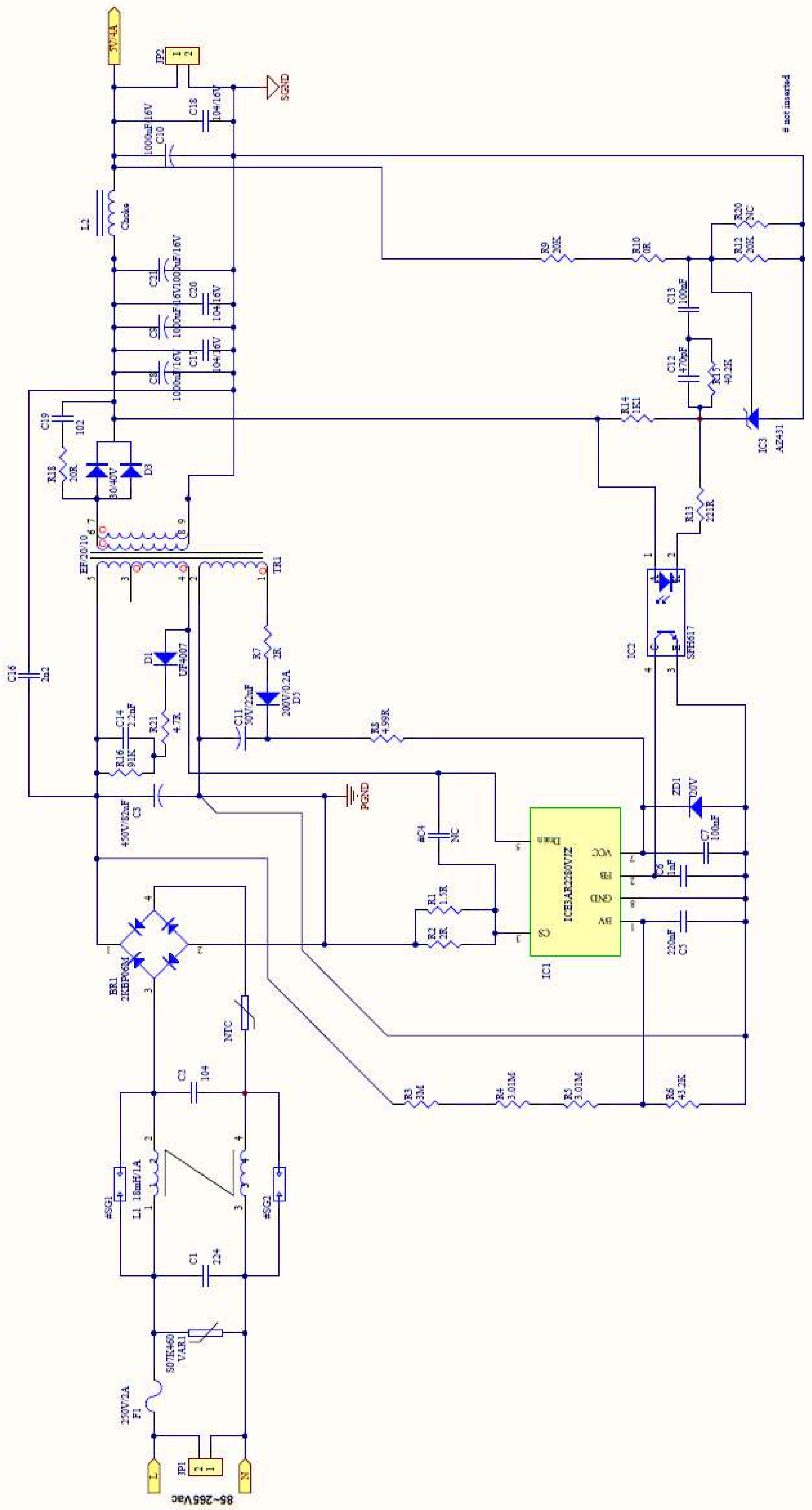


Figure 2 Schematic of EVAL ICE3AR2280VJZ

Note: In order to get the optimized performance of the CoolSET™, the grounding of the PCB layout must be connected very carefully. From the circuit diagram above, it indicates that the grounding for the CoolSET™ can be split into several groups; signal ground, V_{CC} ground, Current sense resistor ground and EMI return ground. All the split grounds should be connected to the bulk capacitor ground separately.

Signal ground includes all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C7, C6, C5 and opto-coupler ground.

V_{CC} ground includes the V_{CC} capacitor ground C11 and the auxiliary winding ground, pin 2 of the power transformer.

Current Sense resistor ground includes current sense resistor R1 and R2.

EMI return ground includes Y capacitor C16.

7 PCB layout

7.1 Top side

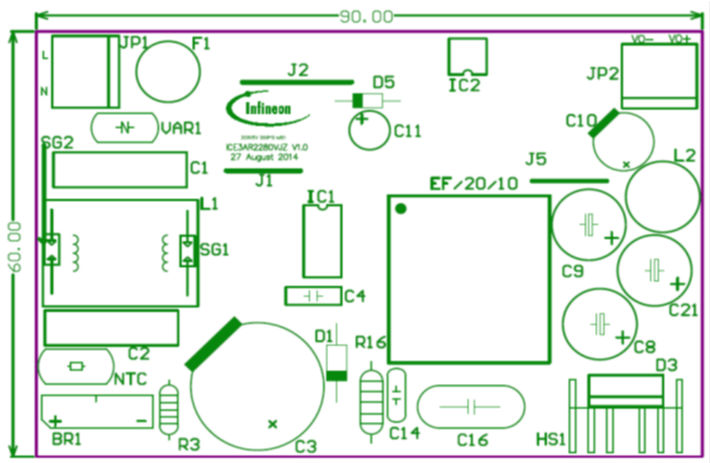


Figure 3 Top side component legend

7.2 Bottom side

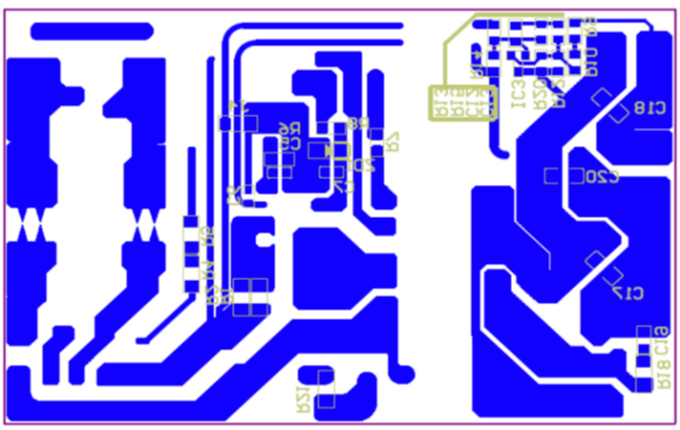


Figure 4 Bottom side copper and component legend

8 Bill of material (BOM)

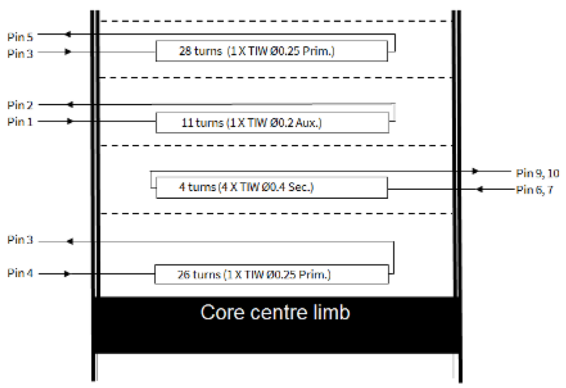
Table 3 Bill of materials

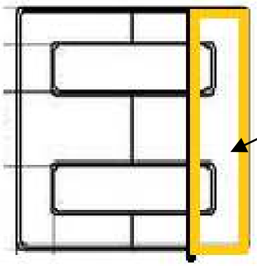
No.	Designator	Component Description	Footprint	Part Number	Manufacturer	Quantity
1	JP1,JP2	5V Test point	Connector	691101710002	Wurth Electronics	2
2	BR1	600V/2A	KBPM	3N257-M4	Vishay	1
3	C1	MKT/220nF/305V	L*W*H: 12.5*7*18-P15mm	B32922C3224M	Epcos	1
4	C2	MKT /100nF/305V	L*W*H: 12.5*5*18-P15mm	B32921C3104M	Epcos	1
5	C3	82uF/450V	Φ*H :18*30-P7.5mm	450TXW82MEF R18x30	Rubycon	1
6	C5	220nF/25V	0603			1
7	C6	1nF/25V	0603			1
8	C7	100nF/50V	0603			1
9	C11	22uF/35V	Φ*H :5*11-P2.5mm	35PX22MEFC5x11	Rubycon	1
10	C14	MKT /2.2nF/630V	L*W*H: 12.5*7.3*6.5-P5mm	B32529C8222J000	Epcos	1
11	C16	Y1/2.2nF/400V	L*W*H: 9*5*10-P10mm			1
12	C19	1nF/1KV	1206			1
13	C8 ,C9,C21	1000uF/16V	Φ*H :10*20-P5mm	16ZL1000MEFC 10x20	Rubycon	3
14	C10	1000uF/16V	Φ*H :8*11.5-P3.5mm			1
15	C17,C18,C20	100nF/16V	1206			3
16	C12	470pF	0805			1
17	C13	100nF /16V	0805			1
18	R3	3M/ 1/4W	DIP-P10mm			1
19	R4,R5	3.1M	1206			2
20	R6	43.2K	1206			1
21	R1	1.5R	1206			1
22	R2	2R	1206			1
23	R21	4.7R	1206			1
24	R7	2R	0805			1

25	R8	4.99R	0805			1
26	R16	92K/1W	DIP-P10mm			1
27	R18	20.1R	1206			1
28	R9	20K	0805			1
29	R10	0R	0805			1
30	R12	20K	0805			1
31	R15	40.2K	0805			1
32	R14	1.1K	0805			1
33	R13	221R	0805			1
34	F1	2A/250V	Φ*H：8.5*7.5-P5mm			1
35	VAR1	VR /S07K460	L*W*H: 9*5.7*11.5-P5mm	B72207S461K101	Epcos	1
36	L1	CM_Choke2* 18mH/1a	L*W*H: 21.46*17*22.6	750342630	Wurth Electronics	1
37	IC1	ICE3AR2280VJZ	DIP-8	ICE3AR2280VJZ	Infineon	1
38	ZD1	20V Zener Diode	SOD-123			1
39	IC2	SFH617-3	DIP-4	SFH617-3		1
40	IC3	AZ431	SOT-23	AZ431		1
41	TR1	410uH(54:4:11)	TR_EF20/10/6_H_10Pin	750342625	Wurth Electronics	1
42	D1	UF4007	DO-41	UF4007		1
43	D5	1N485B 0.2A/200V	DO-35			1
44	D3	SG30SC4M	TO-220FB	SG30SC4M	Shindengen	1
45	L2	Sleeve Choke	DIP-P5	742700221	Wurth Electronics	1
46	J1,J3	Jumper	DIP-P10mm			2
47	J2	Jumper	DIP-P15mm			1
48	J4	0R	1206			1
49	HS1					1
50	NTC	Jumper	DIP-P5mm			1

9 Transformer construction

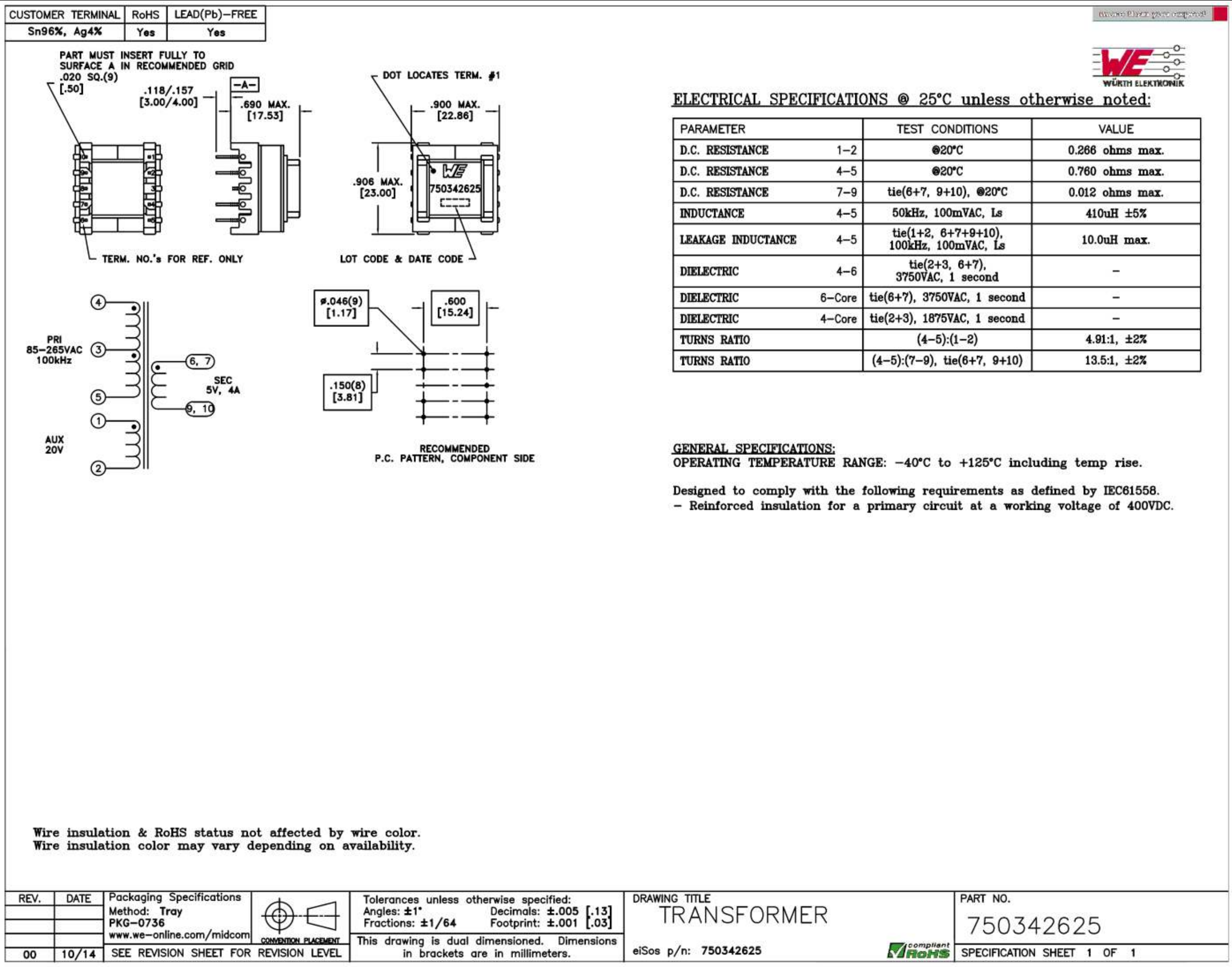
Core and material: EE20/10/6(EF20), TP4A (TDG)
Bobbin: 070-4989 (10-Pins, TH-H, Horizontal version)
Primary Inductance, L_P=410 µH (±5%), measured between pin 4 and pin 5
Manufacturer and part number: Wurth Electronics Midcom (750342625)





The bottom side of the core above the secondary side pins should be taped with 3 layers isolation tapes.

Start	Stop	No. of turns	Wire size	Layer
4	3	26	1 X TIW Ø0.25mm	½ Primary
6, 7	9, 10	4	4 X TIW Ø0.4mm	Secondary
1	2	11	1 X TIW Ø0.2mm	Auxiliary
3	5	28	1 X TIW Ø0.25mm	½ Primary



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn96%, Ag4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1–2	@20°C	0.266 ohms max.
D.C. RESISTANCE	4–5	@20°C	0.760 ohms max.
D.C. RESISTANCE	7–9	tie(6+7, 9+10), @20°C	0.012 ohms max.
INDUCTANCE	4–5	50kHz, 100mVAC, Ls	410uH ±5%
LEAKAGE INDUCTANCE	4–5	tie(1+2, 6+7+9+10), 100kHz, 100mVAC, Ls	10.0uH max.
DIELECTRIC	4–6	tie(2+3, 6+7), 3750VAC, 1 second	–
DIELECTRIC	6–Core	tie(6+7), 3750VAC, 1 second	–
DIELECTRIC	4–Core	tie(2+3), 1875VAC, 1 second	–
TURNS RATIO		(4–5):(1–2)	4.91:1, ±2%
TURNS RATIO		(4–5):(7–9), tie(6+7, 9+10)	13.5:1, ±2%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: –40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC61558.
– Reinforced insulation for a primary circuit at a working voltage of 400VDC.

Wire insulation & RoHS status not affected by wire color.
Wire insulation color may vary depending on availability.

REV. | DATE
00 | 10/14
Packaging Specifications Method: Tray PKG–0736 www.we-online.com/midcom
SEE REVISION SHEET FOR REVISION LEVEL
CONVENTION PLACEMENT
Tolerances unless otherwise specified: Angles: ±1° Fractions: ±1/64 Decimals: ±.005 [.13] Footprint: ±.001 [.03]
This drawing is dual dimensioned. Dimensions in brackets are in millimeters.
DRAWING TITLE TRANSFORMER
eiSos p/n: 750342625
PART NO. 750342625
SPECIFICATION SHEET 1 OF 1

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

V_{in} (V_{AC})	P_{in} (W)	V_{out} (V_{DC})	I_{out} (A)	$V_{out\_ripple\_pk\_pk}$ (mV)	P_{out} (W)	η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85	0.0230	5.01	0.00	24.30				32.57	5.12
	2.5100	5.01	0.40	10.90	2.00	79.78			
	6.0360	5.01	1.00	10.20	5.01	82.92	81.70		
	12.1800	5.00	2.00	17.30	10.01	82.21			
	18.4200	5.00	3.00	30.00	15.01	81.51			
	24.9800	5.00	4.00	34.00	20.02	80.15			
115	0.0260	5.01	0.00	25.00				33.10	5.34
	2.5200	5.01	0.40	13.40	2.00	79.46			
	6.0300	5.01	1.00	12.80	5.01	83.00	82.74		
	12.0300	5.00	2.00	14.70	10.01	83.23			
	18.1200	5.00	3.00	28.00	15.01	82.86			
	24.4500	5.00	4.00	32.00	20.02	81.87			
230	0.0470	5.01	0.00	26.20				34.00	5.62
	2.6800	5.01	0.40	12.20	2.00	74.72			
	6.1670	5.01	1.00	13.40	5.01	81.24	82.91		
	12.0260	5.00	2.00	16.30	10.01	83.26			
	17.9200	5.00	3.00	22.80	15.01	83.78			
	24.0120	5.00	4.00	30.40	20.02	83.36			
265	0.0560	5.01	0.00	26.20				34.19	5.67
	2.7600	5.01	0.40	11.50	2.00	72.55			
	6.2440	5.01	1.00	13.50	5.01	80.24	82.42		
	12.1130	5.00	2.00	16.01	10.01	82.66			
	17.9940	5.00	3.00	20.03	15.01	83.44			
	24.0220	5.00	4.00	30.00	20.02	83.33			

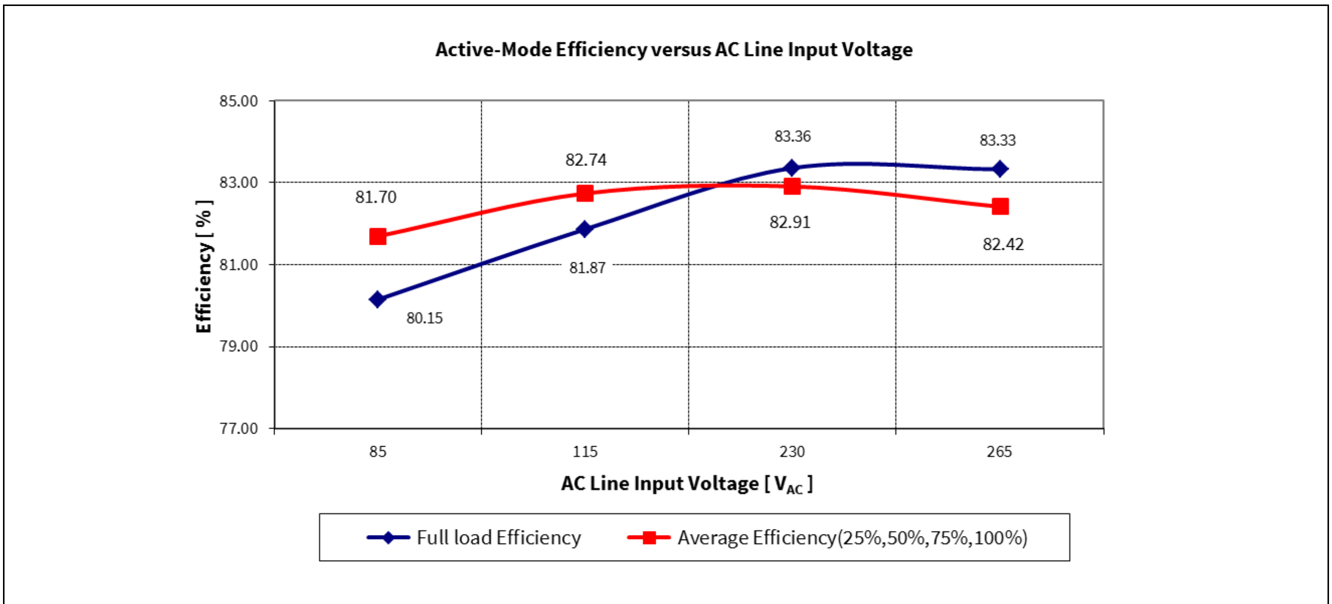


Figure 6 Efficiency vs AC line input voltage

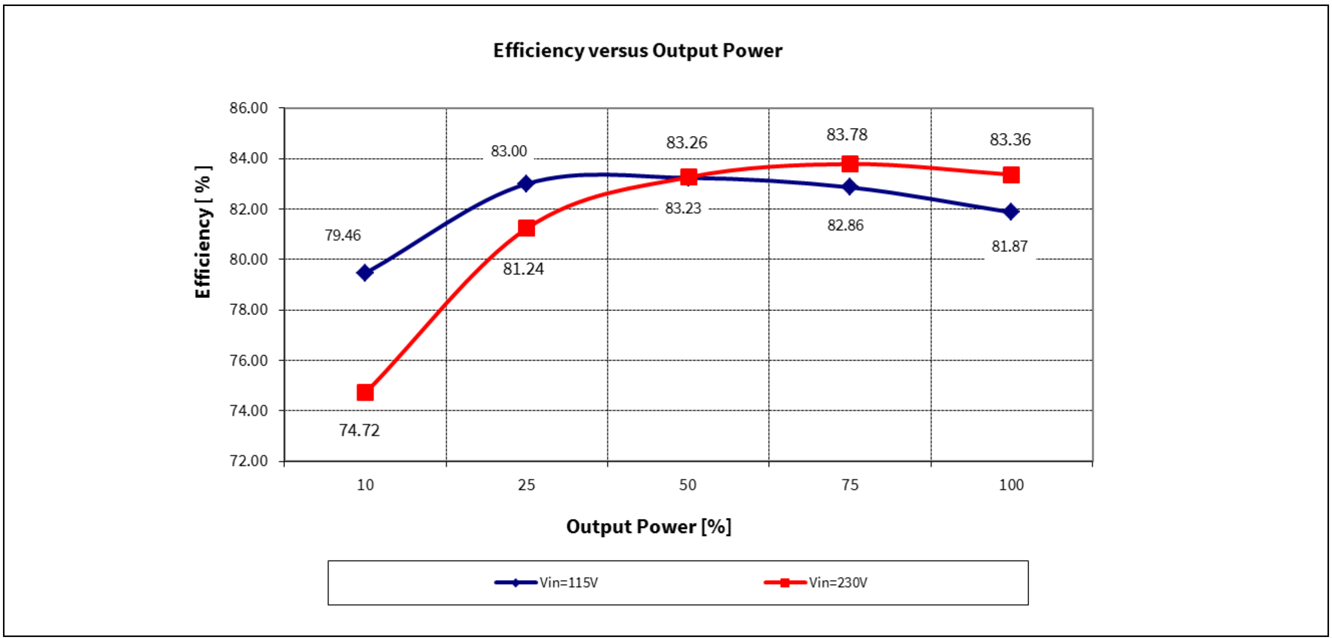


Figure 7 Efficiency vs output power @ 115 V_{AC} and 230 V_{AC} line

10.2 Standby power

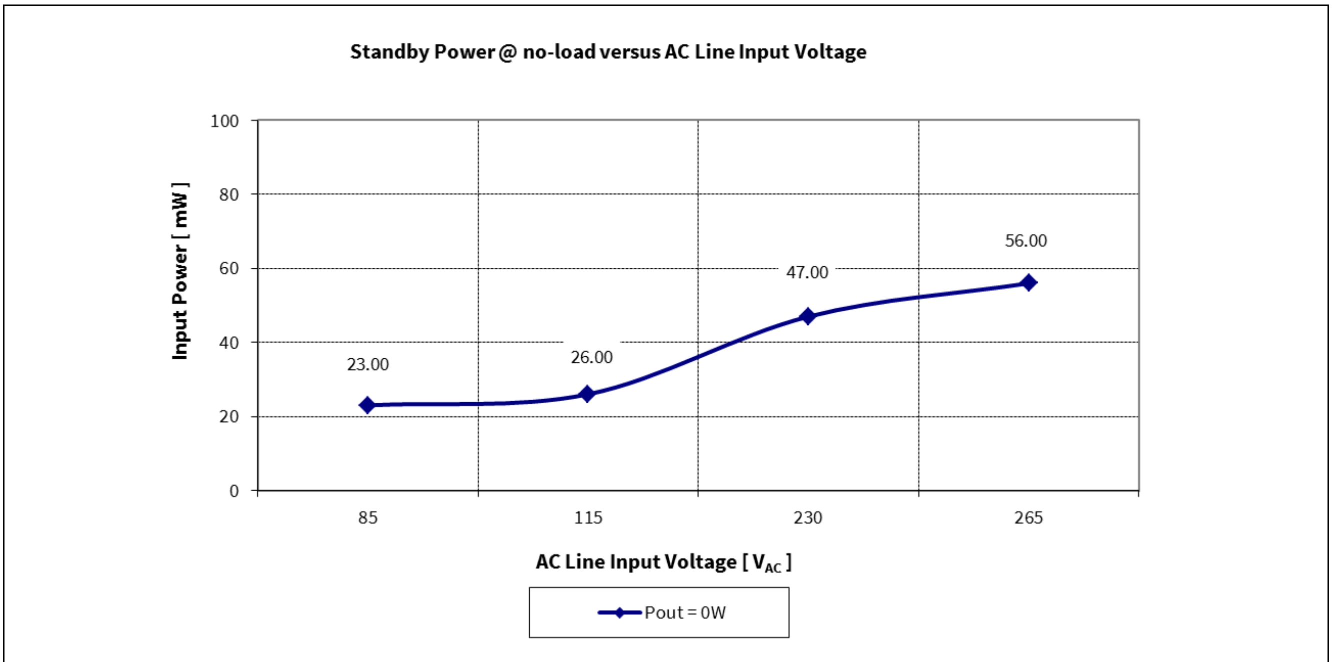


Figure 8 Standby power @ no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

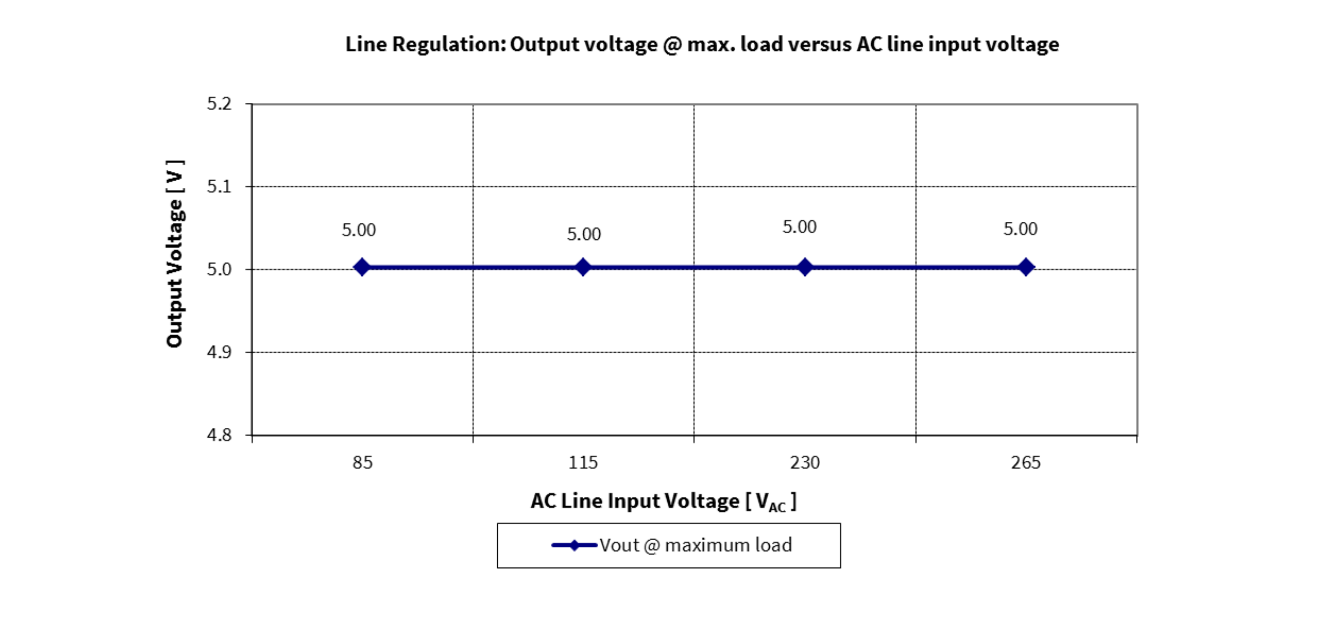


Figure 9 Line regulation V_{out} @ full load vs AC line input voltage

10.4 Load regulation

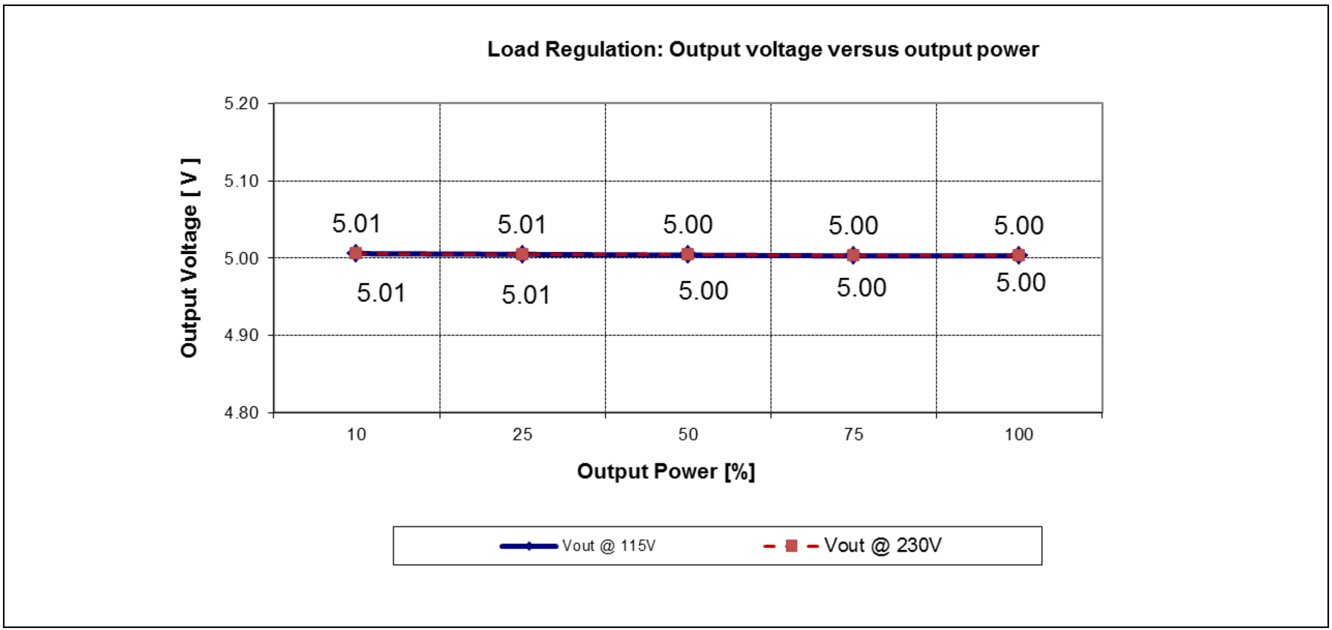


Figure 10 Load regulation V_{out} vs output power

10.5 Maximum power

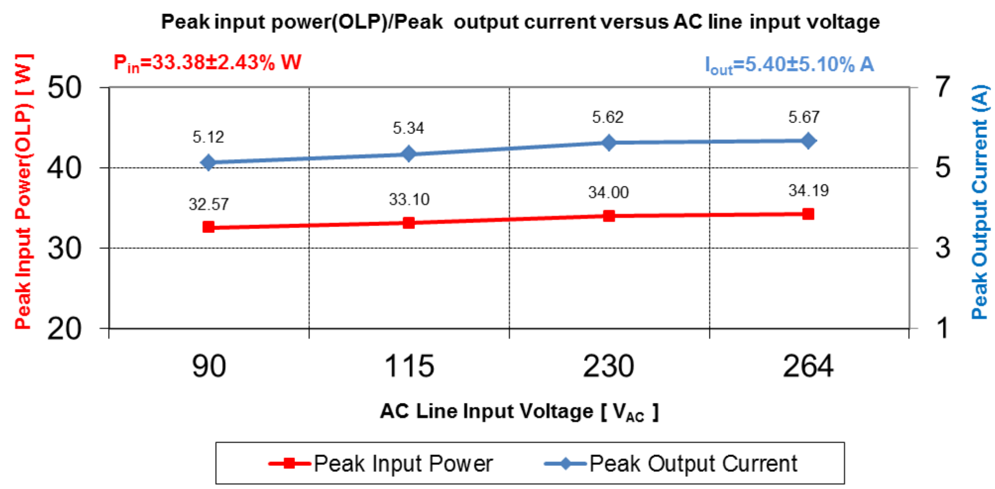


Figure 11 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass [level 3 (±6 kV) for contact discharge].

Pass [special level (±12 kV) for contact discharge by adding SG1 and SG2 (RLS302-301M)].

10.7 Surge immunity (EN61000-4-5)

Pass [Installation class 3, 2 kV (line to earth) and 1 kV (line to line)].

Pass [Installation class 4, 4 kV (line to earth) and 2 kV (line to line) by adding SG1 and SG2 (RLS302-301M)].

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR25503) and followed the test standard of EN55022 (CISPR 22) class B. The evaluation board was set up at maximum load (20 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

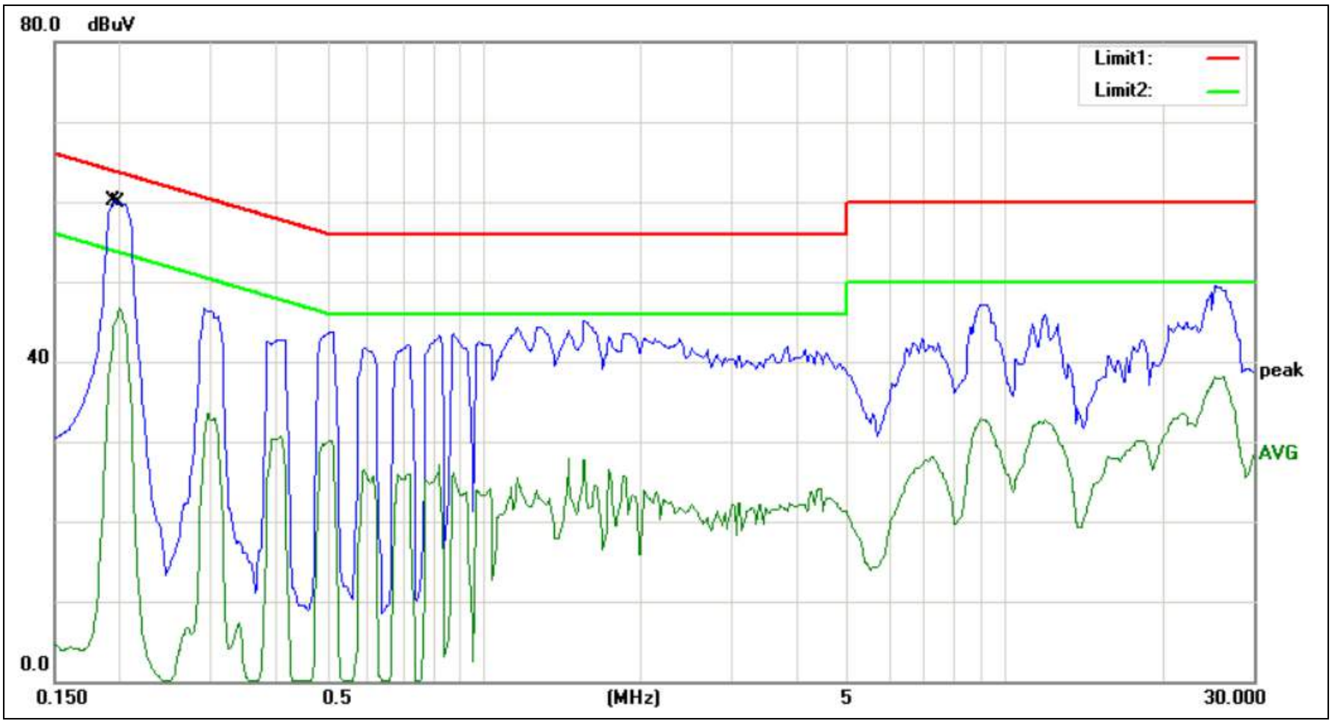


Figure 12 Conducted emissions(Line) at 115 V_{AC} and maximum Load

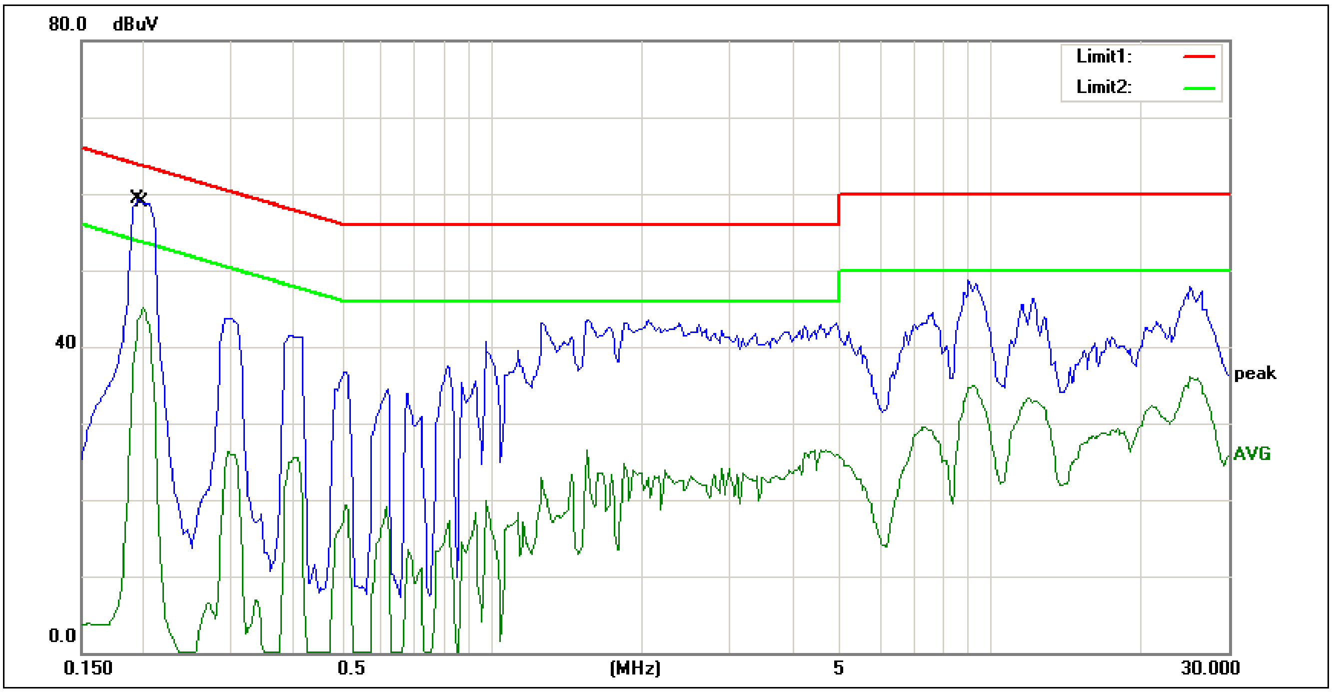


Figure 13 Conducted emissions(Neutral) at 115 V_{AC} and maximum Load

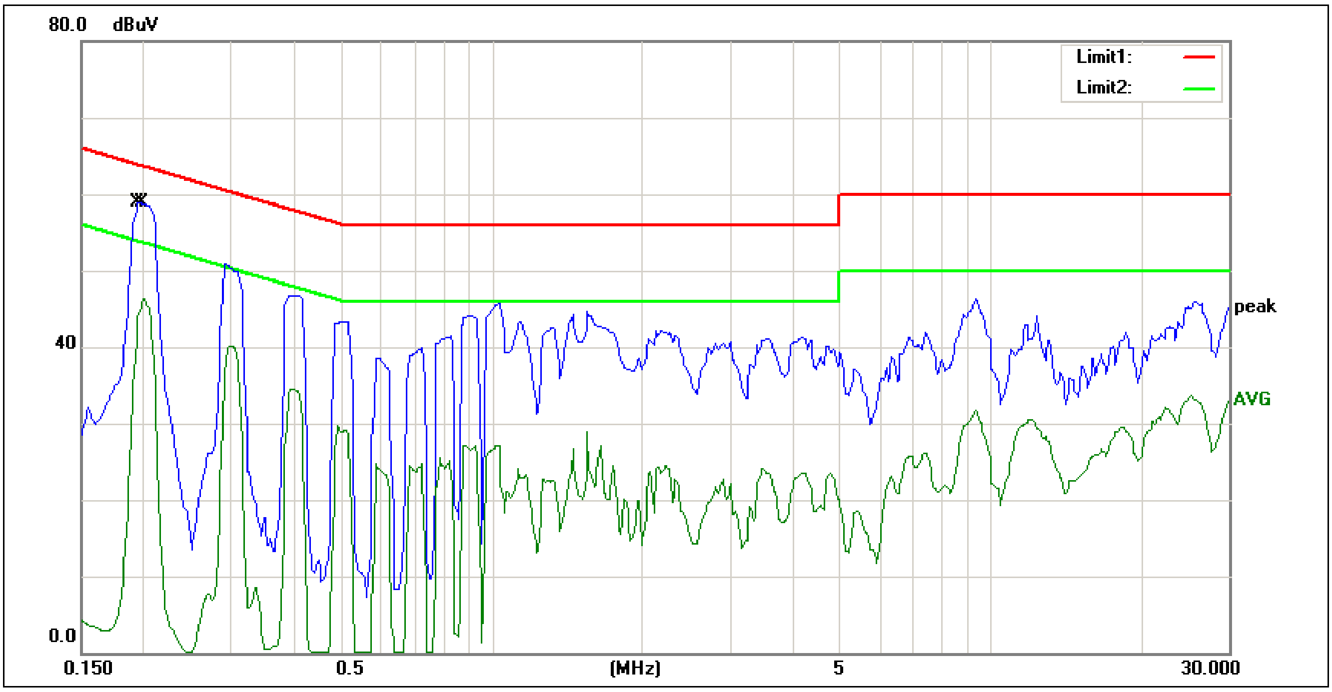


Figure 14 Conducted emissions(line) at 230 V_{AC} and maximum Load

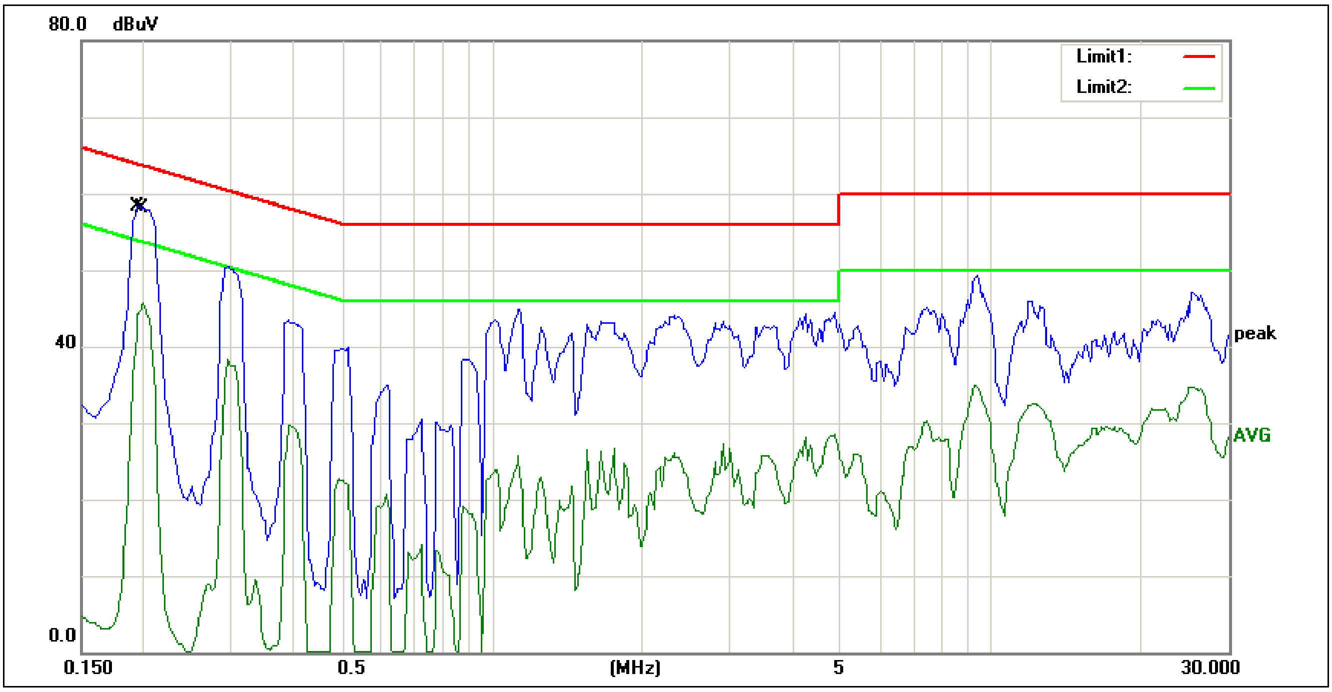


Figure 15 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

Pass conducted EMI EN55022 (CISPR 22) class B with > 6 dB margin for QP.

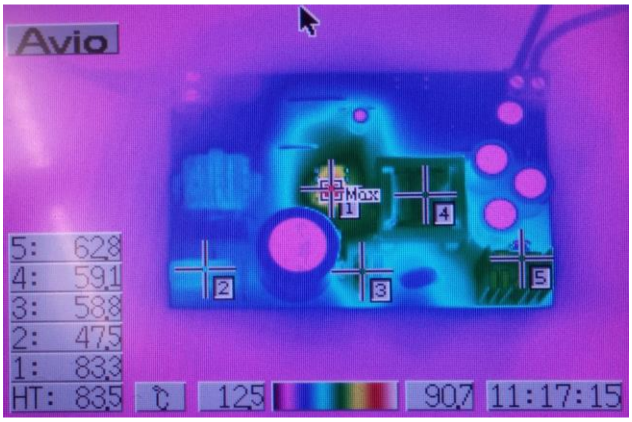
10.9 Thermal measurement

The thermal test of open frame evaluation board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25 ^{o}C. The measurements were taken after two hours running at full load.

Table 5 Hottest temperature of evaluation board

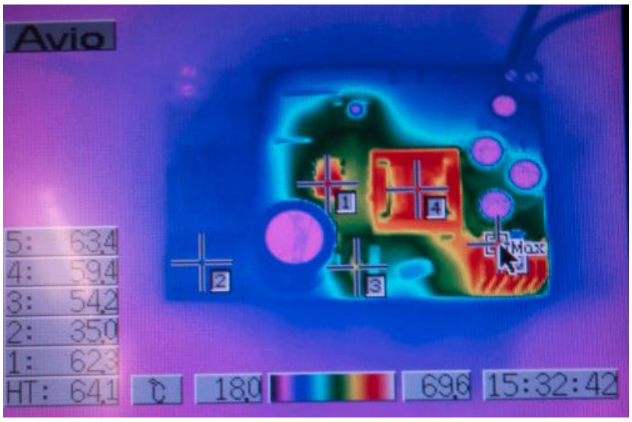
No.	Item	Temperature @ 85 V_{AC} and FL(°C)	Temperature @ 115 V_{AC} and FL(°C)	Temperature @ 230 V_{AC} and FL(°C)	Temperature @ 265 V_{AC} and FL(°C)
1	IC1 (ICE3AR2280VJZ)	83.5	68.5	62.3	62.9
2	BR1	47.5	41.7	35.0	33.8
3	R16	58.8	56.9	54.2	53.8
4	TR1	59.1	59.1	59.4	60
5	D3	62.8	63.0	64.1	64.6
6	Ambient temperature	25	25	25	25

85 V_{AC}, 20 W load, 25 ^{o}C ambient



115 V_{AC}, 20 W load, 25 ^{o}C ambient

230 V_{AC}, 20 W load, 25 ^{o}C ambient



265 V_{AC}, 20 W load, 25 ^{o}C ambient

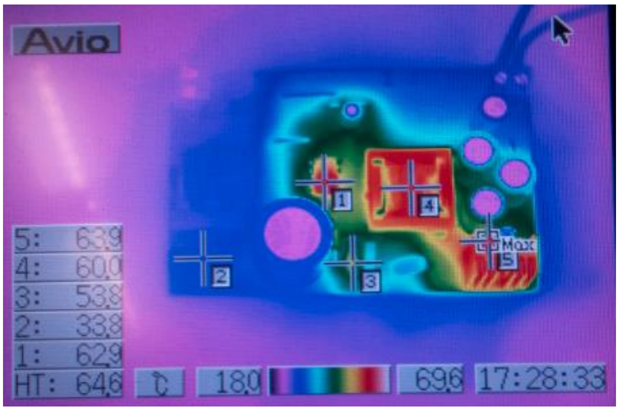
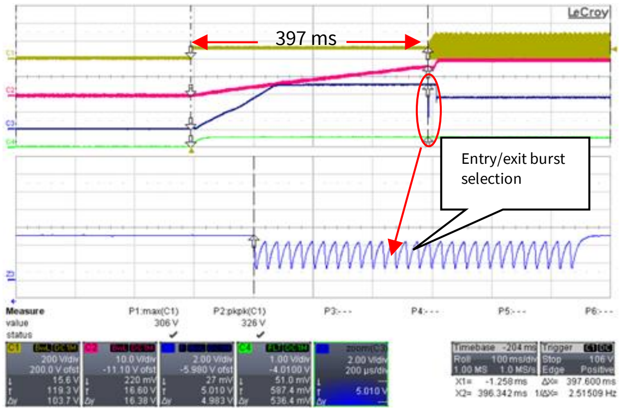


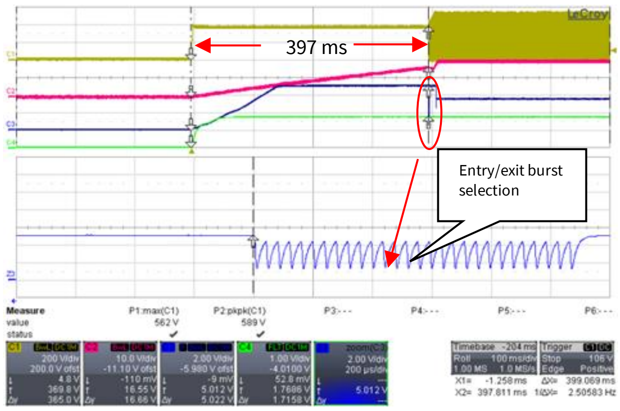
Figure 16 Infrared thermal image of EVAL ICE3AR2280VJZ

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

11.1 Startup at low/high AC line input voltage with maximum load

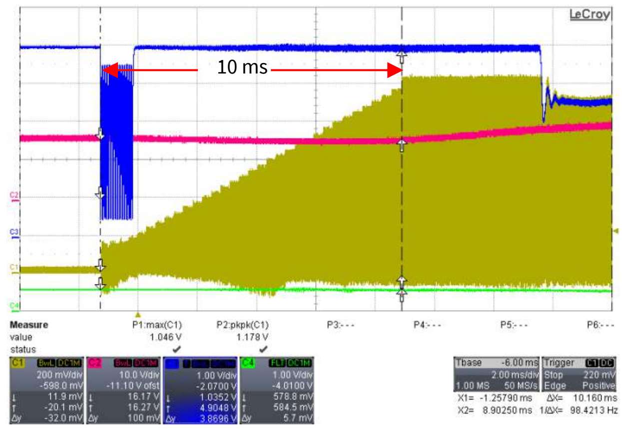




Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel 2; C2(Red): Supply voltage (V_{CC}) Channel 3; C3(Blue) : Feedback voltage (V_{FBB}) Channel 4; C4(Green) :BV voltage (V_{BV})	Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel 2; C2(Red): Supply voltage (V_{CC}) Channel 3; C3(Blue) : Feedback voltage (V_{FBB}) Channel 4; C4(Green) :BV voltage (V_{BV})
Startup time @ 85 V_{AC} & max. load = 397 ms	Startup time @ 265 V_{AC} & max. load = 397 ms

Figure 17 Startup

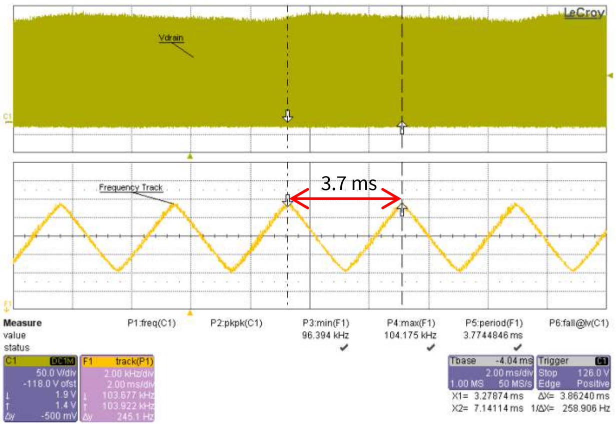
11.2 Soft start



Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : Zero crossing voltage (V_{BV})
Soft Star time @ 85 V_{AC} & max. load = 10 ms

Figure 18 Soft start

11.3 Frequency jittering



Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel F1 : Frequency track of C1
Frequency jittering from 96 kHz ~ 104 kHz, Jitter period is set at 3.7 ms internally

Figure 19 Frequency jittering@ 85 V_{AC} and max. load

11.4 Drain and current sense voltage at maximum load

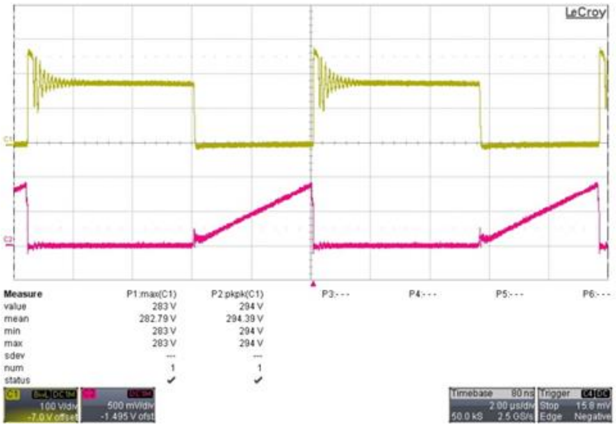
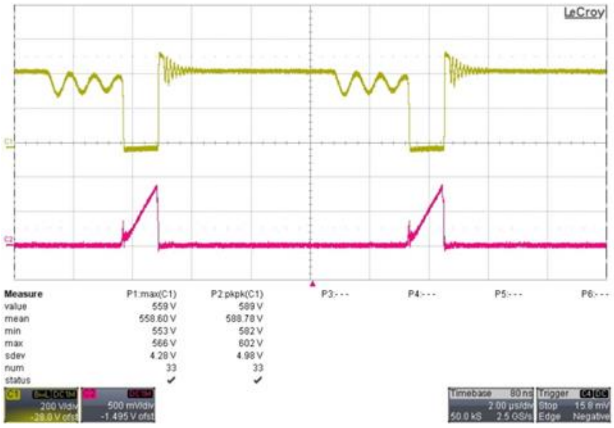
	
Channel 1; C1 : Drain-source voltage (V_{DS}) Channel 2; C2 : Current sense voltage (V_{CS})	Channel 1; C1 : Drain-source voltage (V_{DS}) Channel 2; C2 : Current sense voltage (V_{CS})
V_{Drain_peak} @ 85 V_{AC} = 294 V	V_{Drain_peak} @ 265 V_{AC} = 602 V

Figure 20 Drain and current sense voltage at max. load

11.5 Load transient response (Dynamic load from 10% to 100%)

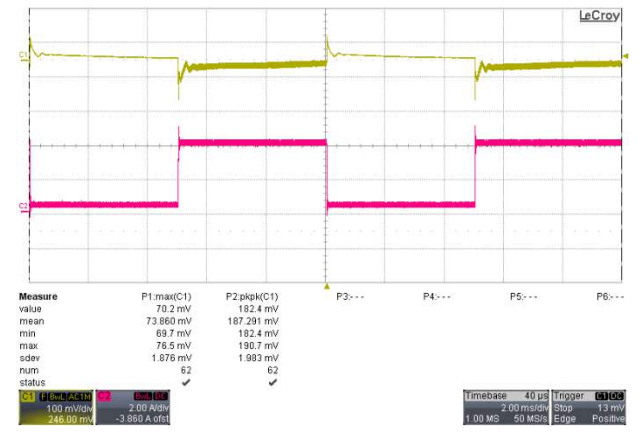
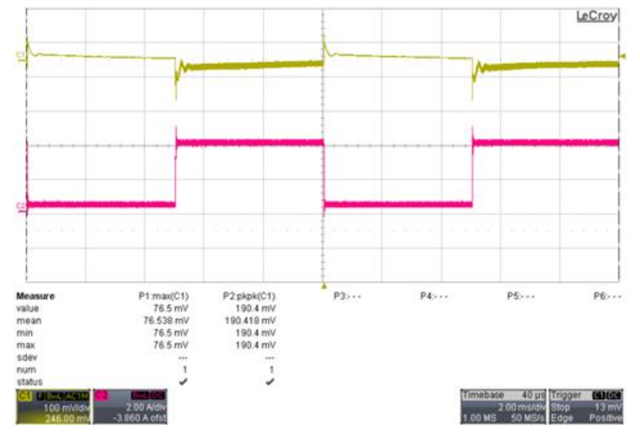
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} =190 mV (Load change from10% to 100%,100 Hz,0.4 A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 26 5V_{AC} =190 mV (Load change from10% to 100%,100 Hz,0.4 A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 21 Load transient response

11.6 Output ripple voltage at maximum load

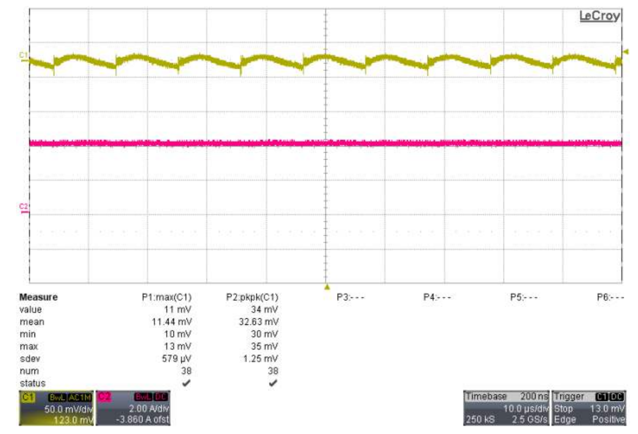
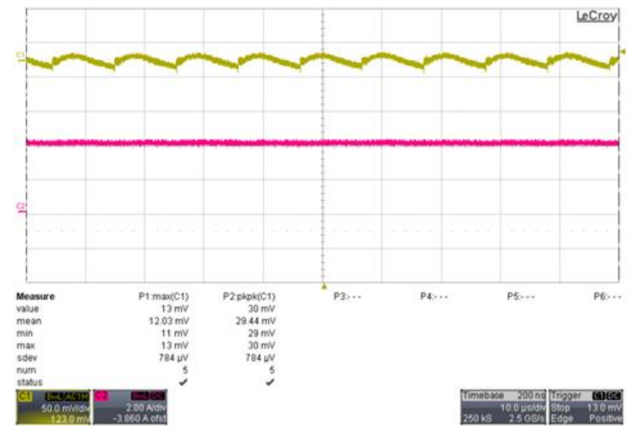
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} =35 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 265 V_{AC} = 30 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 22 AC output ripple at max. load

11.7 Output ripple voltage during burst mode at 1 W load

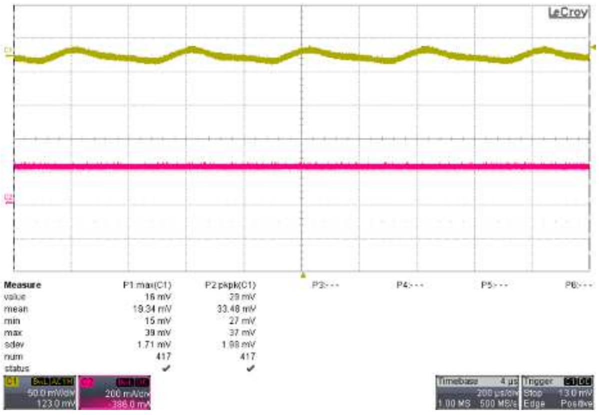
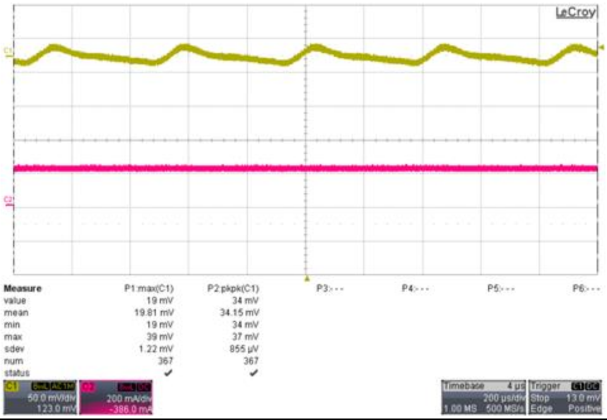
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} =39 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 265 V_{AC} = 39 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 23 AC output ripple at 1 W load

11.8 Active Burst mode operation

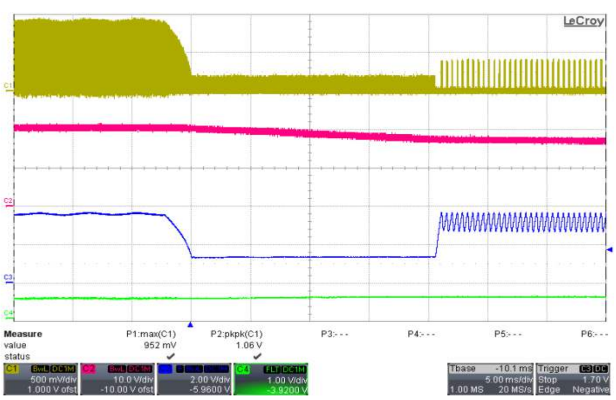
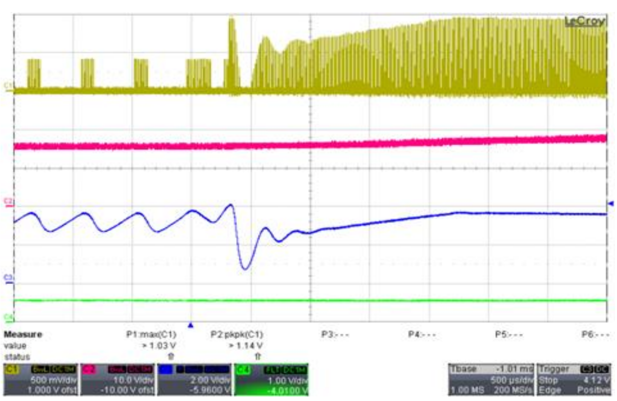
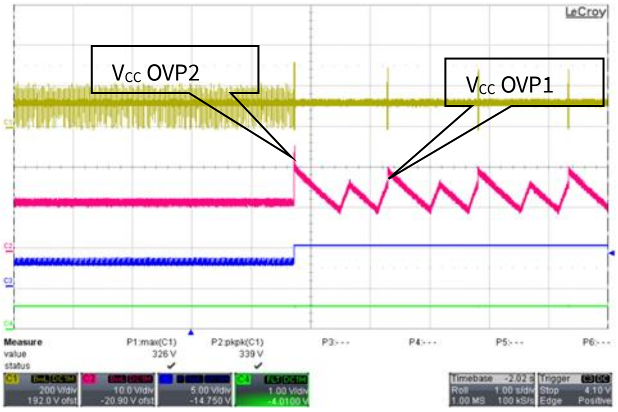
	
Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 :BV voltage (V_{BV})	Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 :BV voltage (V_{BV})
Condition to enter burst: V_{FB}<1.42 V and last for 20 ms (load change form full load to 1 W load)	Condition to leave burst: V_{FB}>4.5 V (load change form 1 W load to full load)

Figure 24 Active burst mode at 85 V_{AC}

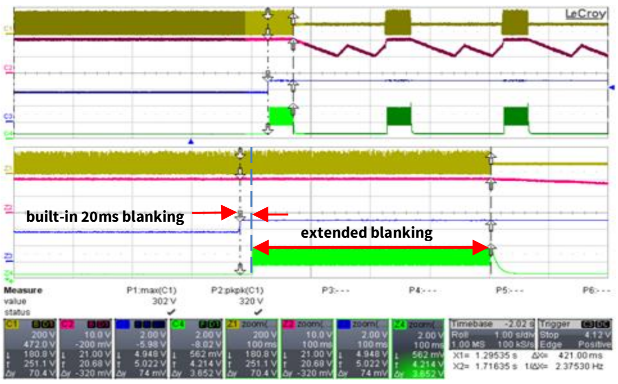
11.9 V_{CC} over voltage protection (Odd skip auto restart mode)



Channel 1; C1 : Drain voltage (V_{Drain}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BV voltage (V_{BV})
Condition: V_{CC}>25.5 V V_{CC}>20.5 V and V_{FB}>4.5 V and during soft start (Short the diode of optocoupler(Pin 1 and 2 of IC2) during system operating at no load)

Figure 25 V_{CC} overvoltage protection at 85 V_{AC}

11.10 Over load protection (Auto restart mode)



Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel 2; C2(Red): Supply voltage (V_{CC}) Channel 3; C3(Blue) : Feedback voltage (V_{FBB}) Channel 4; C4(Green) :BV voltage (V_{BV})
Condition: V_{FB}>4.5 V and last for 20 ms andV_{BV}>4.5 V and last for 30 µs (output load change from 4 Ato 6 A)

Figure 26 Over load protection with built-in+extended blanking time at 85 V_{AC}

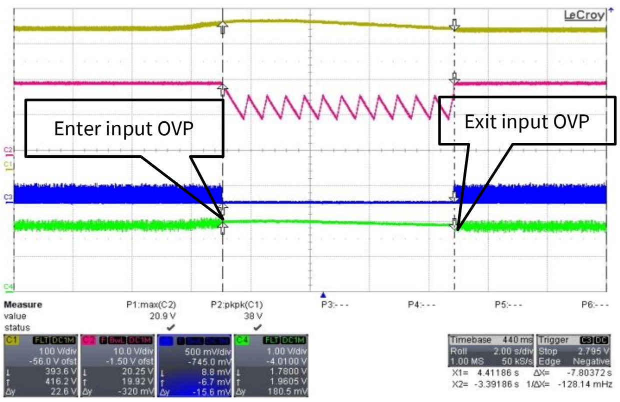
11.11 V_{CC} under voltage/Short optocoupler protection (Normal auto restart mode)

Channel 1; C1(Yellow) : Drain voltage (V_{Drain})
Channel 2; C2(Red): Supply voltage (V_{CC})
Channel 3; C3(Blue) : Feedback voltage (V_{FBB})
Channel 4; C4(Green) :BV voltage (V_{BV})

Condition: V_{CC}<10.5 V
(short the transistor of optocoupler(Pin 3 and 4 of IC2) during system operating @ full load and release)

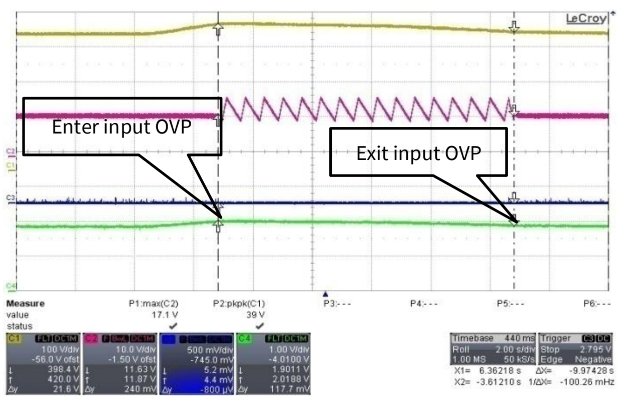
Figure 27 V_{CC} under voltage/short optocoupler protection at 85 V_{AC}

11.12 AC Line input OVP mode



Channel 1; C1(Yellow) : Bulk voltage(V_{bulk})
Channel 2; C2(Red) : Supply voltage (V_{CC})
Channel 3; C3(Blue : Current sense voltage (V_{CS})
Channel 4; C4 (Green): BV voltage (V_{BV})

Max. load condition: V_{BV}>1.98 V and last for 400 µs (OVP detect)
V_{BV}<1.91 V and last for 5 µs (OVP reset)
(gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)



Channel 1; C1(Yellow) : Bulk voltage(V_{bulk})
Channel 2; C2(Red) : Supply voltage (V_{CC})
Channel 3; C3(Blue : Current sense voltage (V_{CS})
Channel 4; C4 (Green): BV voltage (V_{BV})

No load condition: V_{BV}>1.98 V and last for 400 µs (OVP detect)
V_{BV}<1.91 V and last for 5 µs (OVP reset)
(gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)

Figure 28 Input OVP

12 References

[1] Infineon Technologies, Datasheet "CoolSET™-F3R80 ICE3AR2280VJZ Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS™and Startup cell(input OVP and Frequency Jitter) in DIP-7"

[2] Infineon Technologies, AN-PS0044-CoolSET F3R80 DIP-7 brownout/input OVP and frequency jitter version design guide-V1.5

Revision History

Major changes since the last revision

Page or Reference	Description of change
5	Add section 5.3 under circuit description

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