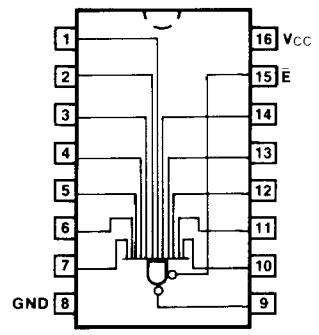


54S/74S134 *010122*
12-INPUT NAND GATE
 (With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C to } +70^\circ\text{ C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{ C to } +125^\circ\text{ C}$	
Plastic DIP (P)	A	74S134PC		9B
Ceramic DIP (D)	A	74S134DC	54S134DM	6B
Flatpak (F)	A	74S134FC	54S134FM	4L

TRUTH TABLE

INPUTS		OUTPUTS	
A	L	Enable	Y
H	H	L	L
Any In LOW		L	H
X	X	H	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	50/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74S		UNITS	CONDITIONS	
			Min	Max			
V _{OH}	Output HIGH Voltage	XM	2.4		V	I _{OH} = -2.0 mA I _{OH} = -6.5 mA	
		XC	2.4				V _{CC} = Min V _{IN} = 0.8 V
I _{CC}	Power Supply Current	Outputs HIGH	13	mA		V _{CC} = Max	
		Outputs LOW	16				
		Outputs OFF	25				
t _{PLH}	Propagation Delay		2.0	6.0	ns	Figs. 3-3, 3-4	
t _{PHL}	Data to Output		2.0	7.5			
t _{PZH}	Output Enable Time				19.5	ns	Figs. 3-3, 3-11, 3-12
t _{PZL}					21		
t _{PHZ}	Output Disable Time				8.5	ns	Figs. 3-3, 3-11, 3-12
t _{PLZ}					14		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

4