

# High Efficiency Linear Regulator

## FEATURES

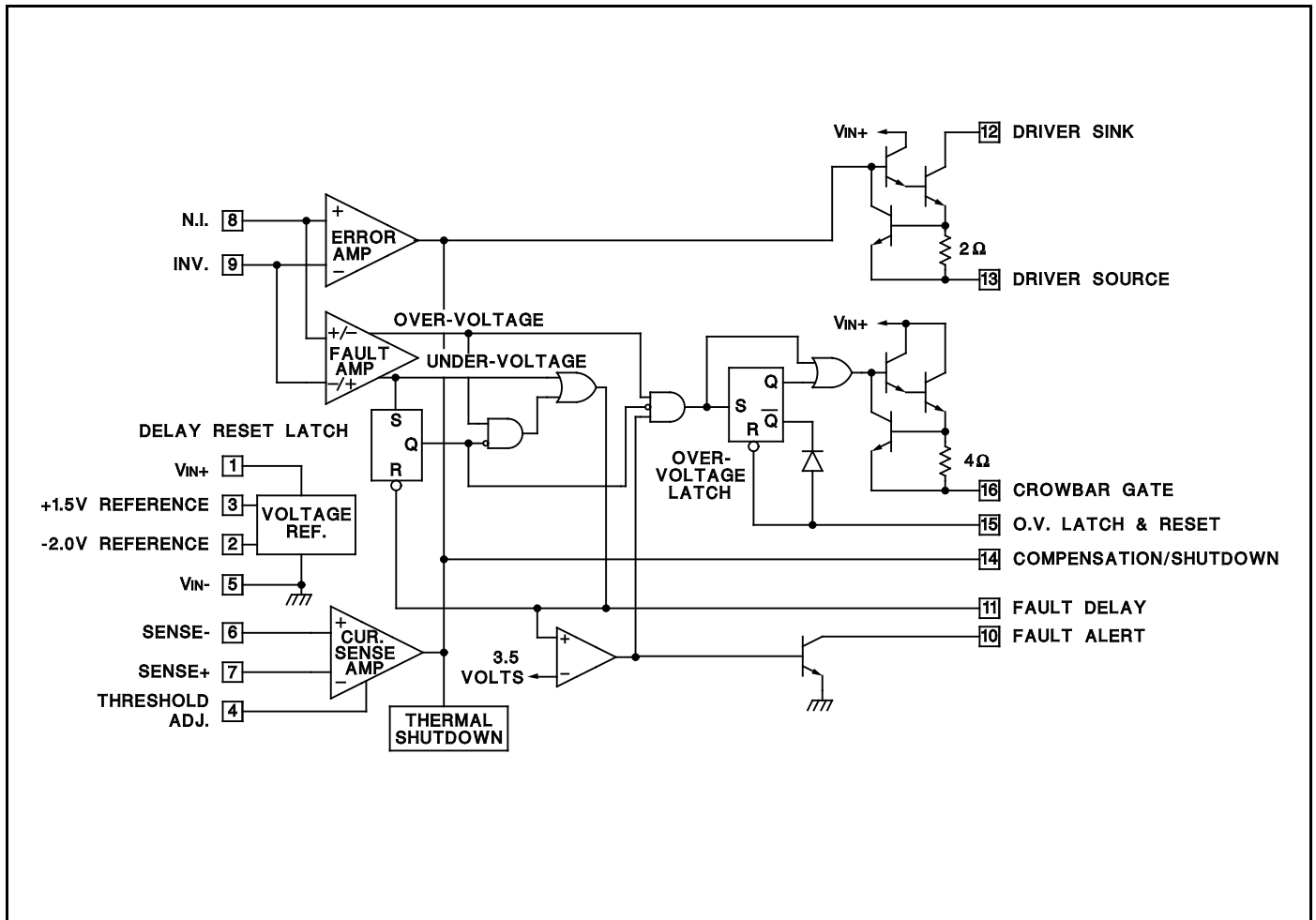
- Minimum  $V_{IN} - V_{OUT}$  Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

## DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

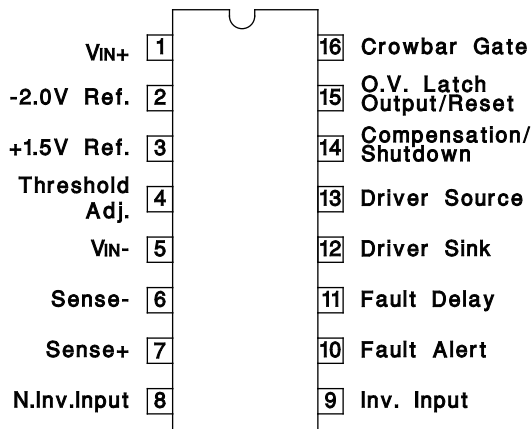
Input Supply Voltage, $V_{IN+}$ .....	40V
Driver Current .....	400mA
Driver Source to Sink Voltage .....	40V
Crowbar Current .....	-200mA
+1.5V Reference Output Current .....	-10mA
Fault Alert Voltage .....	40V
Fault Alert Current .....	15mA
Error Amplifier Inputs .....	-0.5V to 35V
Current Sense Inputs .....	-0.5V to 40V
O.V. Latch Output Voltage .....	-0.5V to 40V
O.V. Latch Output Current .....	15mA

Power Dissipation at $T_A = 25^\circ\text{C}$ .....	1000mW
Power Dissipation at $T_c = 25^\circ\text{C}$ .....	2000mW
Operating Junction Temperature .....	-55°C to +150°C
Storage Temperature .....	-65°C to +150°C
Lead Temperature (soldering, 10 seconds) .....	300°C

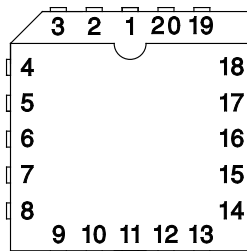
*Note 1: Voltages are reference to  $V_{IN-}$ , Pin 5.  
Currents are positive into, negative out of the specified terminals.  
Consult Packaging section of Databook for thermal limitations and considerations of package.*

**CONNECTION DIAGRAMS**

**DIL-16, SOIC-16 (TOP VIEW)  
J or N Package, DW Package**



**PLCC-20, LCC-20 (TOP VIEW)  
Q, L Packages**



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
$V_{IN+}$	2
-2.0V REF	3
+1.5V REF	4
Threshold Adjust	5
N/C	6
$V_{IN-}$	7
Sense-	8
Sense+	9
N.Inv. Input	10
N/C	11
Inv. Input	12
Fault Alert	13
Fault Delay	14
Driver Sink	15
N/C	16
Driver Source	17
Compensation/ Shutdown	18
O.V. Latch Output/Reset	19
Crowbar Gate	20

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1834,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2834, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3834.  $V_{IN+} = 15\text{V}$ ,  $V_{IN-} = 0\text{V}$ ,  $T_A = T_J$ .

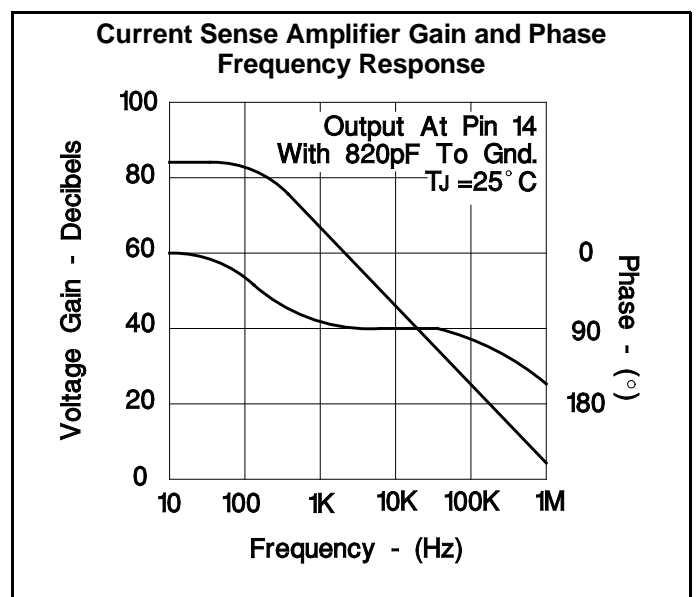
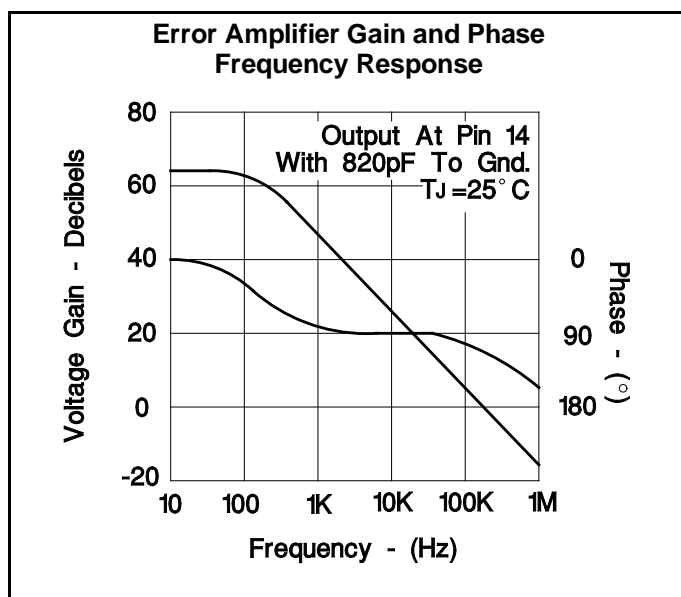
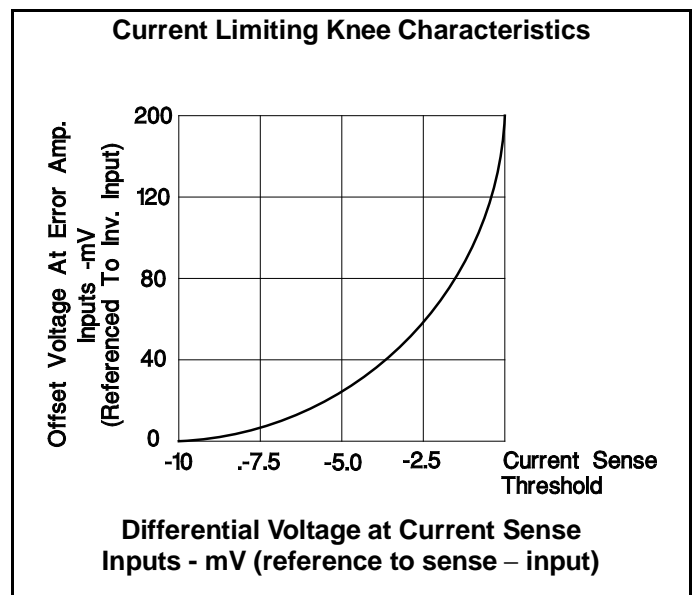
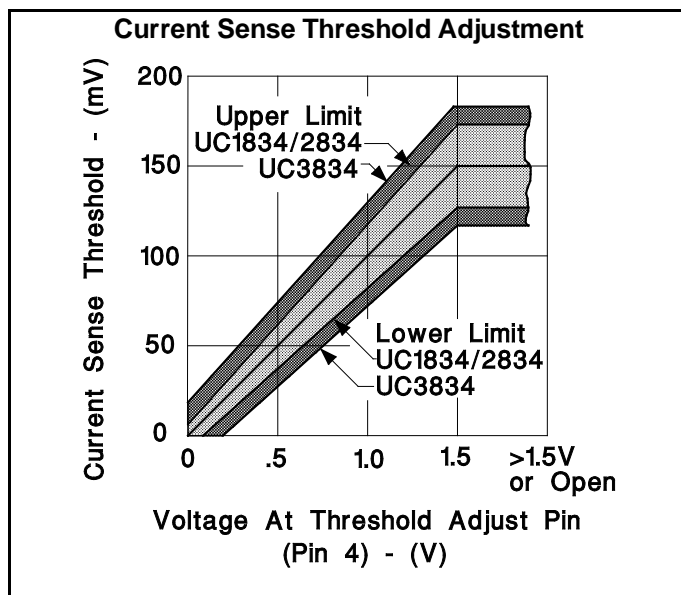
PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Turn-on Characteristics</b>								
Standby Supply Current			5.5	7		5.5	10	mA
<b>+1.5 Volt Reference</b>								
Output Voltage	$T_J = 25^{\circ}\text{C}$	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{J(\text{MIN})} \leq T_J \leq T_{J(\text{MAX})}$	1.47		1.53	1.455		1.545	
Line Regulation	$V_{IN+} = 5$ to $35\text{V}$		1	10		1	15	mV
Load Regulation	$I_{OUT} = 0$ to $2\text{mA}$		1	10		1	15	mV
<b>-2.0 Volt Reference (Note 2)</b>								
Output Voltage (Referenced to $V_{IN+}$ )	$T_J = 25^{\circ}\text{C}$	-2.04	-2	-1.96	-2.06	-2	-1.94	V
	$T_{J(\text{MIN})} \leq T_J \leq T_{J(\text{MAX})}$	-2.06		-1.94	-2.08		-1.92	
Line Regulation	$V_{IN+} = 5$ to $35\text{V}$		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		k $\Omega$
<b>Error Amplifier Section</b>								
Input Offset Voltage	$V_{CM} = 1.5\text{V}$		1	6		1	10	mV
Input Bias Current	$V_{CM} = 1.5\text{V}$		-1	-4		-1	-8	$\mu\text{A}$
Input Offset Current	$V_{CM} = 1.5\text{V}$		0.1	1		0.1	2	$\mu\text{A}$
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = $V_{IN+}$ Pin 13, $20\Omega$ to $V_{IN-}$	50	65		50	65		dB
CMRR	$V_{CM} = 0.5$ to $33\text{V}$ , $V_{IN+} = 35\text{V}$	60	80		60	80		dB
PSRR	$V_{IN+} = 5$ to $35\text{V}$ , $V_{CM} = 1.5\text{V}$	70	100		70	100		dB
<b>Driver Section</b>								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	$I_{OUT} = 100\text{mA}$		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = $35\text{V}$ , Pin 13 = $V_{IN-}$ , Pin 14 = $V_{IN-}$		0.1	50		0.1	50	$\mu\text{A}$
Shutdown Input Voltage at Pin 14	$I_{OUT} \leq 100\mu\text{A}$ , Pin 13 = $V_{IN-}$ , Pin 12 = $V_{IN+}$	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = $V_{IN-}$ , Pin 12 = $V_{IN+}$ $I_{OUT} \leq 100\mu\text{A}$ , Pin 13 = $V_{IN-}$		-100	-150		-100	-150	$\mu\text{A}$
Thermal Shutdown (Note 3)			165			165		$^{\circ}\text{C}$
<b>Fault Amplifier Section</b>								
Under- and Over-Voltage Fault Threshold	$V_{CM} = 1.5\text{V}$ , @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	$V_{IN+} = 35\text{V}$ , $V_{CM} = 1.5$ to $33\text{V}$		-0.4	-0.8		-0.4	-1.0	%/v
Supply Sensitivity	$V_{CM} = 1.5\text{V}$ , $V_{IN+} = 5$ to $35\text{V}$		-0.5	-1.0		-0.5	-1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/ $\mu\text{F}$
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	$I_{OUT} = 1\text{mA}$		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	$I_{OUT} = 1\text{mA}$		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		-100	-175		-100	-175		mA
Crowbar Gate Leakage Current	$V_{IN+} = 35\text{V}$ , Pin 16 = $V_{IN-}$		-0.5	-50		-0.5	-50	$\mu\text{A}$

Note 2: When using both the 1.5V and -2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The -2.0V output will change -2.3mV per  $\mu\text{A}$  of imbalance.

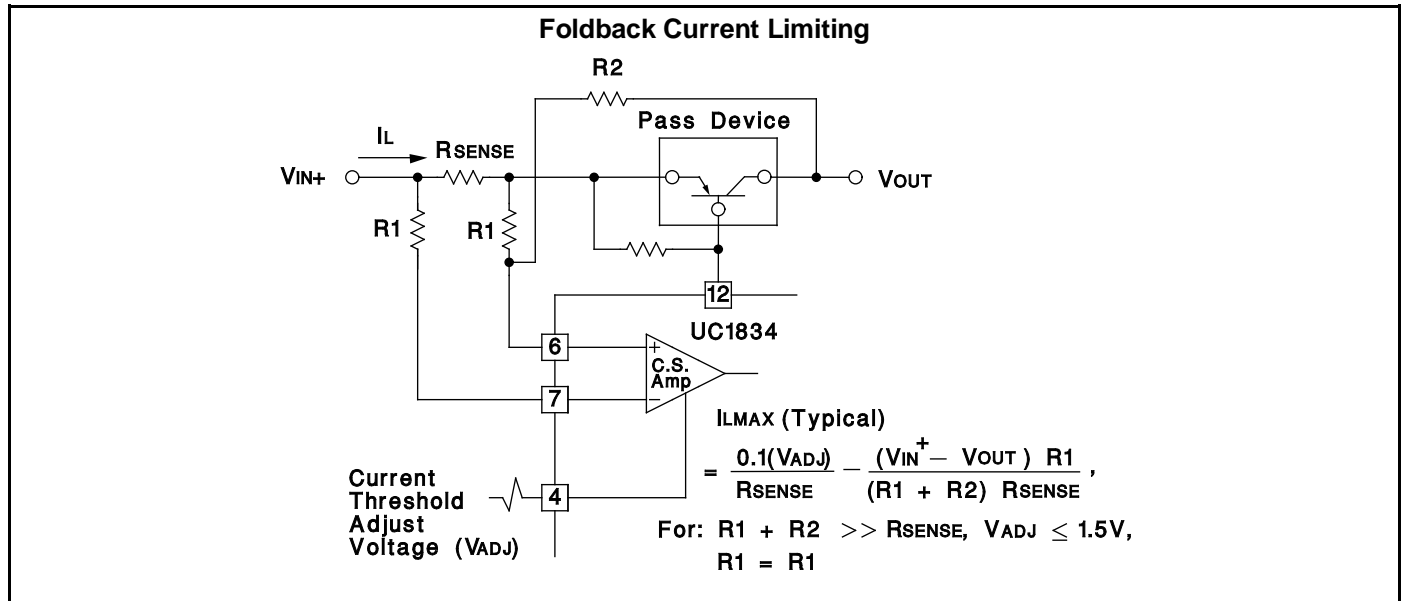
Note 3: Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown) the O.V. Latch will be reset.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1834,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2834, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3834.  $V_{IN+} = 15\text{V}$ ,  $V_{IN-} = 0\text{V}$ .  $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Current Sense Amplifier Section</b>								
Threshold Voltage	Pin 4 Open, $V_{CM} = V_{IN+}$ or $V_{IN-}$	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, $V_{CM} = V_{IN+}$ or $V_{IN-}$	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, $V_{CM} = V_{IN-}$ , $V_{IN+} = 5$ to $35\text{V}$		-0.1	-0.3		-0.1	-0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		-2	-10		-2	-10	$\mu\text{A}$
Sense Input Bias Current	$V_{CM} = V_{IN+}$		100	200		100	200	$\mu\text{A}$
	$V_{CM} = V_{IN-}$		-100	-200		-100	-200	



APPLICATION INFORMATION



Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V C.S./A} = \frac{Z_L(f)}{70\Omega}$$

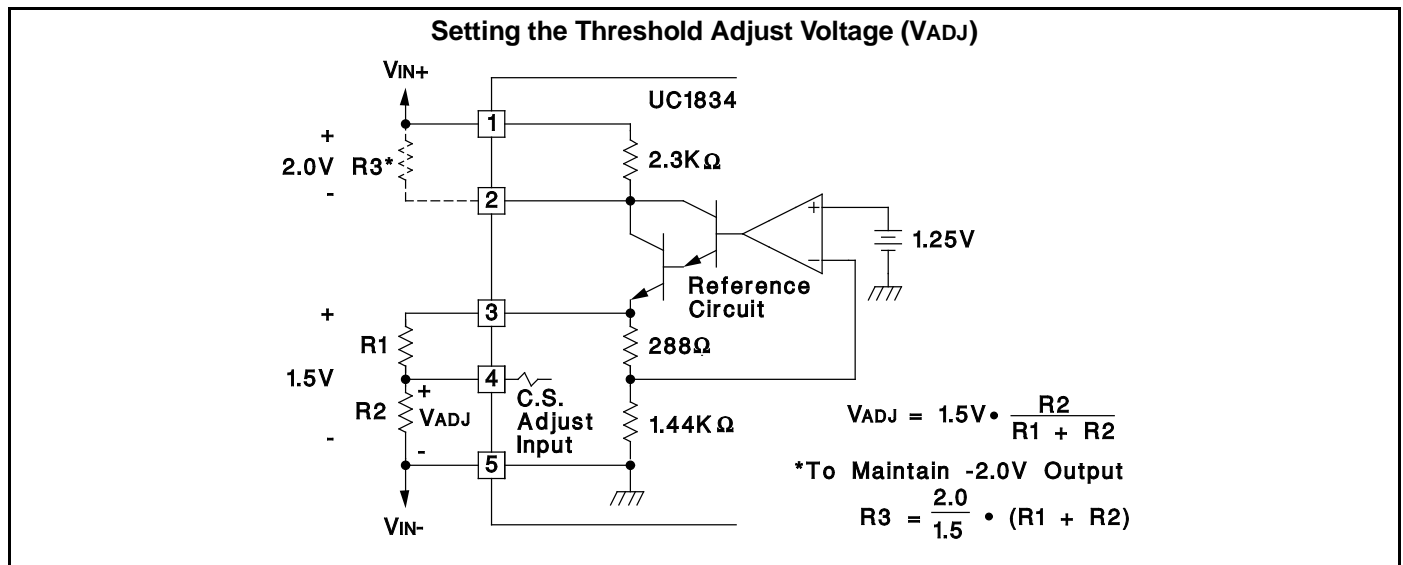
for:  $f \leq 500kHz$  and  $|Z_L(f)| \leq 1 M\Omega$

Where:

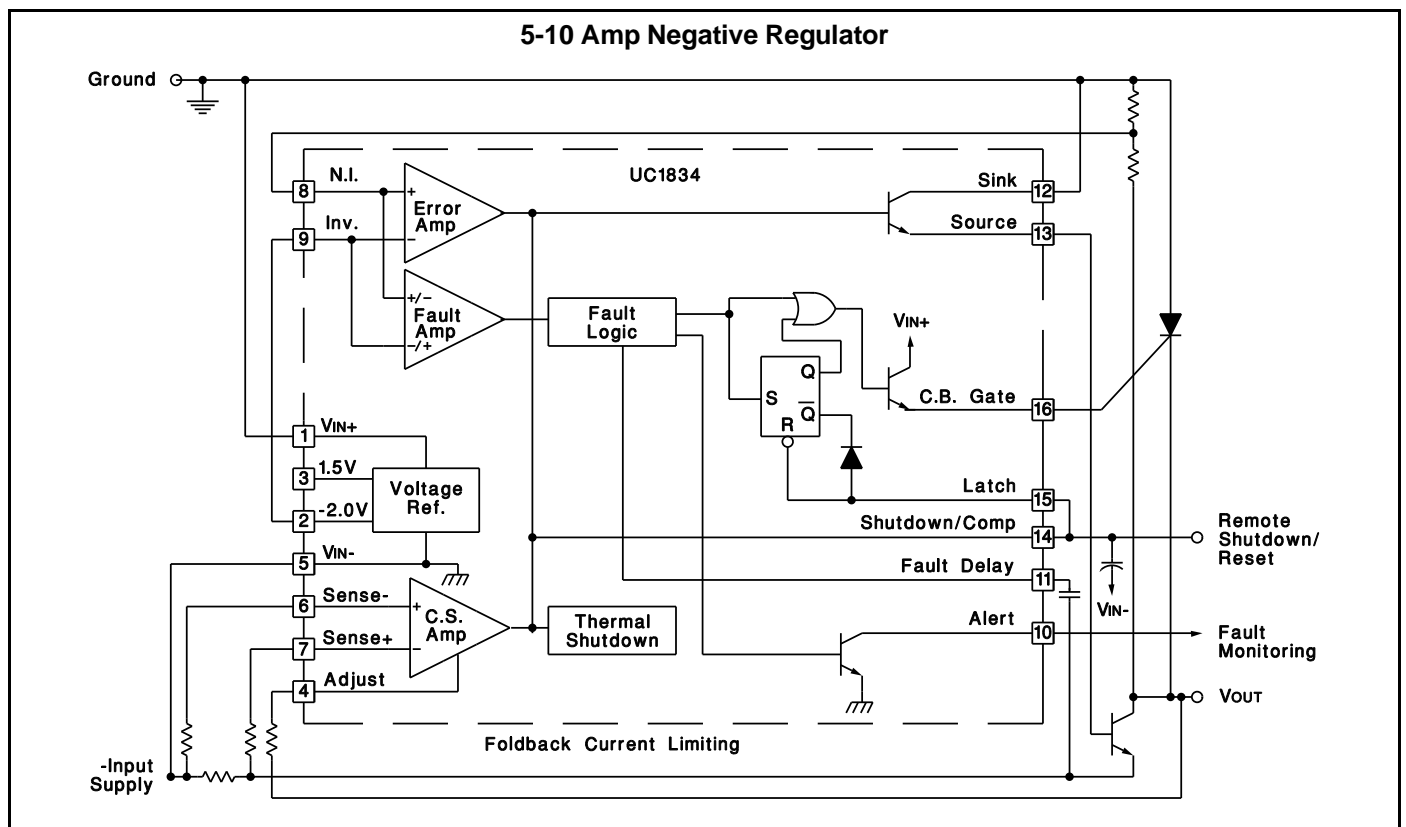
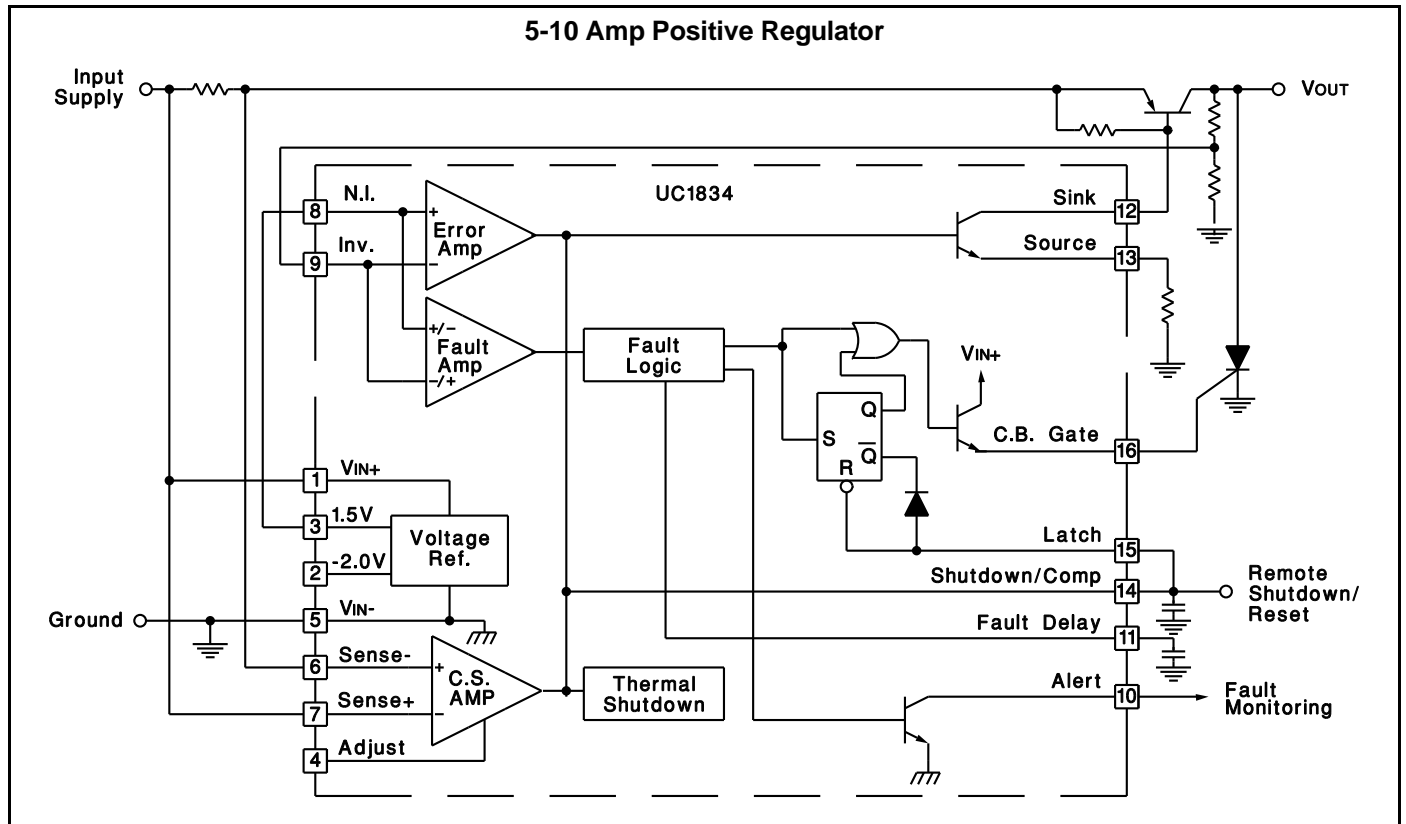
- $A_v$  = Small Signal Voltage Gain to pin 14.
- $Z_L(f)$  = Load Impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q- output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q- from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.



TYPICAL APPLICATIONS



## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.



**TEXAS INSTRUMENTS**

**THE WORLD LEADER IN DSP AND ANALOG**

Advanced Search
TI Home
TI&ME
Employment

Tech Support
Comments
Site Map
TI Global

Power Management

Power Management Home

> > [Power Management](#) > [Linear Regulation](#) > [Low Dropout \(LDO\) Controllers](#)



## UC2834, HIGH EFFICIENCY LINEAR REGULATOR

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)

Parameter Name	UC2834
I <sub>q</sub> (typ) (mA)	5.5
V <sub>in</sub> (max) (V)	40
Tolerance (%)	4
Shutdown	Yes
V <sub>O</sub> (min) (V)	1.5
I <sub>drive</sub> (max) (mA)	200
Type of Short Circuit Limit	Foldback

### Description



The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.



## Features

- Minimum  $V_{IN} - V_{OUT}$  Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

## Datasheets

Full datasheet in Acrobat PDF: [slus363.pdf](#) (657 KB)

## Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
UC2834DW	<a href="#">DW</a>	16	-40 TO 85	ACTIVE	9.30	1		<a href="#">Check stock or order</a>
UC2834DWTR	<a href="#">DW</a>	16	-40 TO 85	ACTIVE	8.10	1		<a href="#">Check stock or order</a>
UC2834J	<a href="#">J</a>	16	-40 TO 85	ACTIVE	9.69	1		<a href="#">Check stock or order</a>
UC2834N	<a href="#">N</a>	16	-40 TO 85	ACTIVE	8.64	1		<a href="#">Check stock or order</a>
UC2834Q	<a href="#">FN</a>	20	-40 TO 85	ACTIVE	9.30	1		<a href="#">Check stock or order</a>
UC2834QTR	<a href="#">FN</a>	20		ACTIVE	8.10	1		<a href="#">Check stock or order</a>

## Application Reports

- [ELECTROSTATIC DISCHARGE APPLICATION NOTE \(SSYA008 - Updated: 05/05/1999\)](#)
- [POWERFLEX \(TM\) -- SURFACE-MOUNT ALTERNATIVE FOR THROUGH-HOLE POWER PACKAGES \(SZZA015 - Updated: 05/09/1999\)](#)
- [SUPPLY VOLTAGE DROP ON FAST CURRENT DEMAND \(SLVA076 - Updated: 09/15/1999\)](#)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS \(SZZA017A - Updated: 09/10/1999\)](#)
- [VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY \(SLUA062 - Updated: 11/04/1999\)](#)

**Table Data Updated on: 8/11/2000**