

# SN74LV373A-Q1 Octal Transparent D-Type Latch With 3-State Outputs

## 1 Features

- Qualified for automotive applications
- $V_{CC}$  operation of 2 V to 5.5 V
- Maximum tpd of 8.5 ns at 5 V
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports mixed-mode voltage operation on all ports
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- [Synchronize digital signals to clock](#)
- [Use fewer inputs to monitor signals](#)
- [Convert a switch to a toggle](#)

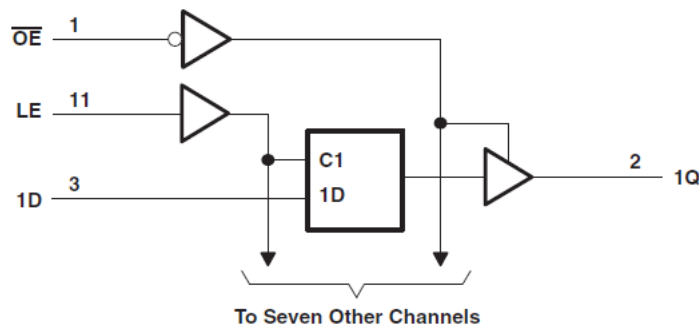
## 3 Description

The SN74LV373A-Q1 device is an octal transparent D-type latch designed for 2 V to 5.5 V  $V_{CC}$  operation. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV373A-Q1	PW (TSSOP, 20)	6.50 mm × 4.40 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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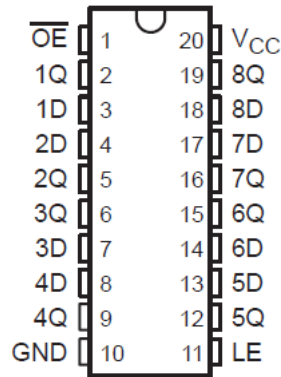
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (October 2007) to Revision D (March 2023)</b>	<b>Page</b>
• Added <i>Applications</i> , <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	<b>1</b>
• Updated thermal values for PW package from R0JA = 83 to 128.2, all values in °C/W .....	<b>5</b>

## 5 Pin Configuration and Functions



**Figure 5-1. SN74LV373A-Q1 TSSOP -PW Package (Top View)**

**Table 5-1. Pin Function**

PIN		TYPE	DESCRIPTION
NAME	NO.		
OE	1	Input	Output enable, active low
1Q	2	Output	Output for channel 1
1D	3	Input	Input for channel 1
2D	4	Input	Input for channel 2
2Q	5	Output	Output for channel 2
3Q	6	Output	Output for channel 3
3D	7	Input	Input for channel 3
4D	8	Input	Input for channel 4
4Q	9	Output	Output for channel 4
GND	10	—	Ground
LE	11	Input	Latch enable
5Q	12	Output	Output for channel 5
5D	13	Input	Input for channel 5
6D	14	Input	Input for channel 6
6Q	15	Output	Output for channel 6
7Q	16	Output	Output for channel 7
7D	17	Input	Input for channel 7
8D	18	Input	Input for channel 8
8Q	19	Output	Output for channel 8
V <sub>CC</sub>	20	—	Positive supply
Thermal Pad <sub>1</sub>		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5	7	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V	
V <sub>O</sub>	Output voltage <sup>(2)</sup> <sup>(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35	mA
	Continuous current through V <sub>CC</sub> or GND			±70	mA
θ <sub>JA</sub>	Package thermal impedance			83	°C/W
T <sub>stg</sub>	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The package thermal impedance is calculated in accordance with JESD 51-7.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±4000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000
			V

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		–50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		–2	
		V <sub>CC</sub> = 3 V to 3.6 V		–8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		–16	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	
		V <sub>CC</sub> = 3 V to 3.6 V		8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV373A-Q1	UNIT
		PW (TSSOP)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	128.2	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V to 5.5 V	V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			
	I <sub>OH</sub> = –8 mA	3 V	2.48			
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4	
	I <sub>OL</sub> = 8 mA	3 V			0.44	
	I <sub>OL</sub> = 16 mA	4.5 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V			5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		2.9		pF

## 6.6 Timing Requirements, 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

			MIN	MAX	UNIT
t <sub>w</sub>	Pulse duration, LE high		6.5		ns
t <sub>su</sub>	Setup time, data before LE↓	High or low	5		ns
t <sub>h</sub>	Hold time, data after LE↓	High or low	1.5		ns

## 6.7 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

			MIN	MAX	UNIT
t <sub>w</sub>	Pulse duration, LE high		5		ns
t <sub>su</sub>	Setup time, data before LE↓	High or low	4		ns
t <sub>h</sub>	Hold time, data after LE↓	High or low	1		ns

## 6.8 Timing Requirements, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

			MIN	MAX	UNIT
t <sub>w</sub>	Pulse duration, LE high		5		ns
t <sub>su</sub>	Setup time, data before LE↓	High or low	4		ns
t <sub>h</sub>	Hold time, data after LE↓	High or low	1		ns

## 6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	2.5 V ± 0.2 V		3.3 V ± 0.3 V		5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	C <sub>L</sub> = 15 pF	1	17	1	13.5	1	8.5	ns
	LE	Q		1	19	1	13	1	8.5	
t <sub>en</sub>	$\overline{OE}$	Q		1	19	1	13.5	1	9.5	ns
t <sub>dis</sub>	$\overline{OE}$	Q		1	15	1	12	1	8.5	ns

over operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	2.5 V ± 0.2 V		3.3 V ± 0.3 V		5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	C <sub>L</sub> = 50 pF	1	21	1	17	1	10.5	ns
	LE	Q		1	22	1	16.5	1	10.5	
t <sub>en</sub>	$\overline{OE}$	Q		1	22	1	17	1	11.5	ns
t <sub>dis</sub>	$\overline{OE}$	Q		1	19	1	15	1	10.5	ns
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF	2		1.5		1		ns

## 6.10 Noise Characteristics

V<sub>CC</sub> = 3.3 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER <sup>(1)</sup>		SN74LV373A-Q1			UNIT
		MIN	TYP	MAX	
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.6	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.6	-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		2.9		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

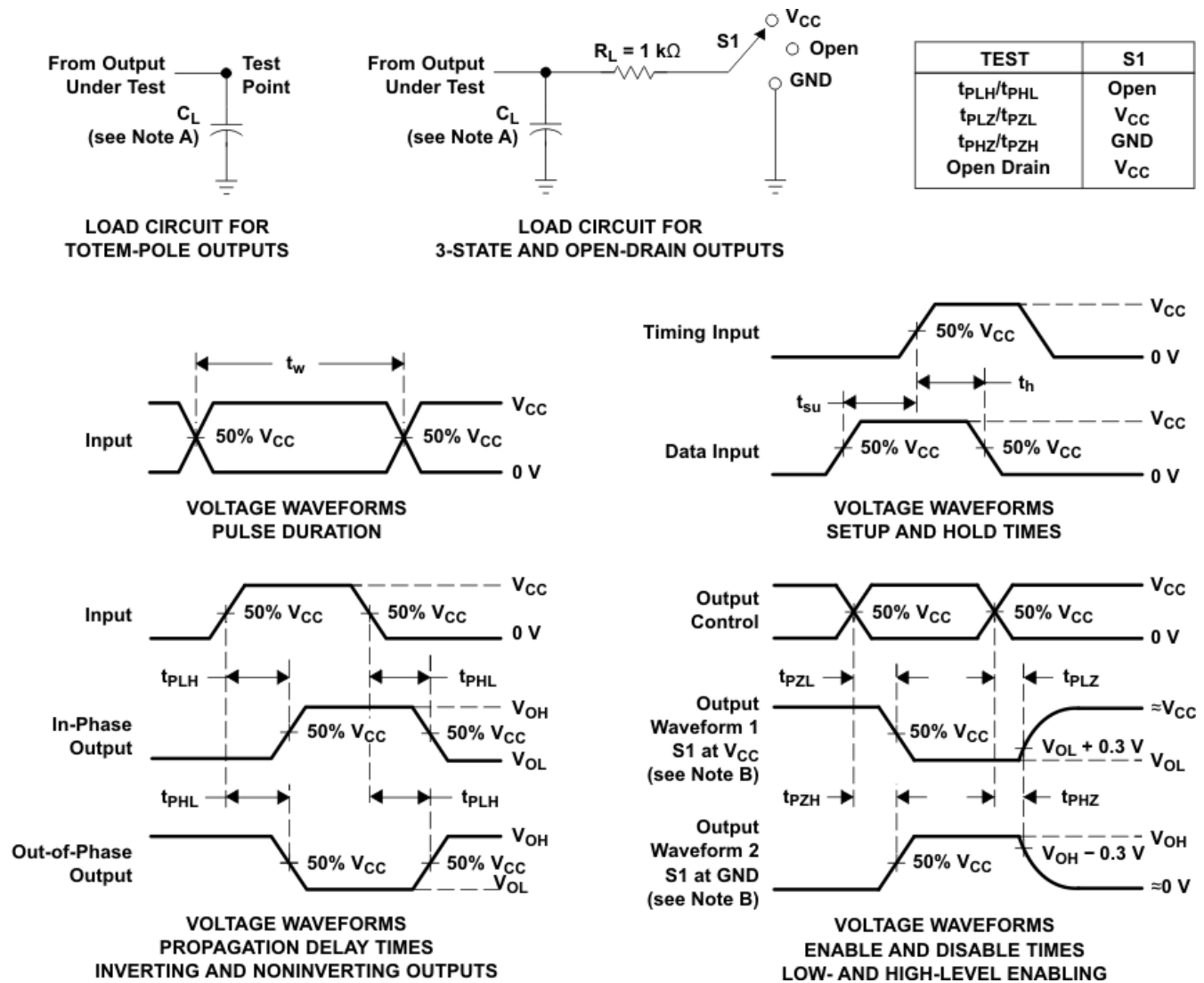
(1) Characteristics for surface-mount packages only.

## 6.11 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance (outputs enabled)	C <sub>L</sub> = 50 pF, f = 10 MHz	3.3 V	17.4	pF
			5 V	19.5	

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns, and  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram

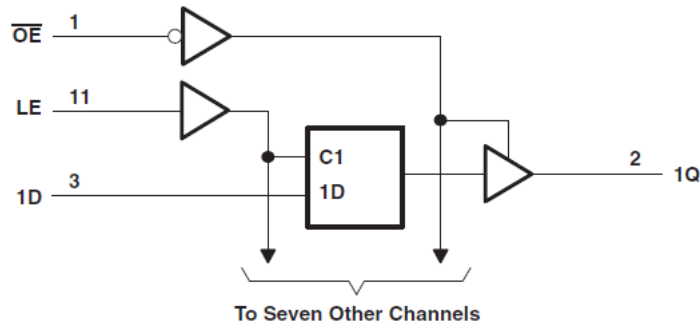


Figure 8-1. Logic Diagram (Positive Logic)

### 8.3 Device Functional Modes

**Table 8-1. Function Table**

INPUTS <sup>(1)</sup>			OUTPUT <sup>(2)</sup>
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	L, H, ↓	X	Q <sub>0</sub>
H	↑	L	L
H	↑	H	H

- (1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = do not care  
 (2) L = output low, H = output high, Q<sub>0</sub> = previous state

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu\text{F}$  capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

### 9.2 Layout

#### 9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

##### 9.2.1.1 Layout Example

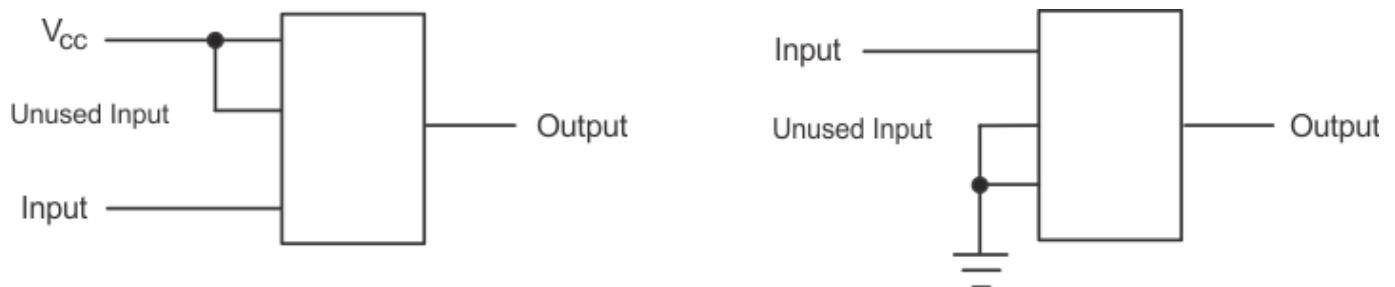


Figure 9-1. Layout Diagram

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV373A-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV373AIPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV373AI	Samples
SN74LV373AIPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LV373AI	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV373A-Q1 :**

- Catalog : [SN74LV373A](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV373AIPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV373AIPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0



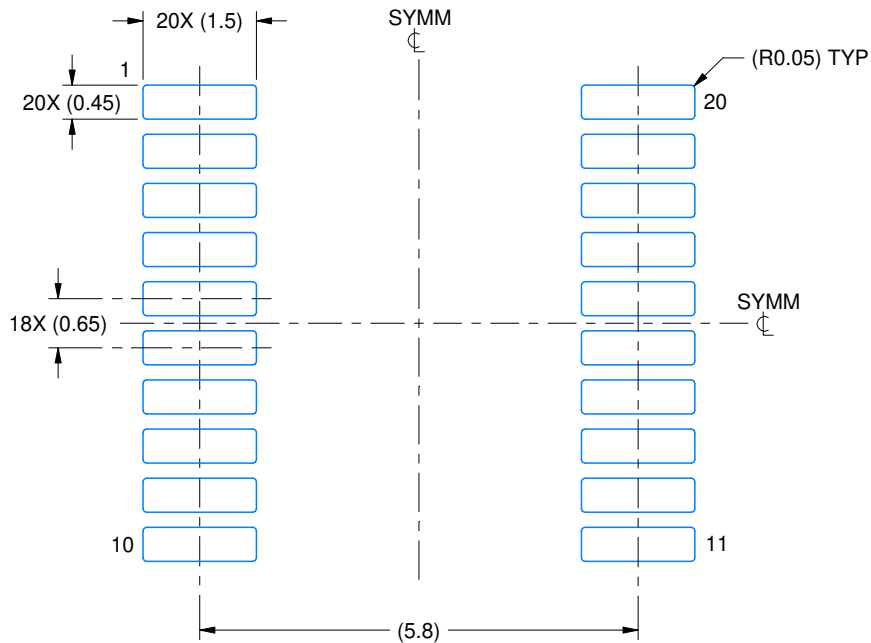


# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

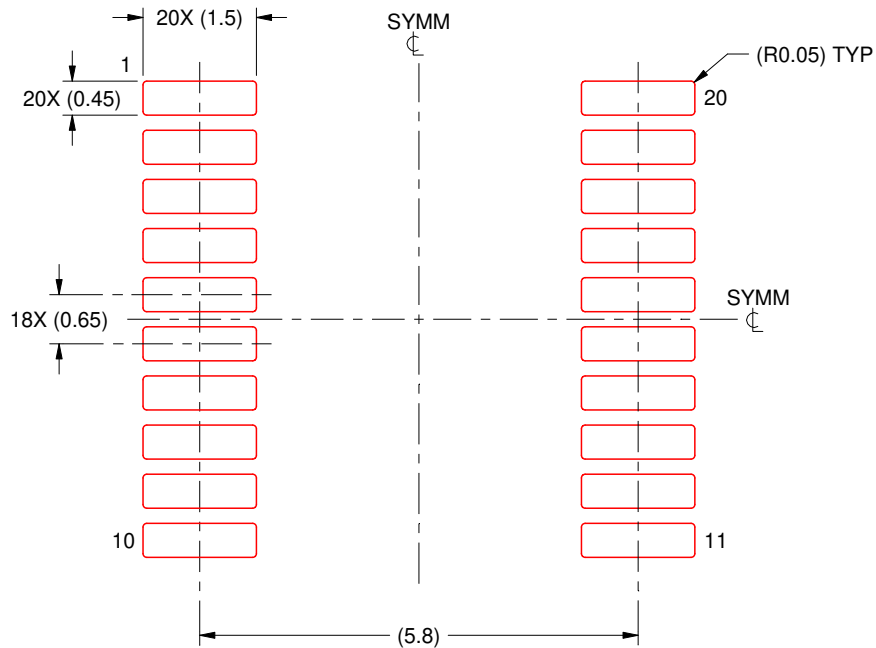
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

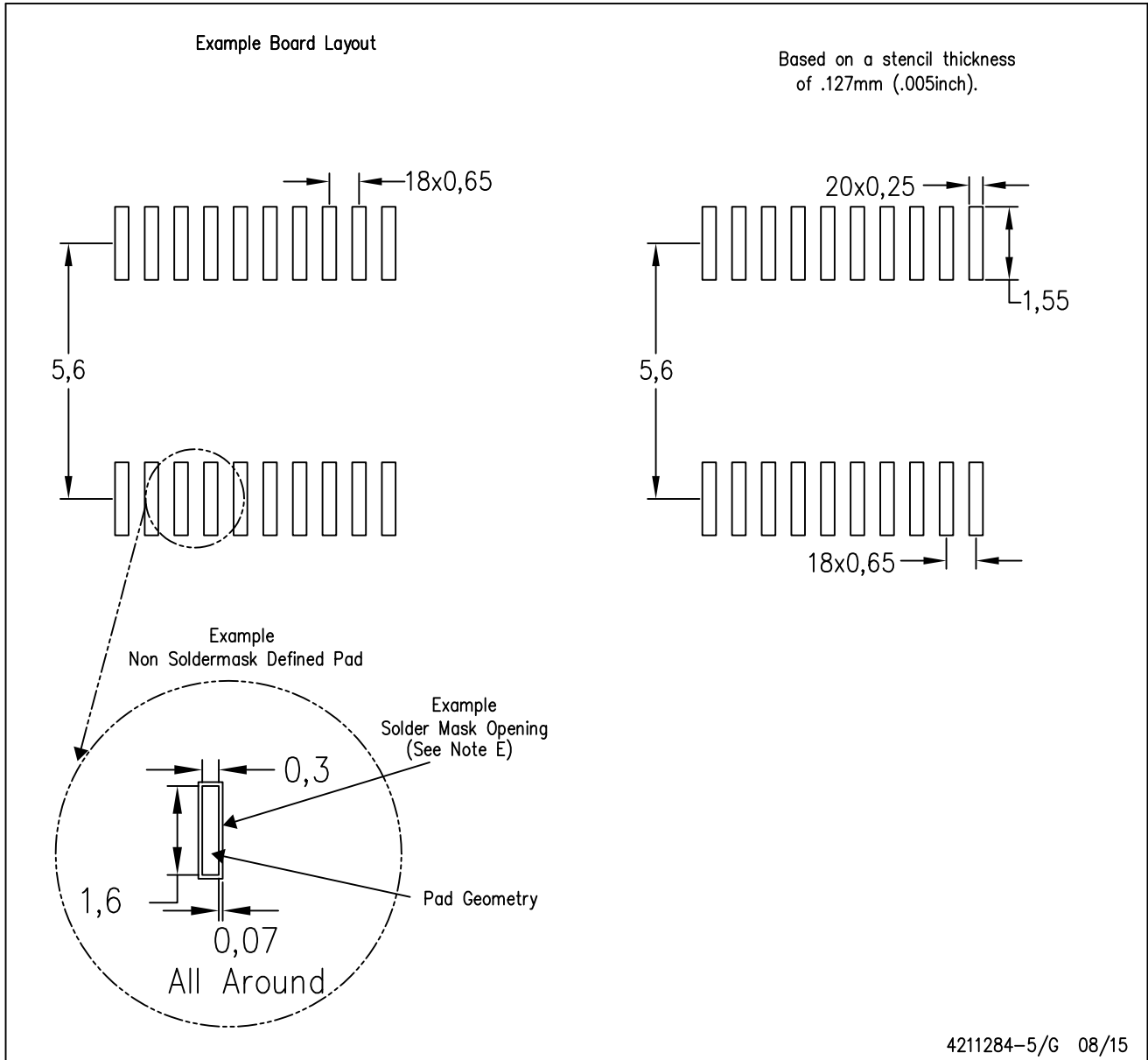
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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