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MOSFET – Single N-Channel, SUPERFET® III, FRFET®

650 V, 46 A, 65 mΩ

NVHL065N65S3F

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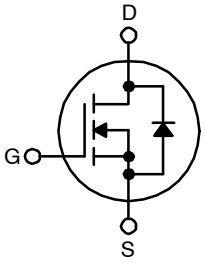
Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on)\ max.}$ x $Q_{g\ typ.}$ & $R_{DS(on)\ max.}$ x E_{OSS})
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	65 mΩ @ 10 V	46 A



POWER MOSFET

TO−247−3LD
CASE 340CH

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	650	V
Gate−to−Source Voltage − DC	V_{GSS}	±30	V
Gate−to−Source Voltage − AC (f > 1 Hz)	V_{GSS}	±30	V
Drain Current − Continuous (T_C = 25°C)	I_D	46	A
Drain Current − Continuous (T_C = 100°C)	I_D	30	A
Drain Current − Pulsed (Note 3)	I_{DM}	115	A
Power Dissipation (T_C = 25°C)	P_D	337	W
Power Dissipation − Derate Above 25°C	P_D	2.7	W/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	635	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	3.37	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8″ from case for 5 s)	T_L	300	°C

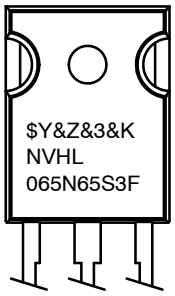
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.37	°C/W
Thermal Resistance, Junction−to−Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse−width limited by maximum junction temperature.
4. I_{AS} = 9 A, R_G = 25 Ω, starting T_J = 25°C.
5. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
NVHL065N65S3F	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVHL065N65S3F	TO−247−4LD (Pb−Free)	30 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D = 15 mA, Referenced to 25°C		630		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		153		
Gate−to−Body Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1.3 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 1.3 mA		−8.6		mV/°C
Static Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 23 A		54	65	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 23 A		31		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz		4075		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			11		
Effective Output Capacitance	$C_{oss(eff.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		876		pF
Energy Related Output Capacitance	$C_{oss(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		160		pF
Total Gate Charge at 10 V	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 23 A (Note 6)		98		nC
Gate−to−Source Gate Charge	Q_{GS}			30		
Gate−to−Drain “Miller” Charge	Q_{GD}			38		
Equivalent Series Resistance	ESR	f = 1 MHz		1.5		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 400 V, I_D = 23 A, R_g = 2.7 Ω (Note 6)		34		ns
Turn-On Rise Time	t_r			31		ns
Turn-Off Delay Time	$t_{d(off)}$			78		ns
Turn-Off Fall Time	t_f			16		ns
SOURCE−DRAIN DIODE CHARACTERISTICS						
Maximum Continuous Source−to−Drain Diode Forward Current	I_S	V_{GS} = 0 V			46	A
Maximum Pulsed Source−to−Drain Diode Forward Current	I_{SM}	V_{GS} = 0 V			115	A
Source−to−Drain Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 23 A			1.3	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 100 A/μs, I_{SD} = 23 A		116		ns
Charge Time	t_a			90		
Discharge Time	t_b			24		
Reverse Recovery Charge	Q_{rr}			488		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

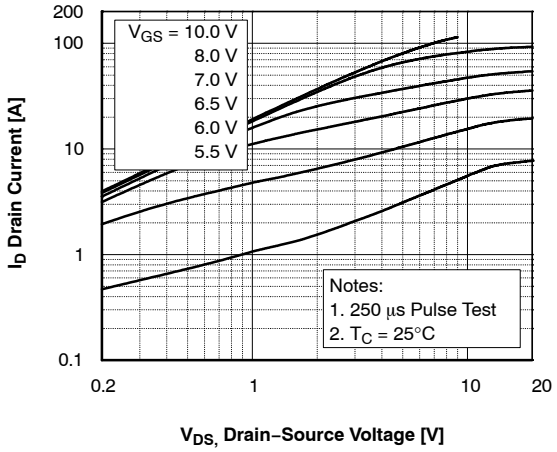


Figure 1. On−Region Characteristics

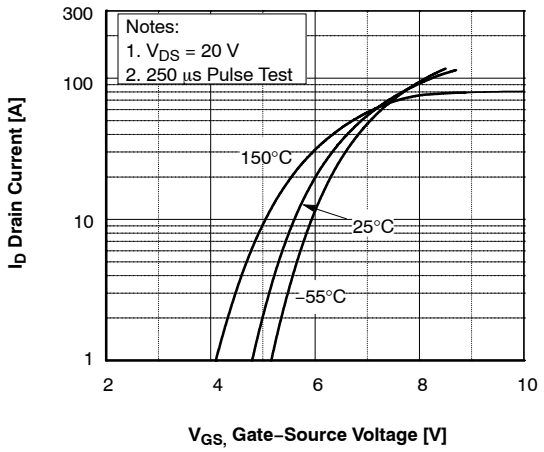


Figure 2. Transfer Characteristics

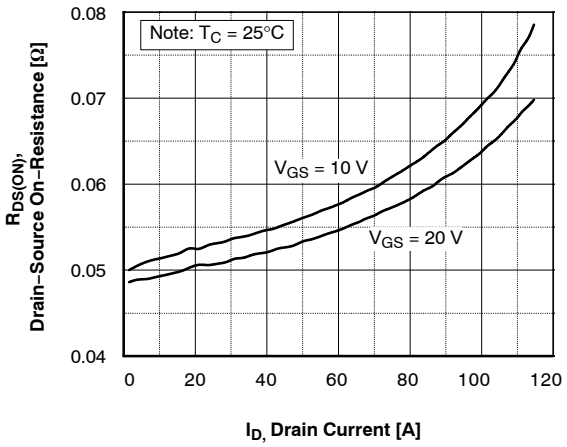


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

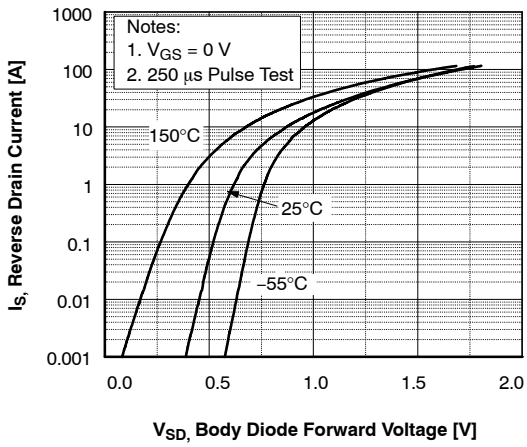


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

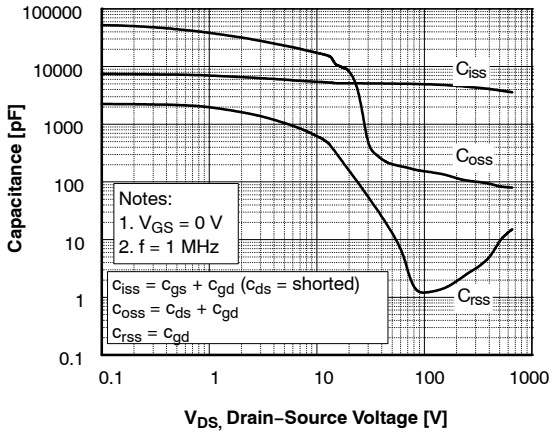


Figure 5. Capacitance Characteristics

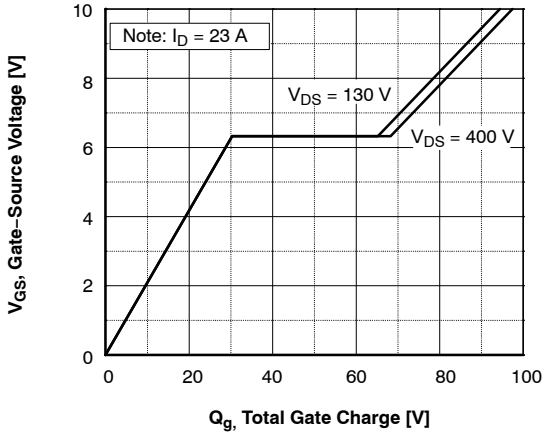


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

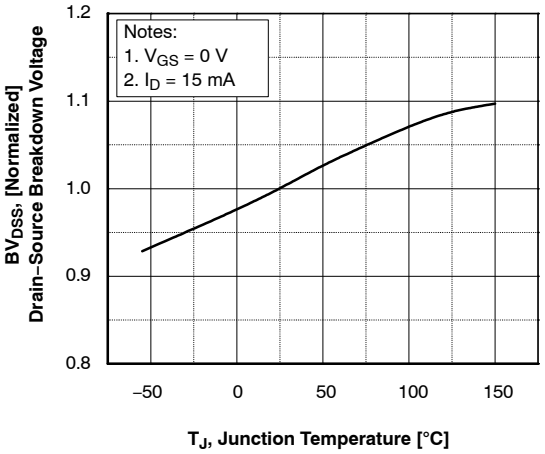


Figure 7. Breakdown Voltage Variation vs. Temperature

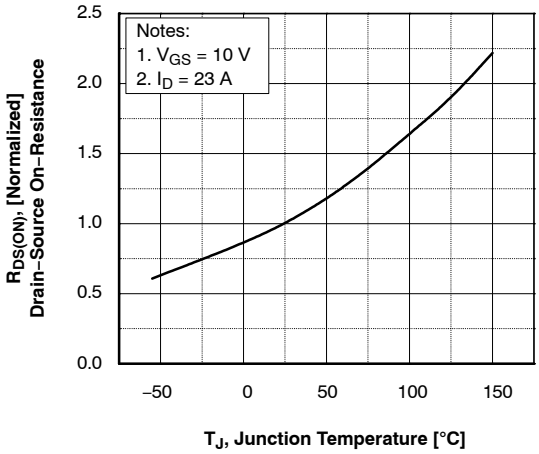


Figure 8. On−Resistance Variation vs. Temperature

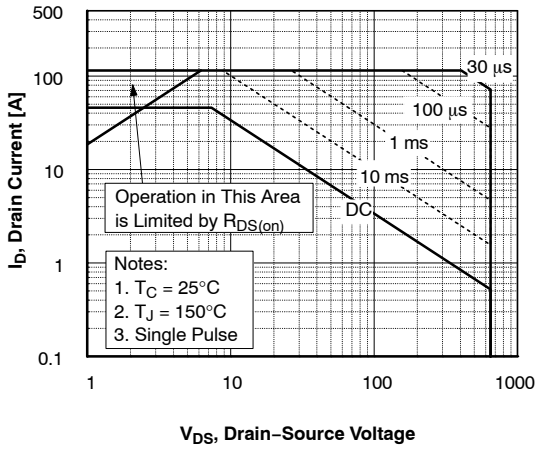


Figure 9. Maximum Safe Operating Area

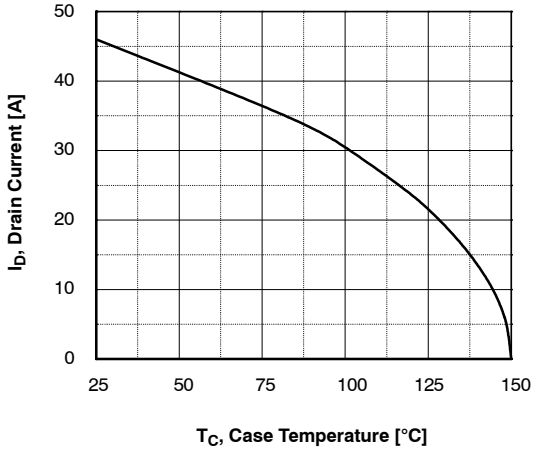


Figure 10. Maximum Drain Current vs. Case Temperature

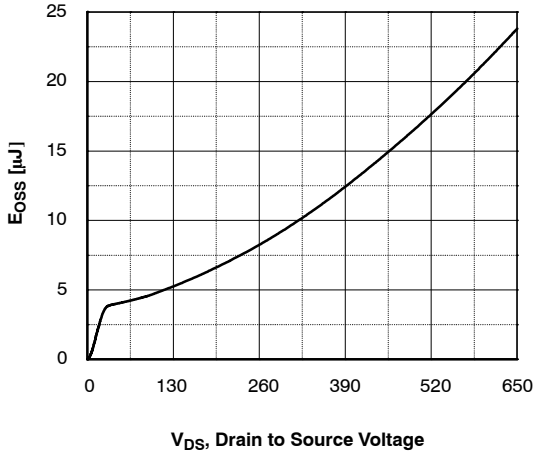


Figure 11. E_{oss} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

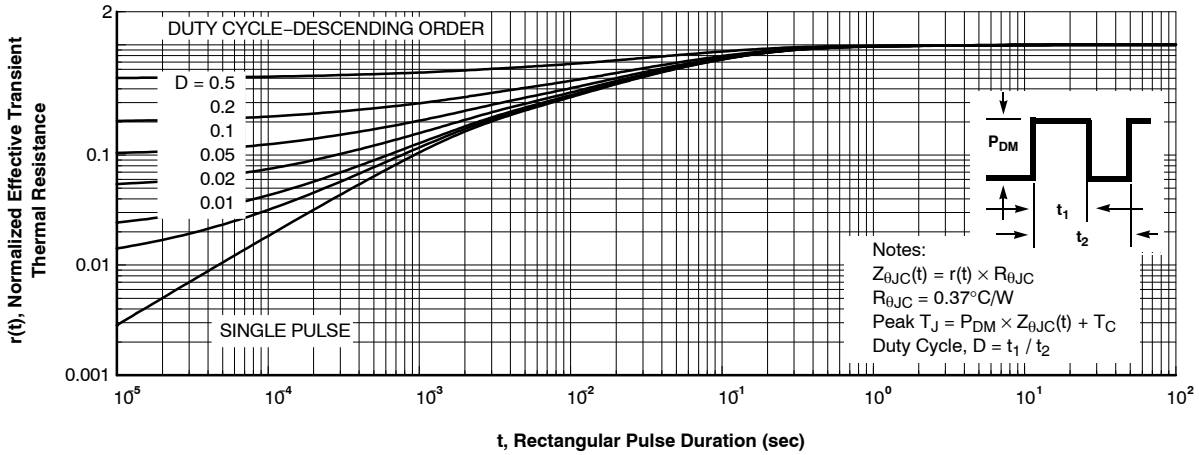


Figure 12. Transient Thermal Response Curve

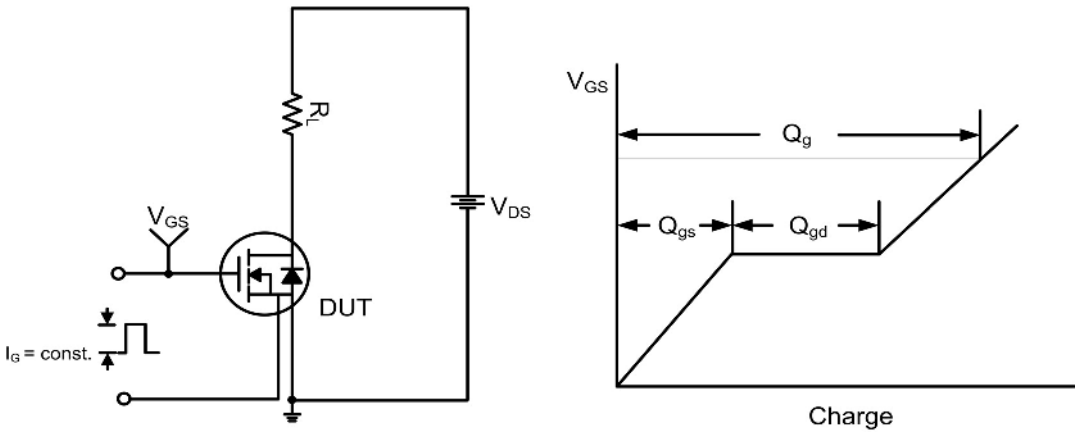


Figure 13. Gate Charge Test Circuit & Waveform

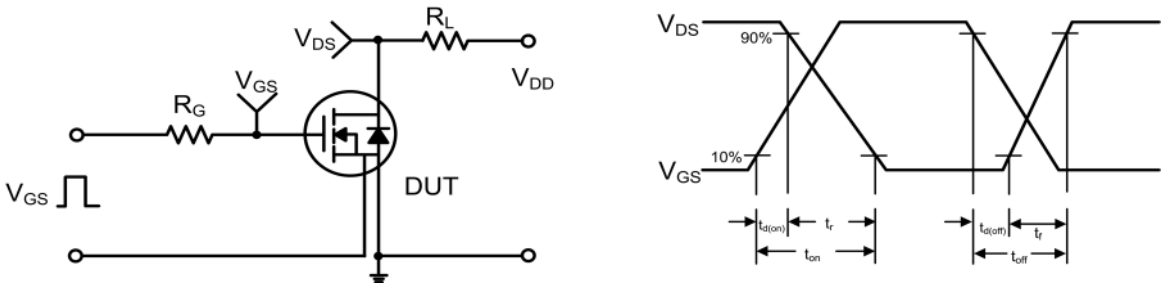


Figure 14. Resistive Switching Test Circuit & Waveforms

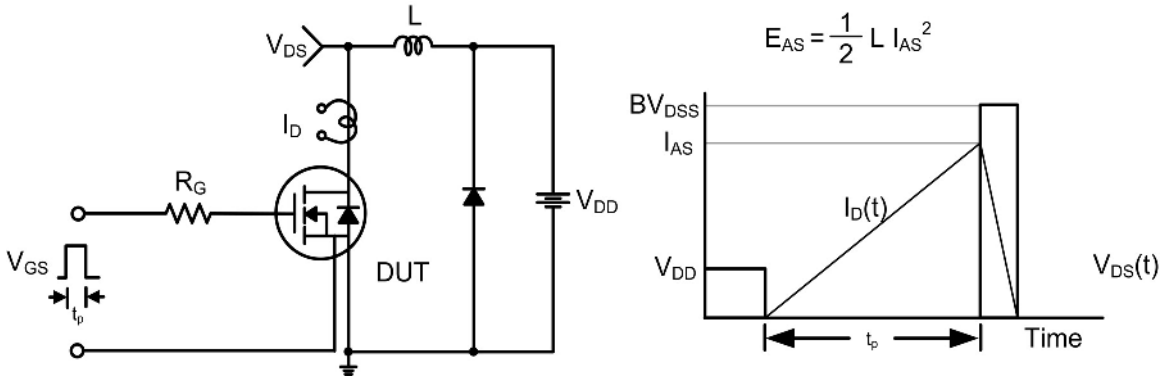


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

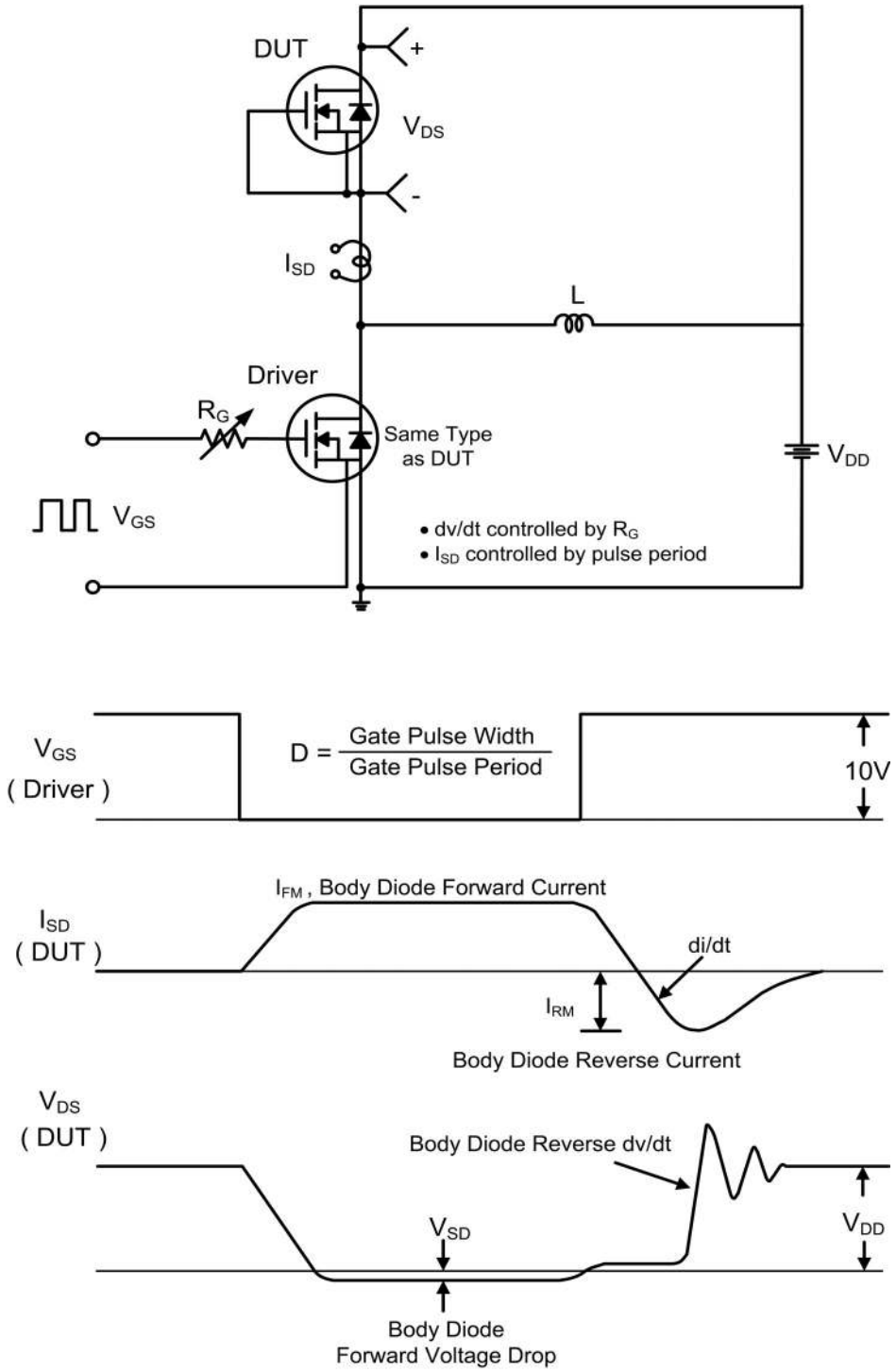
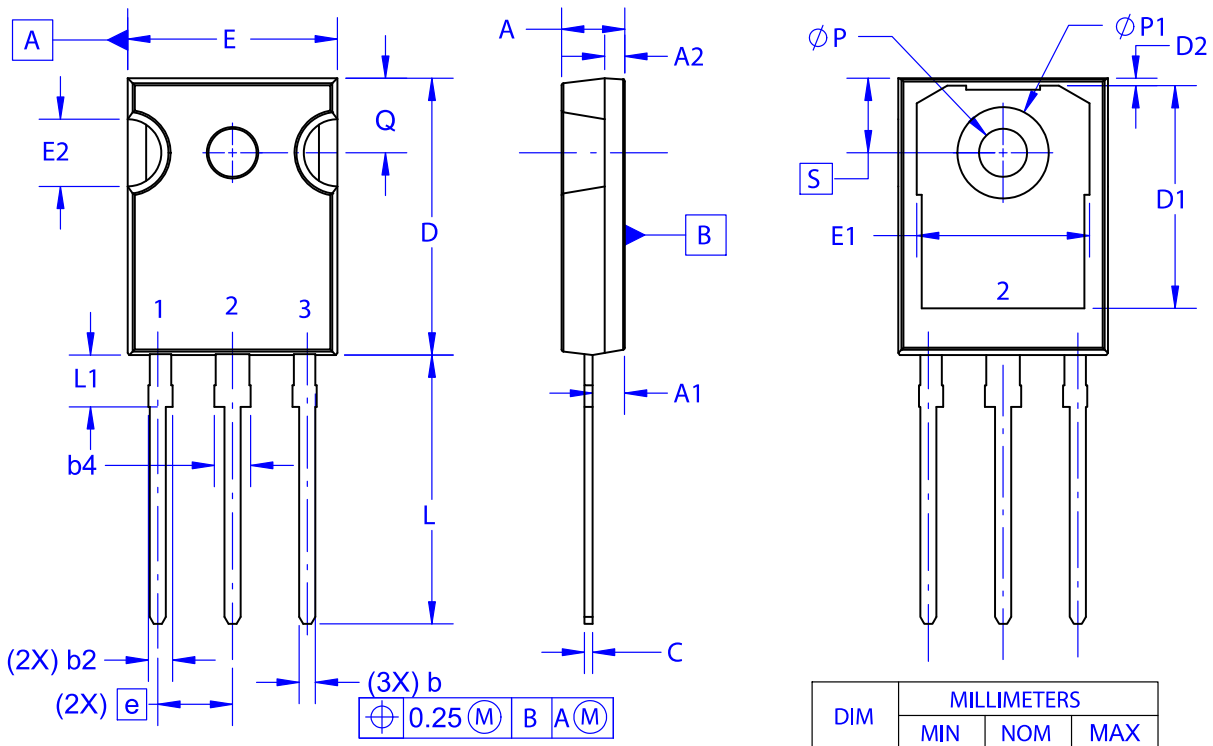


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE DIMENSIONS

TO−247−4LD
CASE 340CH
ISSUE A



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.61	6.73	6.85

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