User's Guide

TPS53513 Step-Down Converter Evaluation Module User's Guide

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1 Introduction

The TPS53513EVM-PWR587 evaluation module (EVM) uses the TPS53513 device. The TPS53513 device is a D-CAP3™ mode, 8-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.2-V output at up to 8 A from a 12-V input bus.

2 Description

The TPS53513EVM-PWR587 is designed to use a regulated 12-V bus to produce a regulated 1.2-V output at up to 8 A of load current. The TPS53513EVM-PWR587 is designed to demonstrate the TPS53513 device in a typical low voltage application while providing a number of test points to evaluate the performance of the TPS53513 device.

2.1 Typical Applications

- Server and storage
- Workstations and desktops
- Telecommunication infrastructure

2.2 Features

The TPS53513EVM- PWR587 features:

- 8-A DC steady-state output current
- Support pre-bias output voltage start-up
- J2 for enable function
- J5 for auto-skip and forced CCM selection
- J7 for extra 5-V input for further power saving purpose
- Convenient test points for probing critical waveforms

3 Electrical Performance Specifications

Table 3-1. TPS53513EVM-PWR587 Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristic					
Voltage range	V_{IN}	5	12	18	V
Maximum input current	V_{IN} = 5 V, I_O = 8 A		2.5		A
No load input current	V_{IN} = 12 V, I_O = 0 A with auto skip mode		1		mA
Output Characteristics					
Output voltage	V_{OUT}		1.2		V
Output voltage regulation	Line regulation, V_{IN} = 5 V – 14 V with FCCM		0.2%		
	Load regulation, V_{IN} = 12 V, I_O = 0 A – 8 A with FCCM		0.5%		
Output voltage ripple	V_{IN} = 12 V, I_O = 8 A with FCCM		10		mV_{PP}
Output load current		0		8	A
Output over current			11		
Soft start			1		mS
Systems Characteristics					
Switching frequency			1000		kHz
Peak efficiency	V_{IN} = 12 V, 1.2 V / 4 A		88.5%		
Full load efficiency	V_{IN} = 12 V, 1.2 V / 8 A		86.9%		
Operating temperature			25		°C

(1) Jumpers set to default locations. See Section 6.

4 Schematic

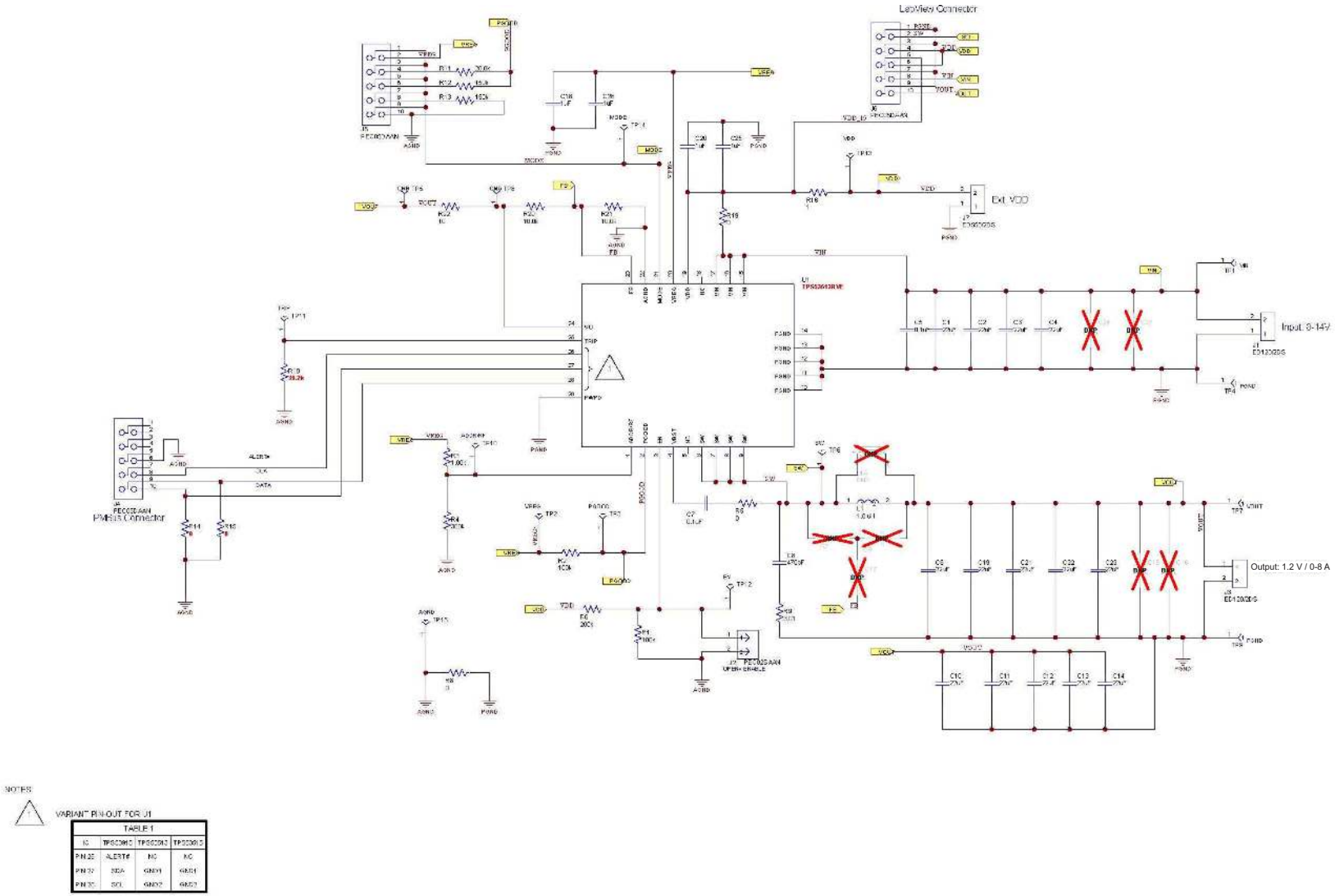

Figure 4-1. TPS53513EVM-PWR587 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source: The input voltage source V_{IN} must be a 0-V to 14-V variable DC source capable of supplying 10 A_{DC}. Connect V_{IN} to J1 as shown in Figure 5-2.

Multimeters:

- **V1:** V_{IN} at TP1 (VIN) and TP4 (GND)
- **V2:** V_{OUT} at TP7 (VOUT) and TP9 (GND)

Output Load: The output load must be an electronic constant resistance mode load capable of 15 A_{DC} at 1.2 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 1-µs/div horizontal resolution
- 20-mV/div vertical resolution

Test points TP7 and TP9 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP7 and holding the ground barrel on TP9 as shown in Figure 5-1. Using a leaded ground connection may induce additional noise due to the large ground loop.

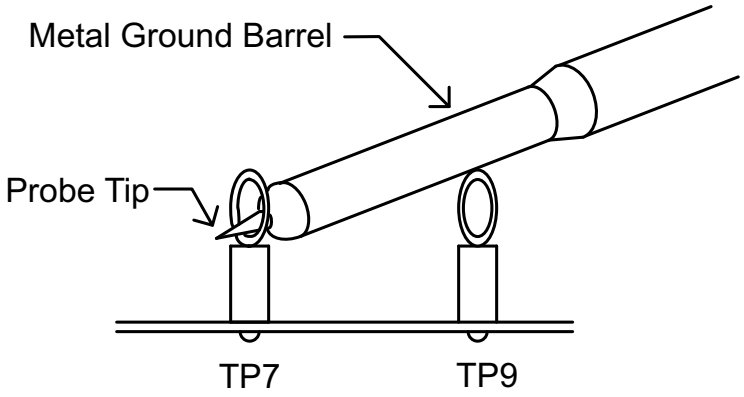

Figure 5-1. Tip and Barrel Measurement for V_{OUT} Ripple

Recommended Wire Gauge:

- **VIN to J1 (12V input):** The recommended wire size is 1× AWG #14 per input connection, with the total length of wire less than four feet (two feet input, two feet return).
- **J3 to LOAD:** The minimum recommended wire size is 2× AWG #14, with the total length of wire less than four feet (two feet output, two feet return).

5.2 Recommended Test Setup

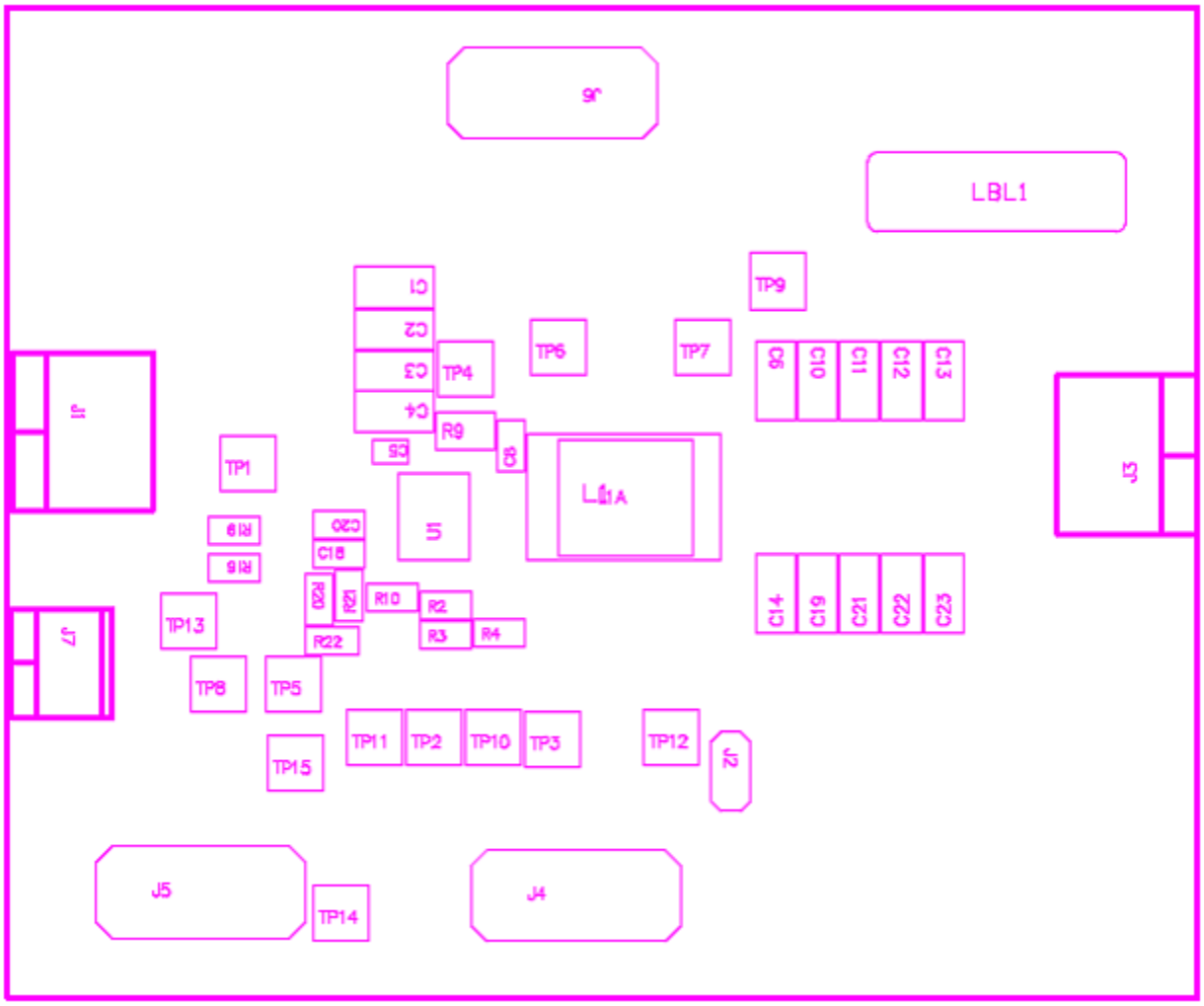

Figure 5-2. TPS53513EVM-587 Top Layer for Test Setup

5.2.1 Input Connections

1. Prior to connecting the DC input source (V_{IN}), it is advisable to limit the source current from V_{IN} to 10 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 5-2.
2. Connect a voltmeter V1 at TP1 (V_{IN}) and TP2 (GND) to measure the input voltage.

5.2.2 Output Connections

1. Connect Load to J3 and set load to constant resistance mode to sink 0 A_{DC} before V_{IN} is applied.
2. Connect a voltmeter V2 at TP7 (V_{OUT}) and TP9 (GND) to measure the output voltage.

6 Configurations

All jumper selections should be made prior to applying power to the EVM. The user can configure this EVM per the following configurations.

6.1 Switching Frequency Selection

Switching frequency can be changed according to Table 6-1.

Default setting: 1 MHz

Table 6-1. Switching Frequency

SWITCHING FREQUENCY (F_{SW})(KHZ)	RESISTOR DIVIDER RATIO (R_{DR})	EXAMPLE RF FREQUENCY COMBINATIONS	
		R_{RF_H} (kΩ)	R_{RF_L} (kΩ)
1000	> 0.557	1	300
850	0.461	180	154
750	0.375	200	120
600	0.297	249	105
500	0.229	240	71.5
400	0.16	249	47.5
300	0.096	255	27
250	< 0.041	270	11.5

For different switching frequency settings, change R3 and R4 according to Table 6-1.

6.2 Mode Selection

The MODE can be set by J5.

Default setting: FCCM

Table 6-2. MODE Selection

JUMPERS SET TO:	MODE SELECTION
1-2 pin shorted	FCCM with 2× RC time constant
3-4 pin shorted	**Forced CCM(1) with 1× RC time constant**
5-6 pin shorted	Forced CCM(1) with 2× RC time constant
7-8 pin shorted	Auto-Skip Mode with 2× RC time constant
9-10 pin shorted	Auto-Skip Mode with 1× RC time constant

(1) Device goes into FCCM after PGOOD becomes high.

6.3 VDD Pin Supply Selection

The controller can be enabled and disabled by J7.

Default setting: VDD pin connected to VIN pins through R19

Table 6-3. The Controller Can Be Enabled and Disabled by J7(1)

SET ON CONNECTION	ENABLE SELECTION
R19 = 0 Ω	VDD pin connected to VIN pins
R19 = Open	VDD pin disconnected to VIN pins

(1) J7 requires the proper input voltage for power up. The VDD pin input voltage range is from 4.5 V to 25 V.

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in Section 5 and Figure 5-2.
2. Ensure the load is set to constant resistance mode and to sink 0 A_{DC}.
3. Ensure all jumpers set per Section 6.
4. Ensure the jumper provided in the EVM shorts on J2 before V_{IN} is applied.
5. Increase V_{IN} from 0 V to 12 V. Using V1 to measure input voltage.
6. Remove the jumper on J2 to enable the controller.
7. Use V2 to measure V_{OUT} voltage.
8. Vary load from 0 A_{DC} to 10 A_{DC}, V_{OUT} must remain in load regulation.
9. Vary V_{IN} from 8 V to 14 V, V_{OUT} must remain in line regulation.
10. Put the jumper on J2 to disable the converter.
11. Decrease load to 0 A.
12. Decrease V_{IN} to 0 V.

7.2 Control Loop Gain and Phase Measurement Procedure

The TPS53513EVM-PWR587 contains a 10-Ω series resistor in the feedback loop for loop response analysis.

1. Set up the EVM as described in Section 5 and Figure 5-2.
2. Connect the isolation transformer to test points marked TP5 and TP8.
3. Connect input signal amplitude measurement probe (channel A) to TP10. Connect the output signal amplitude measurement probe (channel B) to TP11.
4. Connect ground lead of channel A and channel B to TP15.
5. Inject around 20-mV or less signal through the isolation transformer.
6. Sweep the frequency from 100 Hz to 1 MHz with 10 Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect the isolation transformer from bode plot test points before making other measurements (signal injection into feedback may interfere with accuracy of other measurements).

7.3 List of Test Points

Table 7-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	VIN	Converter input supply voltage
TP2	VREG	LDO voltage
TP3	PGood	Power good output
TP4	PGND	Power ground
TP5	CHB	Input B for loop injection
TP6	SW	Switching node
TP7	VOUT	V_{OUT} terminal +
TP8	CHA	Input A for loop injection
TP9	PGND	Power ground
TP10	RF	RF pin
TP11	TRIP	TRIP pin
TP12	EN	Enable pin
TP13	VDD	VDD pin
TP14	MODE	Mode pin
TP15	AGND	Analog ground

7.4 Equipment Shutdown

1. Shut down load
2. Shut down V_{IN}

8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 8-1 through Figure 8-8) show the design of the TPS53513EVM-PWR587 printed circuit board. The EVM has been designed using 4 Layers, 2-oz copper circuit board.

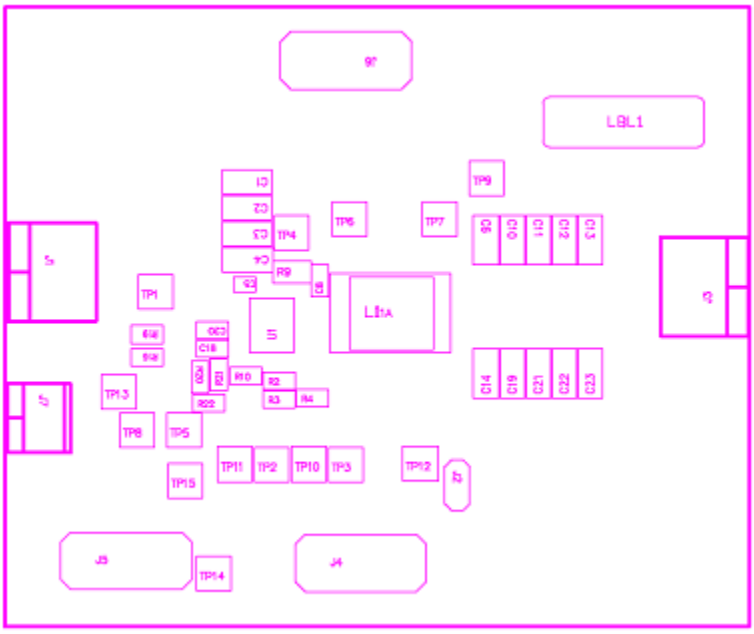

Figure 8-1. TPS53513EVM-587 Top Layer Assembly Drawing

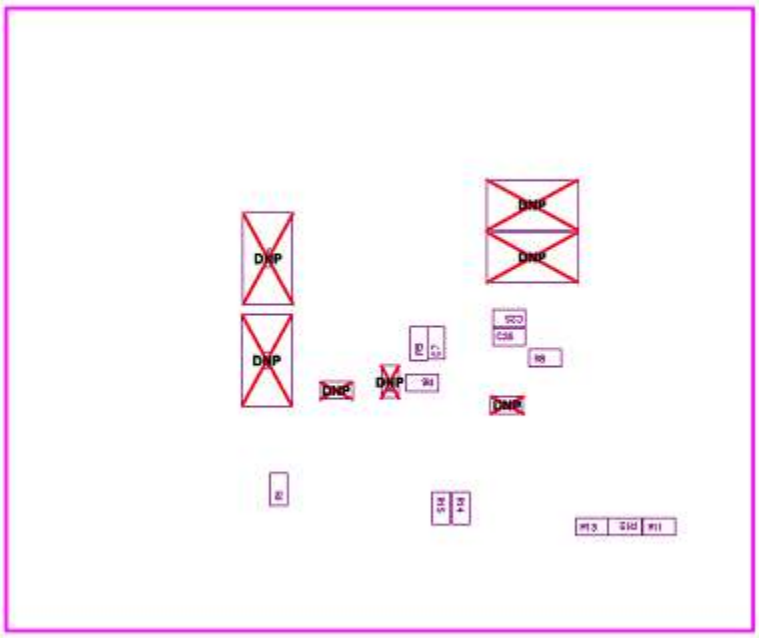

Figure 8-2. TPS53513EVM-587 Bottom Assembly Drawing

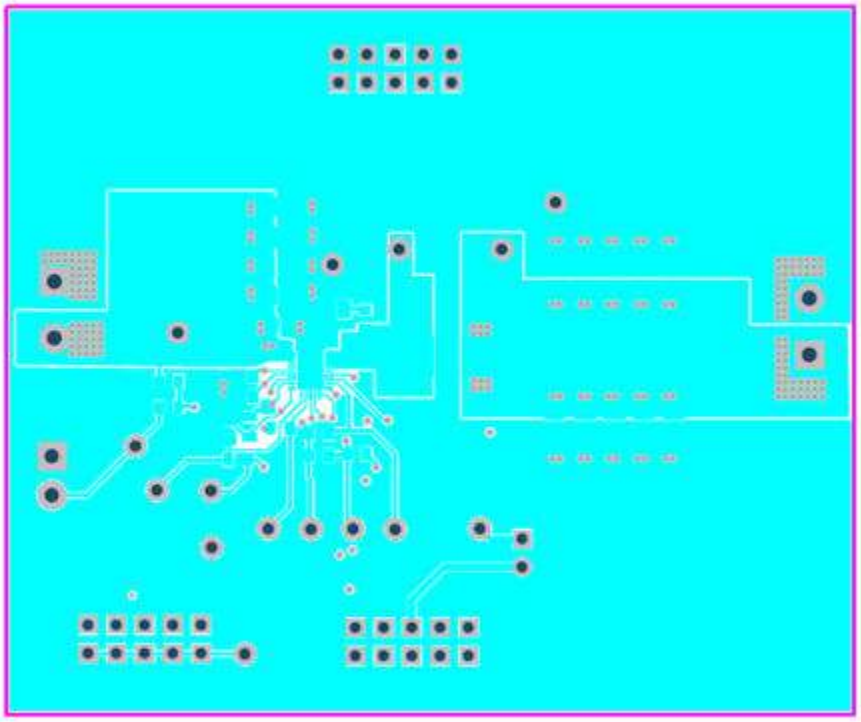

Figure 8-3. TPS53513EVM-587 Top Copper

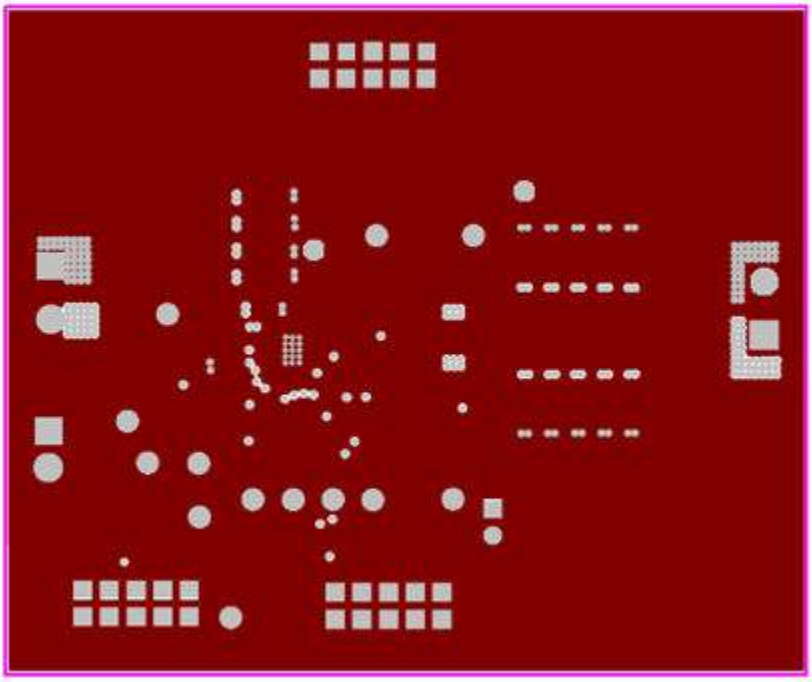

Figure 8-4. TPS53513EVM-587 Layer 2 Copper

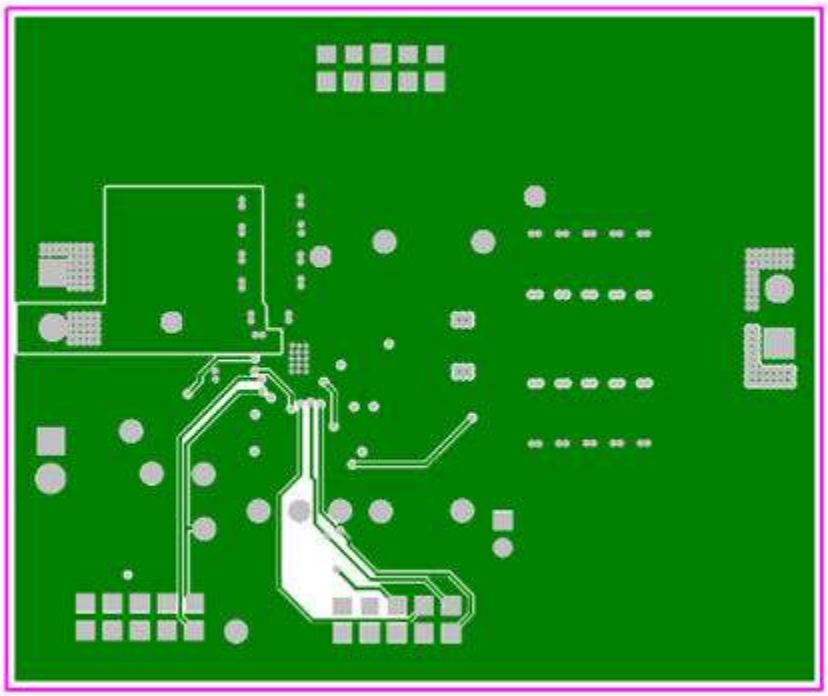

Figure 8-5. TPS53513EVM-587 Layer 3 Copper

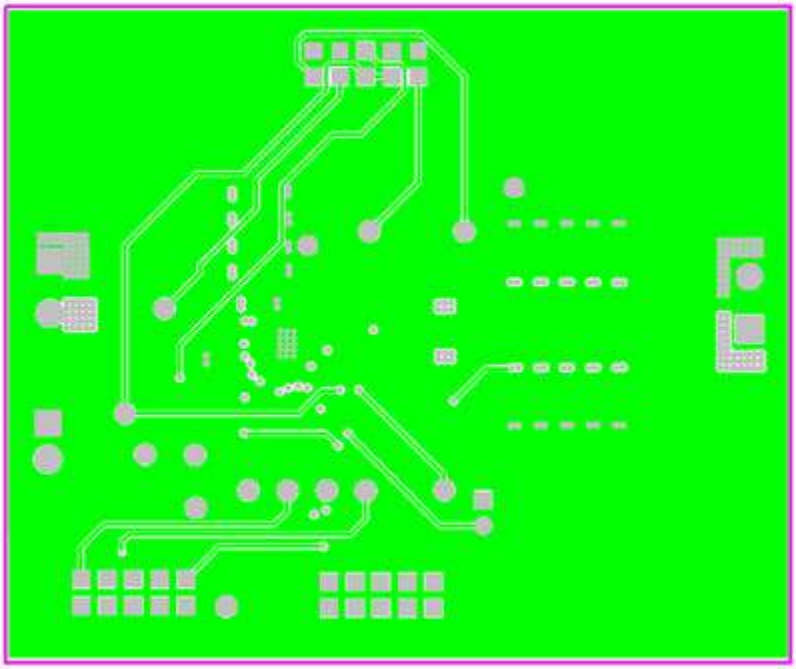

Figure 8-6. TPS53513EVM-587 Layer 4 Copper

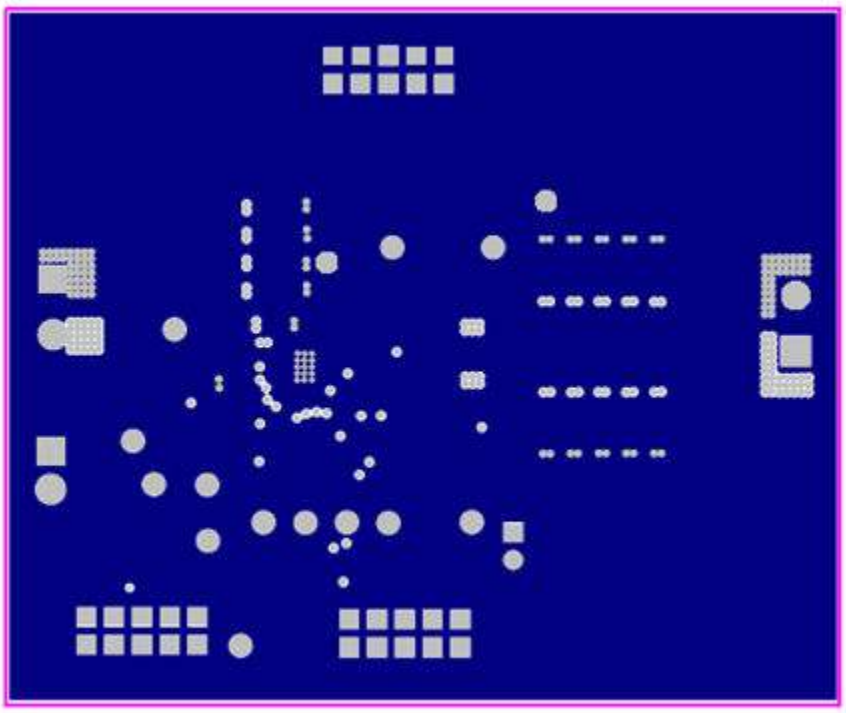

Figure 8-7. TPS53513EVM-587 Layer 5 Copper

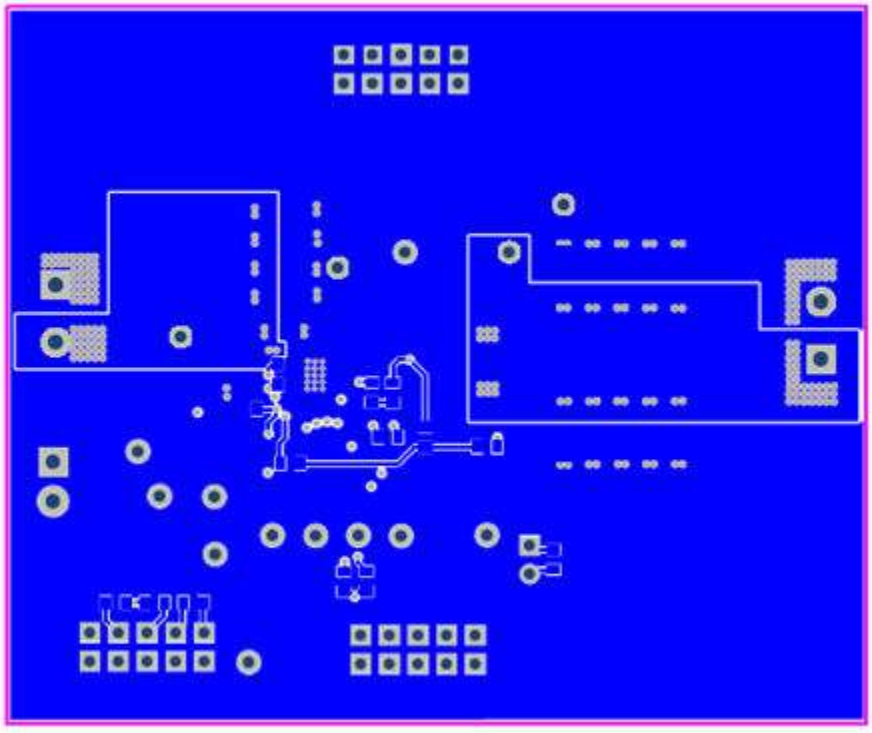

Figure 8-8. TPS53513EVM-587 Bottom Layer Copper

9 List of Materials

The EVM components list according to the schematic shown in Figure 4-1.

Table 9-1. TPS53313EVM-078 List of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REF.	PART NUMBER	MANUFACTURER
C1–C4	4	22 µF	Capacitor, Ceramic, 25 V, X5R, 10%	1206	GRM31CR61E226KE15L	Murata
C5	1	0.1 µF	CAP CER 0.1 µF 25 V 10% X5R 0402	0402	GRM155R61E104KA87D	Murata
C6, C10–C14, C19, C21–C23	10	22 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1206	GRM31CR60J226KE19L	Murata
C7	1	0.1 µF	CAP CER 0.1 µF 50 V 10% X7R 0603	0603	GRM188R71H104KA93D	Murata
C8	1	470 pF	CAP CER 470 pF 50 V 10% X7R 0603	0603	GRM188R71H471KA01D	Murata
C9, C17	0	Open	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
C15, C16, C24, C27	0	Open	Capacitor, POSCAP, SMT, 2.5 V, 330 µF, 8 mΩ	7343(D)	2R5TPE330M9 or 6TPE330MIL	Sanyo
C18, C20, C25, C26	4	1 µF	CAP CER 1 µF 16 V 10% X7R 0603	0603	GRM188R71C105KA12J	Murata
FID1–FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J1, J3	2	ED120/2DS	Terminal Block, 2-pin, 15 A, 5.1 mm	0.40 × 0.35 inch	ED120/2DS	OST
J2	1	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch × 2	PEC02SAAN	Sullins
J4–J6	3	PEC05DAAN	Header, Male 2 × 5-pin, 100mil spacing	0.100 inch × 5 × 2	PEC05DAAN	Sullins
J7	1	ED555/2DS	Terminal Block, 2-pin, 6 A, 3.5 mm	0.27 × 0.25 inch	ED555/2DS	OST
L1	1	1.0 µH	Inductor, Power Chokes SMD	6.6 × 7.1 mm	PIMB065T-1R0MS	Cyntec
L1A	0	DNP	Inductor, High Frequency Power, ±15%	0.283 × 0.433 inch	69P987xN	Vitec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650"H × 0.200"W	THT-14-423-10	Brady
R1, R2	2	100 k	RES, 100 k Ω, 1%, 0.1W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R3	1	1.00 k	RES, 1.00 k Ω, 1%, 0.1 W, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R4	1	300 k	RES, 300 k Ω, 1%, 0.1 W, 0603	0603	RC0603FR-07300KL	Yageo America
R5, R8, R14, R15, R19	5	0	RES, 0 Ω, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R6	1	200 k	RES, 200 k Ω, 1%, 0.1 W, 0603	0603	CRCW0603200KFKEA	Vishay-Dale
R7	0	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R9	1	3.01	RES, 3.01 Ω, 1%, 0.125W, 0805	0805	CRCW08053R01FKEA	Vishay-Dale
R10	1	39.2 k	RES, 39.2 k Ω, 1%, 0.1W, 0603	0603	RC0603FR-0739K2L	Yageo America
R11	1	20.0 k	RES, 20.0 k Ω, 1%, 0.1W, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R12, R13	2	150 k	RES, 150 k Ω, 1%, 0.1 W, 0603	0603	CRCW0603150KFKEA	Vishay-Dale
R16	1	1	RES, 1.00 Ω, 1%, 0.1 W, 0603	0603	CRCW06031R00FKEA	Vishay-Dale
R20, R21	2	10.0 k	RES, 10.0 k Ω, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R22	1	10	RES, 10.0 Ω, 1%, 0.1 W, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
TP1–TP3, TP5–TP8, TP10–TP15	13	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
TP4, TP9	2	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
U1	1	TPS53513RVE	IC, High Performance, 8-A Single Sync. Step-Down Converter		TPS53513RVE	

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2014) to Revision C (November 2021)	Page
• Changed user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Edited user's guide for clarity	2

Changes from Revision A (December 2013) to Revision B (February 2014)	Page
• Changed the test points in Figure 5-1 from TPS5 and TPS7 to TPS7 and TPS9 (respectively from left to right)	4

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