CIRRUS LOGIC
Leading the Digital Entertainment Revolution™

CDB4265

Evaluation Board for CS4265

Features

- Single-ended Analog Inputs
- Single-ended Analog Outputs
- Coaxial and Optical Connections for CS4265 S/PDIF Transmitter Output
- CS8416 S/PDIF Digital Audio Receiver
- Header for Optional External Software Configuration of CS4265
- Header for External PCM Serial Audio I/O
- 3.3 V Logic Interface
- Pre-defined Software Scripts
- Demonstrates Recommended Layout and Grounding Arrangements
- Windows® Compatible Software Interface to Configure CS4265 and Inter-board Connections

ORDERING INFORMATION

CDB4265 Evaluation Board

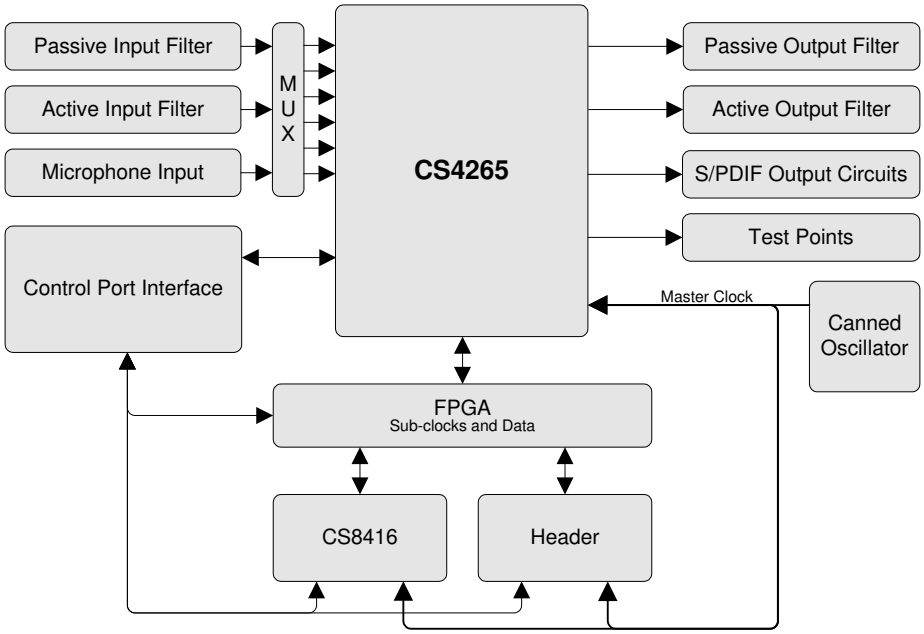
Description

The CDB4265 evaluation board is an excellent means for evaluating the CS4265 CODEC. Evaluation requires an analog/digital signal source and analyzer, and power supplies. A Windows® PC compatible computer must be used to evaluate the CS4265.

System timing for the I²S, Left-Justified and Right-Justified interface formats can be provided by the CS4265, the CS8416, or by a PCM I/O stake header with an external source connected.

RCA phono jacks are provided for the CS4265 analog inputs and outputs. Digital data I/O is available via RCA phono or optical connectors to the CS8416 and CS4265.

The Windows® software provides a GUI to make configuration of the CDB4265 easy. The software communicates through the PC's serial port to configure the control port registers so that all features of the CS4265 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.



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1. SYSTEM OVERVIEW

The CDB4265 evaluation board is an excellent means for evaluating the CS4265 CODEC. Analog and digital audio signal interfaces are provided, an on-board FPGA is used for easily configuring the evaluation platform, and a 9-pin serial cable is included for use with the supplied Windows® configuration software.

The CDB4265 schematic set is shown in Figures 5 through 12.

1.1 Power

Power must be supplied to the evaluation board through the red +5.0 V binding post. On-board regulators provide 3.3 V, 2.5 V, and 1.8 V supplies. Appropriate supply levels for powering VA, VD, VLS, and VLC are set by a series of jumpers (see Table 7 on page 17). All voltage inputs must be referenced to the single black binding post ground connector (see Table 6 on page 16).

WARNING: Please refer to the CS4265 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS4265 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 on page 18 provides an overview of the connections to the CS4265. Figure 13 on page 27 shows the component placement. Figure 14 on page 28 shows the top layout. Figure 15 on page 29 shows the bottom layout. The decoupling capacitors are located as close to the CS4265 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 CS4265 Audio CODEC

A complete description of the CS4265 is included in the CS4265 product data sheet.

The required configuration settings of the CS4265 are made in its control port registers, accessible through the CS4265 tab of the Cirrus Logic FlexGUI software.

Clock and data source selections are made through the control port of the FPGA. Basic routing selections can be made using the CS4265 Controls tab in the GUI software application. Advanced options are accessible through the Board Configuration sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software. Refer to the FPGA register descriptions sections beginning on page 12.

1.4 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 8 on page 22) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS4265 and operates in master or slave mode, generating either a 128 Fs or 256 Fs master clock on the RMCK output pin, and can operate in the Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8416 may be controlled via the S/PDIF Rx Controls tab in the GUI software application. Advanced options are accessible through the CS8416 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.5 FPGA

The FPGA handles both clock and data routing on the CDB4265. Clock and data routing selections made via the CDB4265 Controls tab in the GUI will be handled by the FPGA with no user intervention required. For advanced information regarding the internal registers and operation of the FPGA, see sections 4 and 5 beginning on page 11.

1.6 Canned Oscillator

A canned oscillator, Y1, is available to provide a master clock source to the CDB4265.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.2880 MHz crystal oscillator populated.

1.7 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J15, and J17.

The 14-pin, 2 row header, J15, provides access to the serial audio signals required to interface to the serial audio port of the CS4265 with a DSP (see Figure 11).

The direction of the signals on header J15 can be configured using the controls located within the Board Controls group box on the CDB4265 Controls tab in the provided GUI software.

The 12-pin, 3 row header, J17, allows the user bidirectional access to the SPI/I^2C control signals by simply removing all the shunt jumpers from the “PC” position. The user may then choose to connect a ribbon cable to the “EXT CONTROL” position. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I^2C power rail.

1.8 Analog Inputs

RCA connectors supply the CS4265 analog inputs through single-ended, unity gain, active or passive circuits. Refer to the CS4265 data sheet for the ADC full-scale level.

A 4-pin CD-ROM type header is provided for easily connecting the analog outputs from a CD-ROM drive to the analog inputs of the CS4265.

1.9 Analog Outputs

The CS4265 analog outputs are routed through a two-pole active filter. The output of the filter is connected to RCA jacks for easy evaluation.

1.10 Serial Control Port

A graphical user interface is included with the CDB4265 to allow easy manipulation of the registers in the CS4265, CS8416, and FPGA. See the device-specific data sheets for the CS4265, CS8416, and CD8406 internal register descriptions. The internal register map for the FPGA is located in section 4 on page 11.

Connecting a cable to the RS-232 connector (J19) and launching the Cirrus Logic FlexGUI software (FlexLoader.exe) will enable the CDB4265.

Refer to “PC Software Control” on page 7 for a description of the Graphical User Interface (GUI).

1.11 USB Control Port

The USB control port connector (J29) is currently unavailable.

2. SYSTEM CLOCKS AND DATA

The CDB4265 implements comprehensive clock and data routing capabilities. Configuration of the clock and data routing can be easily achieved using the controls within the Board Controls group box on the CDB4265 Controls tab in the GUI software application.

2.1 Clock Routing

The master clock signal (MCLK) may be sourced from the canned oscillator (Y1), the CS8416 S/PDIF receiver, or the PCM I/O header (J15)

The sub-clock signals (SCLK and LRCK) may be sourced from the CS4265 in master mode, the CS8416 in master mode, or the PCM I/O header.

Clock routing configuration is achieved using the MCLK Source and Subclock Source controls within the Board Controls group box on the CDB4265 Controls tab in the GUI software application.

2.2 Data Routing

The CDB4265 implements comprehensive data routing capabilities. The SDIN source of the CS4265 may be easily selected using the provided GUI software application.

2.2.1 CS4265 SDIN1 and SDIN2 Source

The CS8416 S/PDIF receiver, the PCM I/O header (J15), or the CS4265 serial data output (SDOUT) may source the serial data input of the CS4265. Configuration of the CS4265 SDIN1 and SDIN2 source is achieved using the respective CS4265 SDIN Source control within the Board Controls group box on the CDB4265 Controls tab in the GUI software application.

2.2.2 CS4265 TXSDIN Source

The CS8416 S/PDIF receiver, the PCM I/O header (J15), or the CS4265 serial data output (SDOUT) may source the serial data input of the CS4265. Configuration of the CS4265 TXSDIN source is achieved using the CS4265 TxSDIN Source control within the S/PDIF Transmitter group box on the CDB4265 Controls tab in the GUI software application.

3. PC SOFTWARE CONTROL

The CDB4265 is shipped with a Microsoft Windows® based graphical user interface which allows control over the CS4265, CS8416, and FPGA. The board control software communicates with the CDB4265 over the RS-232 interface using the PC's COM1 port.

To use the board control software, the contents of the included CD-ROM should first be copied to a directory on the PC's local disk. If applied, the Read Only attribute should be removed from all files. Once the appropriate cable has been connected between the CDB4265 and the host PC, load FlexLoader.exe from the Software directory. When the software loads, all devices will be reset to their default reset state.

The GUI's File menu provides the ability to save and load script files containing all of the register settings. Pre-configured script files are provided for basic functionality. Refer to "Pre-Configured Script Files" on page 9 for details.

3.1 CDB4265 Controls Tab

The CDB4265 Controls tab provides a high-level intuitive interface to many of the configuration options of the CS4265 and CDB4265. The controls within the CS4265 Controls group box (with the exception of the AD0 control) control the internal registers of the CS4265. The controls within the Board Controls group box control the board level clock and data routing on the CDB4265.

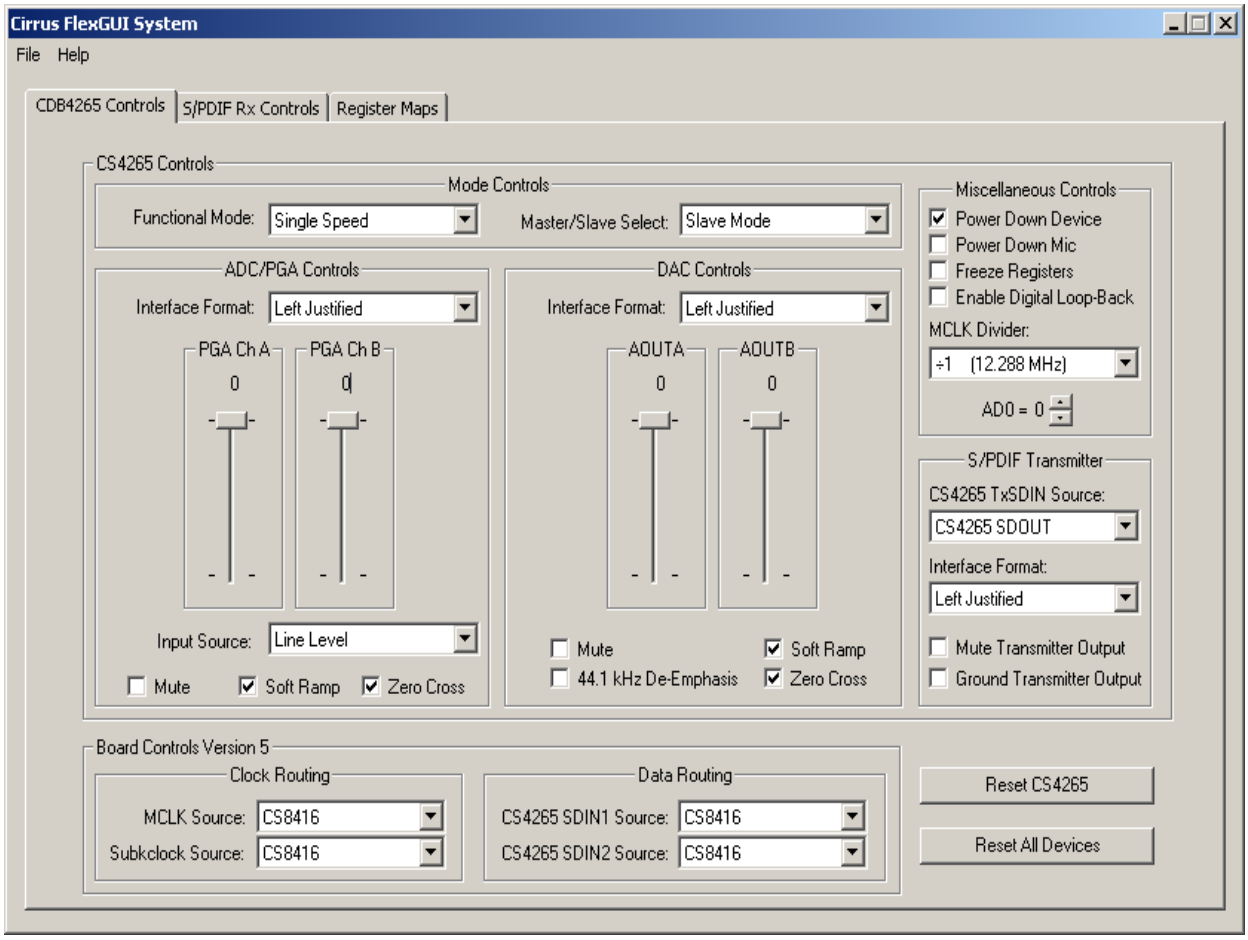

Figure 1. CDB4265 Controls Tab

3.2 S/PDIF Rx Controls Tab

When the CDB4265 is configured to make use of the CS8416 S/PDIF receiver, these devices must be configured for proper operation. The S/PDIF Rx Controls tab provides a high-level intuitive interface to the most common configuration options of the CS8416.

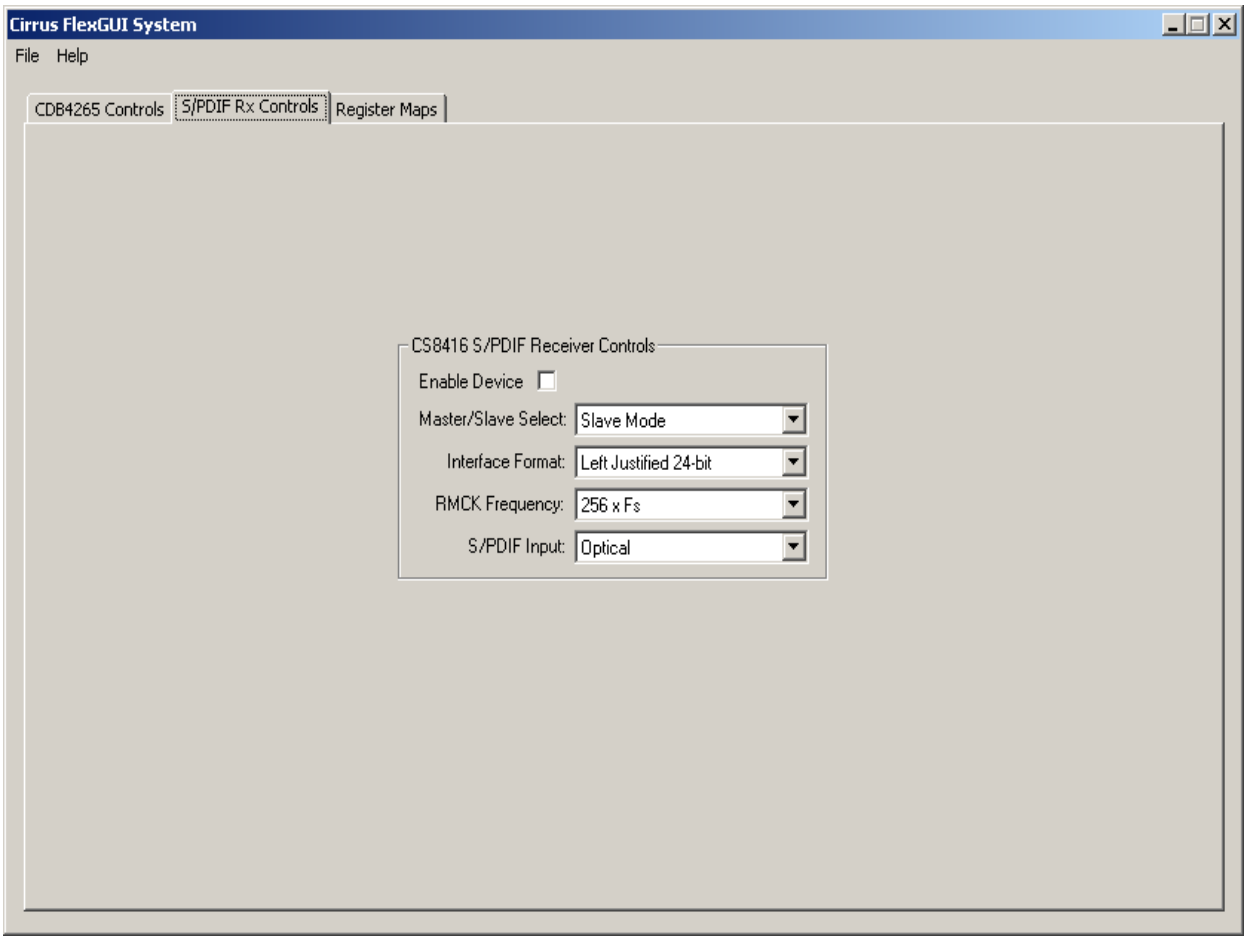

Figure 2. S/PDIF Rx Controls Tab

3.3 Register Maps Tab

The Register Maps tab provides low level control over the register level settings of the CS4265, CS8416, and FPGA. Each device is displayed on a separate tab. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push button for the desired bit. For byte-wise, the desired hex value can be typed directly in the register address box in the register map.

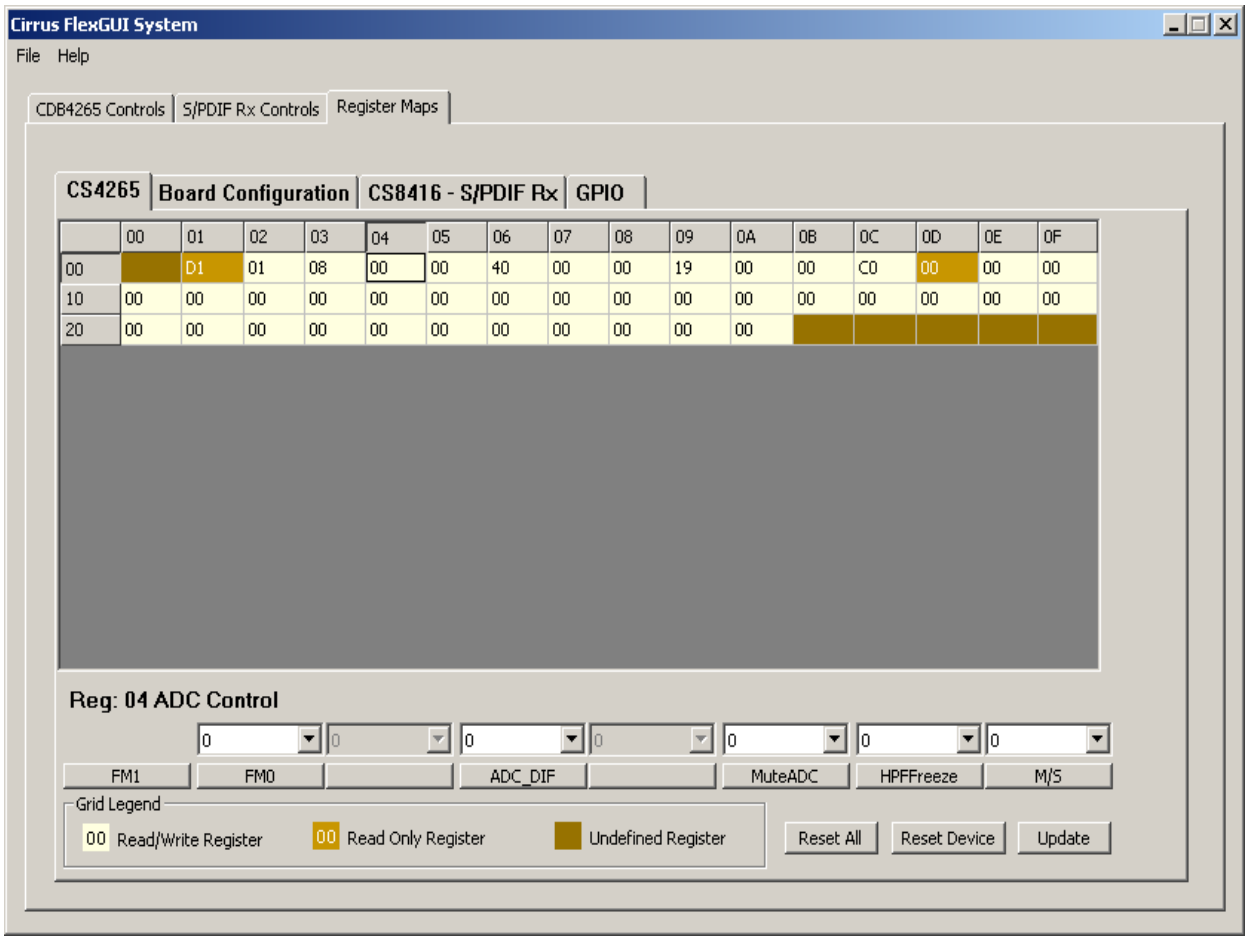

Figure 3. Register Maps Tab

3.4 Pre-Configured Script Files

Pre-configured script files are provided with the CDB4265 to allow easy initial board bring-up. The board configurations stored within these files are described in sections 3.4.1 - 3.4.2.

3.4.1 Oscillator Clock - Line In to DAC & SPDIF Out

Using the pre-configured script file named “Oscillator Clock - Line In to DAC & SPDIF Out.txt”, an analog input signal applied to the line level inputs of the CS4265 input multiplexer will be digitized by the ADC, transmitted in S/PDIF format by the CS4265 internal S/PDIF transmitter, and converted to analog by the DAC and output through the passive output filter.

The canned oscillator is the source of MCLK. The CS4265 is the sub-clock master to the PCM I/O header.

3.4.2 SPDIF Recovered Clock - SPDIF In to DAC - ADC to SPDIF Out

Using the pre-configured script file named “SPDIF Recovered Clock - SPDIF In to DAC - ADC to SPDIF Out.txt”, an analog input signal applied to the line level inputs of the CS4265 input multiplexer will be digitized by the ADC and transmitted in S/PDIF format by the CS4265 internal S/PDIF transmitter. The S/PDIF signal received by the CS8416 will be recovered, decoded into PCM, and routed to the CS4265 DAC where it will be converted to analog by the DAC and output through the passive output filter. For proper operation of this script, a valid S/PDIF signal must be applied.

The CS8416 recovered clock is the source of MCLK. The CS8416 is also the sub-clock master to the CS4265 and the PCM I/O header.

4. FPGA REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Code Rev. ID	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0
		x	x	x	x	x	x	x	x
02h	MCLK Source	Reserved	Reserved	MCLK1	MCLK0	Reserved	Reserved	Reserved	Reserved
		0	0	1	0	0	0	0	0
03h	Subclock Source	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SUBCLK1	SUBCLK0
		0	0	0	1	0	0	0	1
03h	CS4265 SDIN Source	Reserved	SDIN2.2	SDIN2.1	SDIN2.0	Reserved	SDIN1.2	SDIN1.1	SDIN1.0
		0	0	0	0	0	0	0	0
04h	Transmitter SDIN Source	Reserved	Reserved	Reserved	Reserved	Reserved	TXSDIN2	TXSDIN1	TXSDIN0
		0	0	0	1	0	0	0	1

5. FPGA REGISTER DESCRIPTION

5.1 CODE REVISION ID - REGISTER 01H

7	6	5	4	3	2	1	0
Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0

Function:

Identifies the revision of the FPGA code. This register is Read-Only.

5.2 MCLK SOURCE CONTROL - ADDRESS 02H

7	6	5	4	3	2	1	0
Reserved	Reserved	MCLK1	MCLK0	Reserved	Reserved	Reserved	Reserved

5.2.1 MCLK SOURCE (BITS 5:4)

Default = 10

Function:

These bits select the source of the CS4265 MCLK signal. Table 1 shows the available settings.

Table 1. MCLK Source

MCLK1	MCLK0	MCLK Source
0	0	Oscillator
0	1	MCLK position on PCM Header (J15)
1	0	CS8416 RMCK
1	1	Reserved

5.3 SUBCLOCK SOURCE CONTROL - ADDRESS 03H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SUBCLK1	SUBCLK0

5.3.1 SUBCLOCK SOURCE (BITS 1:0)

Default = 01

Function:

This bit selects the source of the CS4265 SCLK and LRCK signals. Table 2 shows the available settings.

Table 2. CS4265 Subclock Source

SUBCLK1	SUBCLK0	CS4265 Subclock Source
0	0	- CS4265 is Master - PCM Header Subclocks are Output from CS4265
0	1	Reserved
1	0	- CS4265 is Slave to PCM Header - PCM Header Subclocks are an Input
1	1	- CS4265 is Slave to CS8416 subclocks - PCM Header Subclocks are Output from CS8416 Subclocks

5.4 CS4265 SDIN SOURCE CONTROL - ADDRESS 04H

7	6	5	4	3	2	1	0
Reserved	SDIN2.2	SDIN2.1	SDIN2.0	Reserved	SDIN1.2	SDIN1.1	SDIN1.0

5.4.1 SDIN2 SOURCE (BITS 6:4)

Default = 00
Function:

These bits select the source of the CS4265 SDIN2 signal. Table 3 shows the available settings.

Table 3. SDIN2 Source

SDIN2.2	SDIN2.1	SDIN2.0	SDIN2 Source
0	0	0	CS8416 SDOUT
0	0	1	CS4265 SDOUT
0	1	0	SDIN1 from Header
0	1	1	SDIN2 from Header
1	0	0	TXSDIN from Header
1 ... 1	0 ... 1	1 ... 1	Reserved

5.4.2 SDIN1 SOURCE (BITS 2:0)

Default = 00
Function:

These bits select the source of the CS4265 SDIN1 signal. Table 4 shows the available settings.

Table 4. SDIN1 Source

SDIN1.2	SDIN1.1	SDIN1.0	SDIN1 Source
0	0	0	CS8416 SDOUT
0	0	1	CS4265 SDOUT
0	1	0	SDIN1 from Header
0	1	1	SDIN2 from Header
1	0	0	TXSDIN from Header
1 ... 1	0 ... 1	1 ... 1	Reserved

5.5 TRANSMITTER SDIN SOURCE CONTROL - ADDRESS 05H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	TXSDIN2	TXSDIN1	TXSDIN0

5.5.1 TXSDIN SOURCE (BITS 2:0)

Default = 01
Function:

These bits select the source of the CS4265 TXSDIN signal. Table 5 shows the available settings.

Table 5. TXSDIN Source

TXSDIN2	TXSDIN1	TXSDIN0	TXSDIN Source
0	0	0	CS8416 SDOUT
0	0	1	CS4265 SDOUT
0	1	0	SDIN1 from Header
0	1	1	SDIN2 from Header
1	0	0	TXSDIN from Header
1 ... 1	0 ... 1	1 ... 1	Reserved

6. CDB CONNECTORS, JUMPERS, AND SWITCHES

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J4	Input	+5.0 V Power Supply
GND	J3	Input	Ground Reference
S/PDIF RX	OPT1	Input	CS8416 digital audio input via optical cable
S/PDIF RX	J1	Input	CS8416 digital audio input via coaxial cable
CS4265 TXOUT	J13	Output	CS4265 S/PDIF transmitter digital audio output via coaxial cable
CS4265 TXOUT	OPT3	Output	CS4265 S/PDIF transmitter digital audio output via optical cable
RS232 I/O	J19	Input/Output	Serial connection to PC for SPI / I^2C control port signals
USB I/O	J29	Input/Output	USB connection to PC for SPI / I^2C control port signals. **Not Available.**
PCM I/O	J15	Input/Output	I/O for Serial Audio Clocks & Data
CONTROL	J17	Input/Output	I/O for external SPI / I^2C control port signals.
MICRO JTAG	J22	Input/Output	I/O for programming the micro controller (U32).
FPGA-JTAG	J23	Input/Output	I/O for programming the FPGA (U27).
RESET	S2	Input	Reset for the micro controller (U32).
PROGRAM FPGA	S1	Input	Reset for the FPGA (U27).
AINA AINB	J18 J24	Input	RCA phono jacks for analog input signal to CS4265.
CD IN	J30	Input	CD-ROM type header for analog input signal to CS4265.
MICIN1 MICIN2	J14 J16	Input	1/8“ TRS jacks for microphone input.
AOUTA AOUTB	J14 J16	Output	RCA phono jacks for DAC analog outputs.

Table 6. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J6	Selects the source of voltage for the VLS supply.	+1.8 V +2.5 V +3.3 V +5 V*	Voltage source is +1.8 V regulator. Voltage source is +2.5 V regulator. Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J7	Selects the source of voltage for the VLC supply.	+1.8 V +2.5 V +3.3 V +5 V*	Voltage source is +1.8 V regulator. Voltage source is +2.5 V regulator. Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J11	Selects the source of voltage for the VD supply.	+3.3 V +5 V*	Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J12	Selects the source of voltage for the VA supply.	+3.3 V +5 V*	Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J20 J21	Selects the input connector for the mic inputs of the CS4265 ADC input multiplexer.	Line Input* Mic Input	Select RCA inputs as source. Select TRS inputs as source.
J26 J27	Selects the input connector for the line inputs of the CS4265 ADC input multiplexer.	RCA* CD	Select RCA inputs as source. Select CD input as source.
J28	Selects the source of the CS4265 SGND signal.	GND* SGND	Local connection to board ground plane. SGND signal from CD IN connector.

*Default factory settings

Table 7. System Jumper Settings

7. CDB BLOCK DIAGRAM

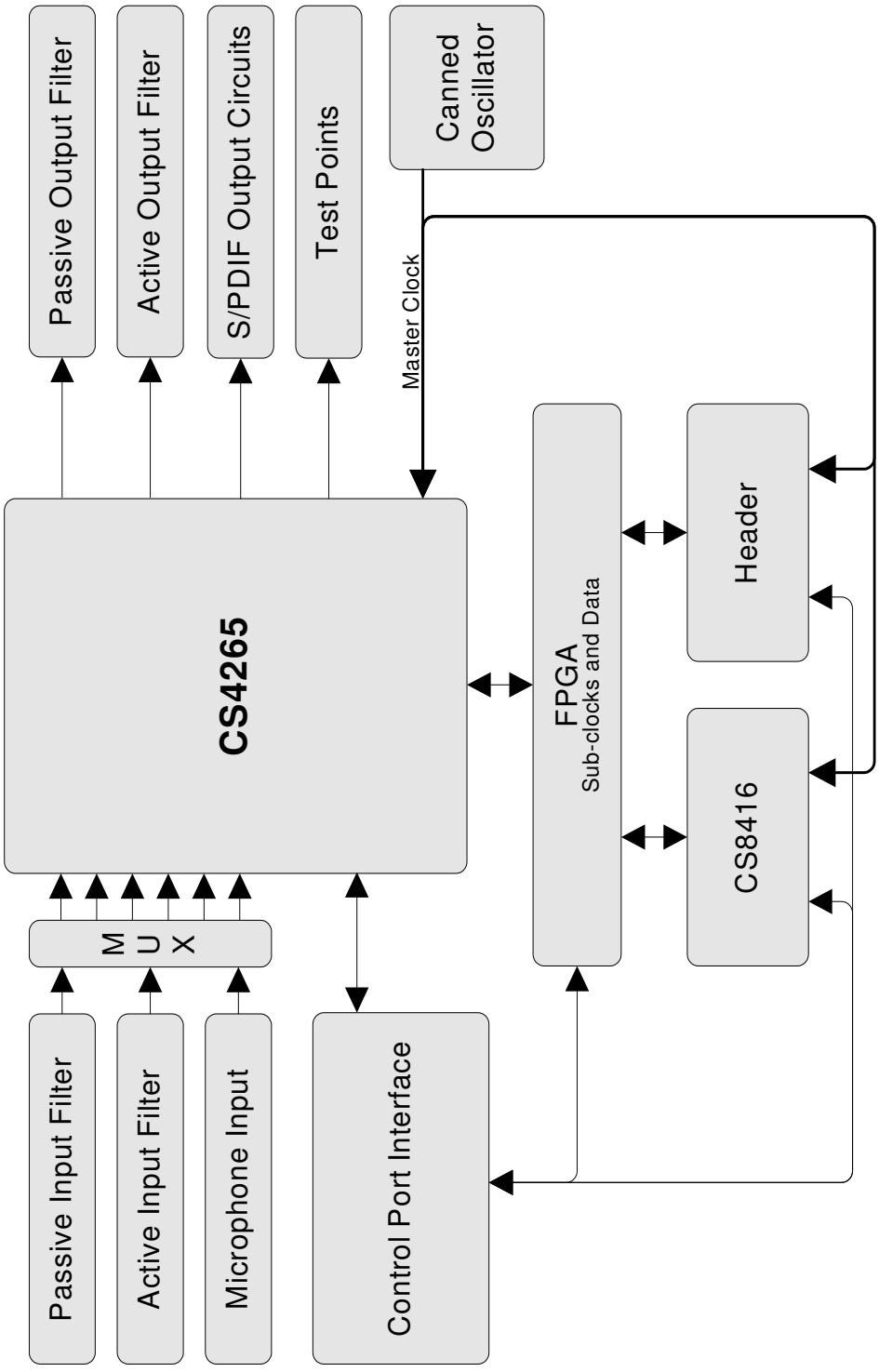

Figure 4. Block Diagram

8. CDB SCHEMATICS

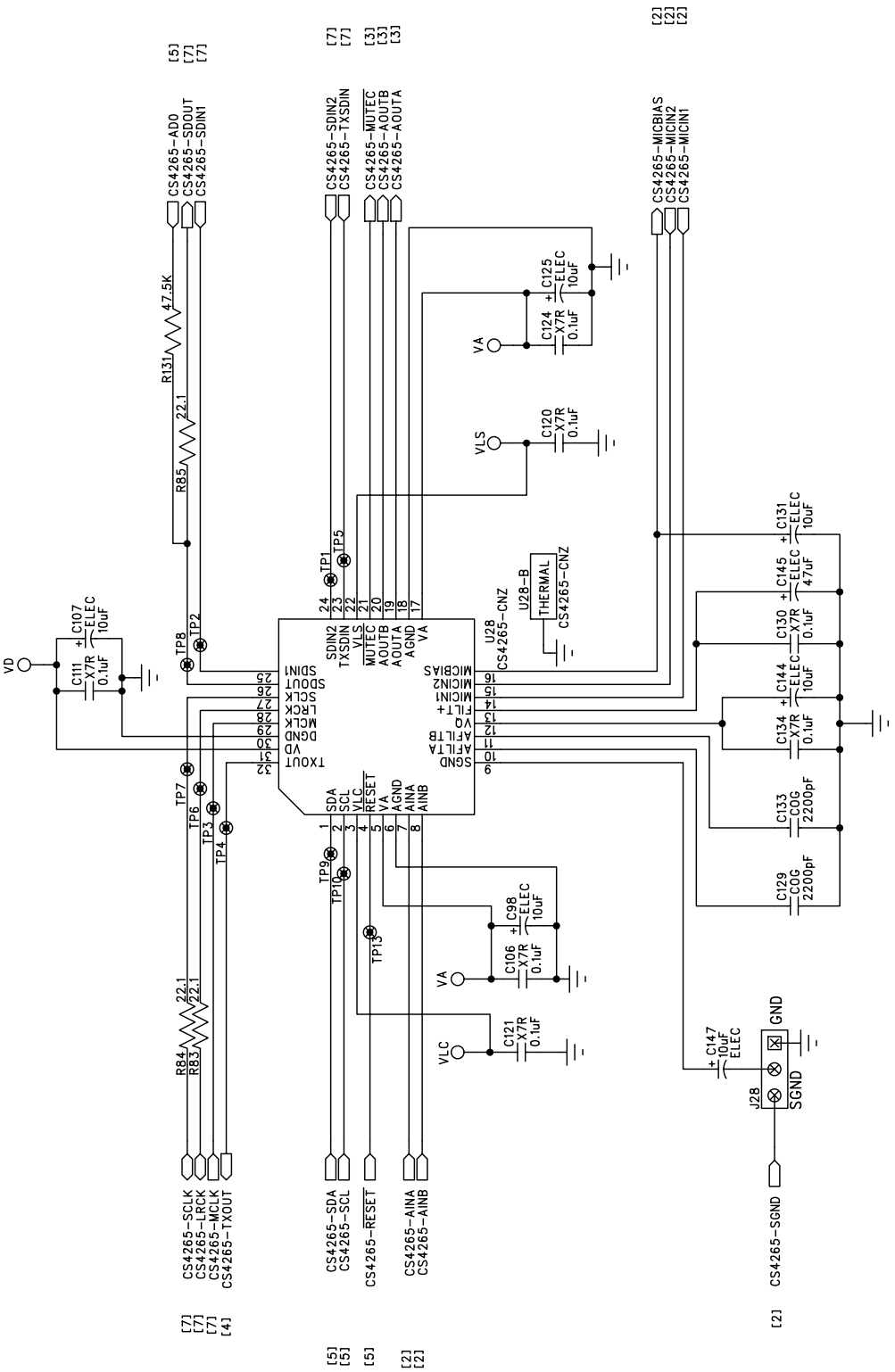

Figure 5. CS4265

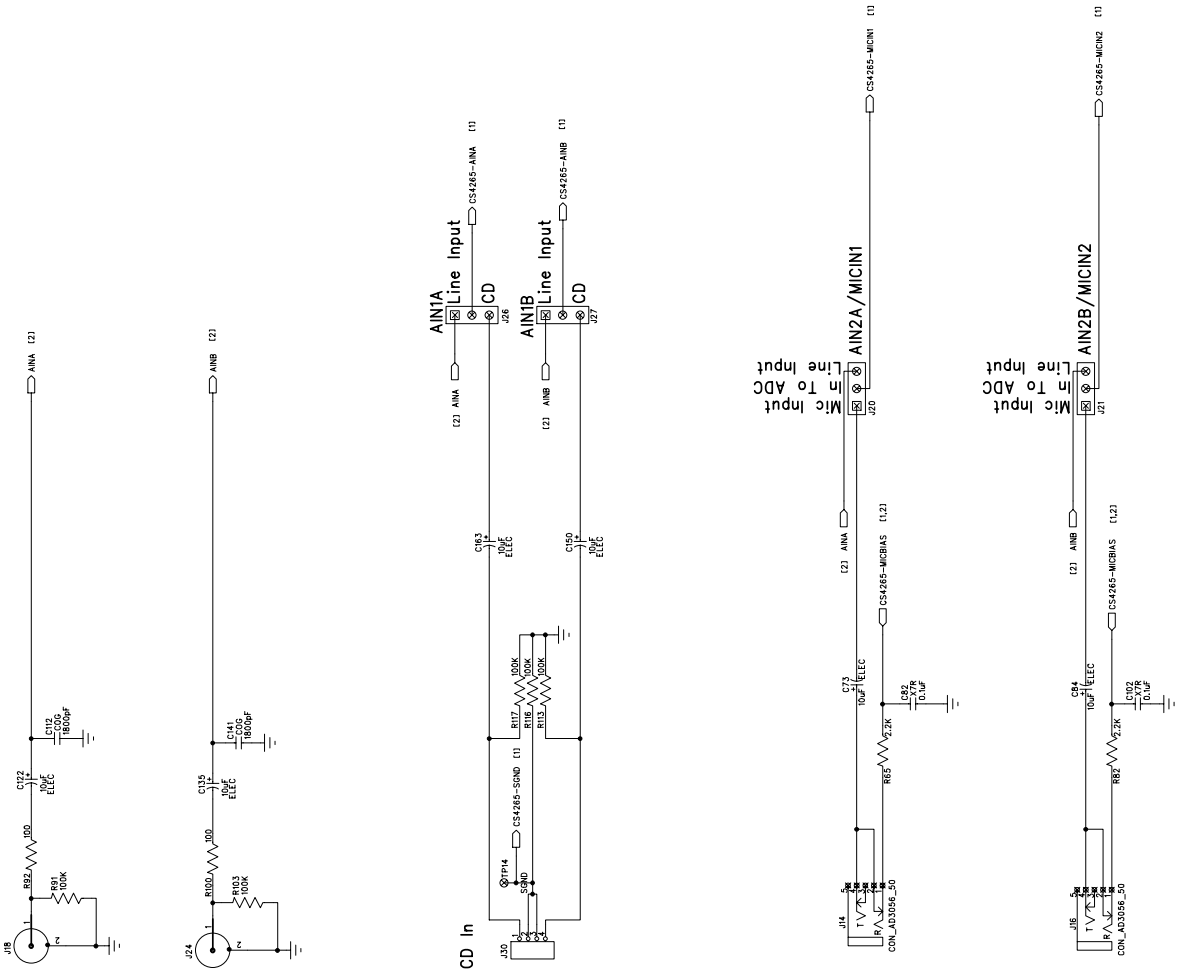

Figure 6. Analog Inputs

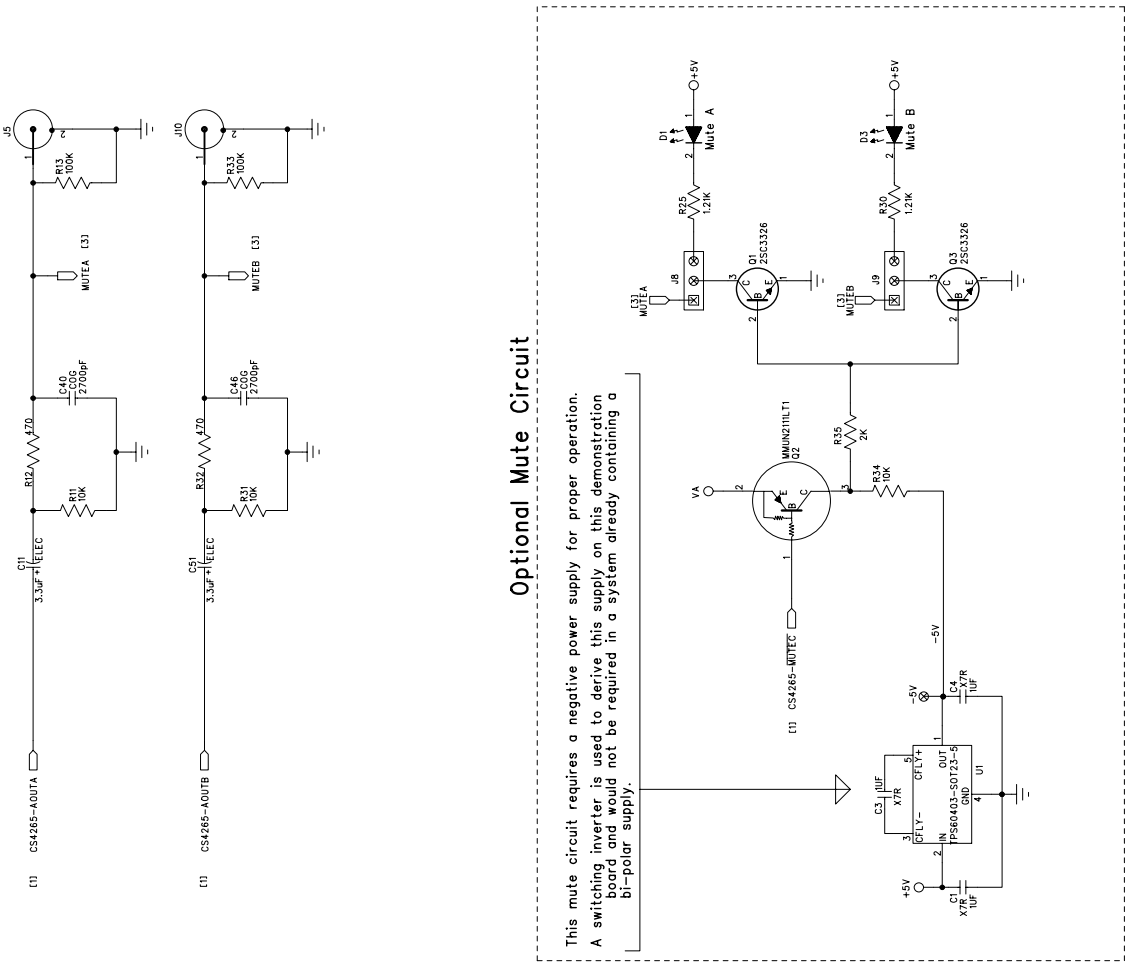

Figure 7. Analog Outputs

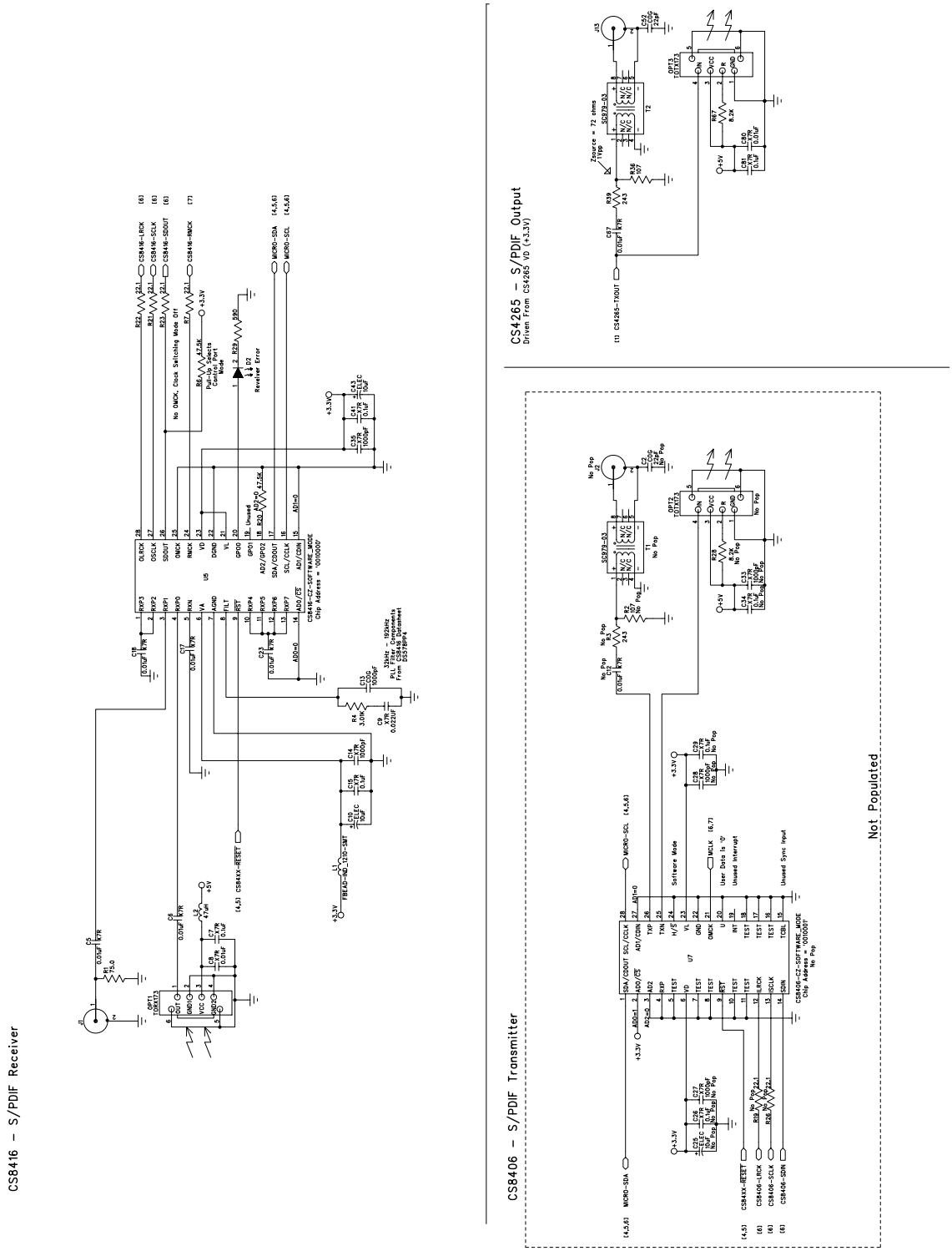

Figure 8. S/PDIF I/O

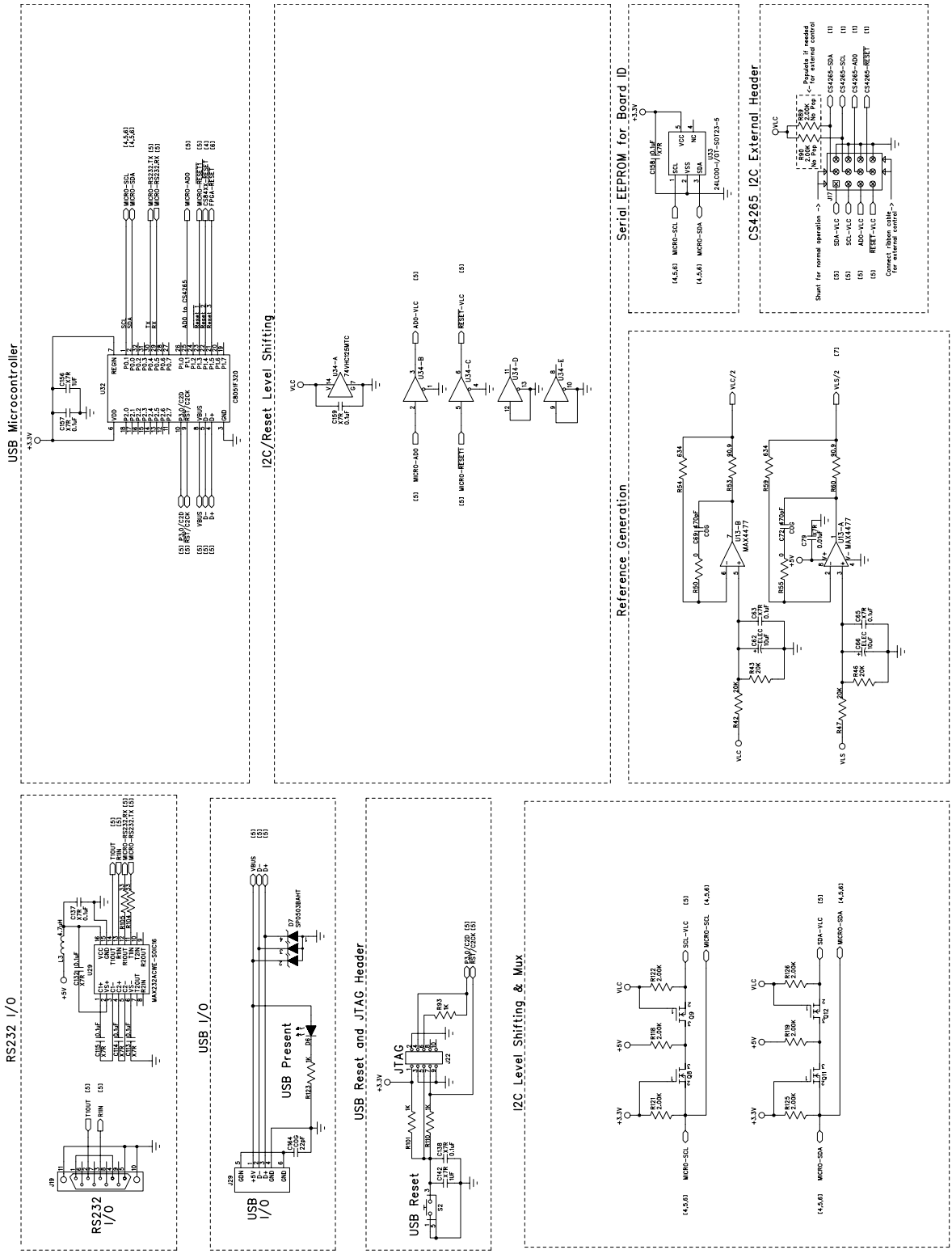

Figure 9. Control Port

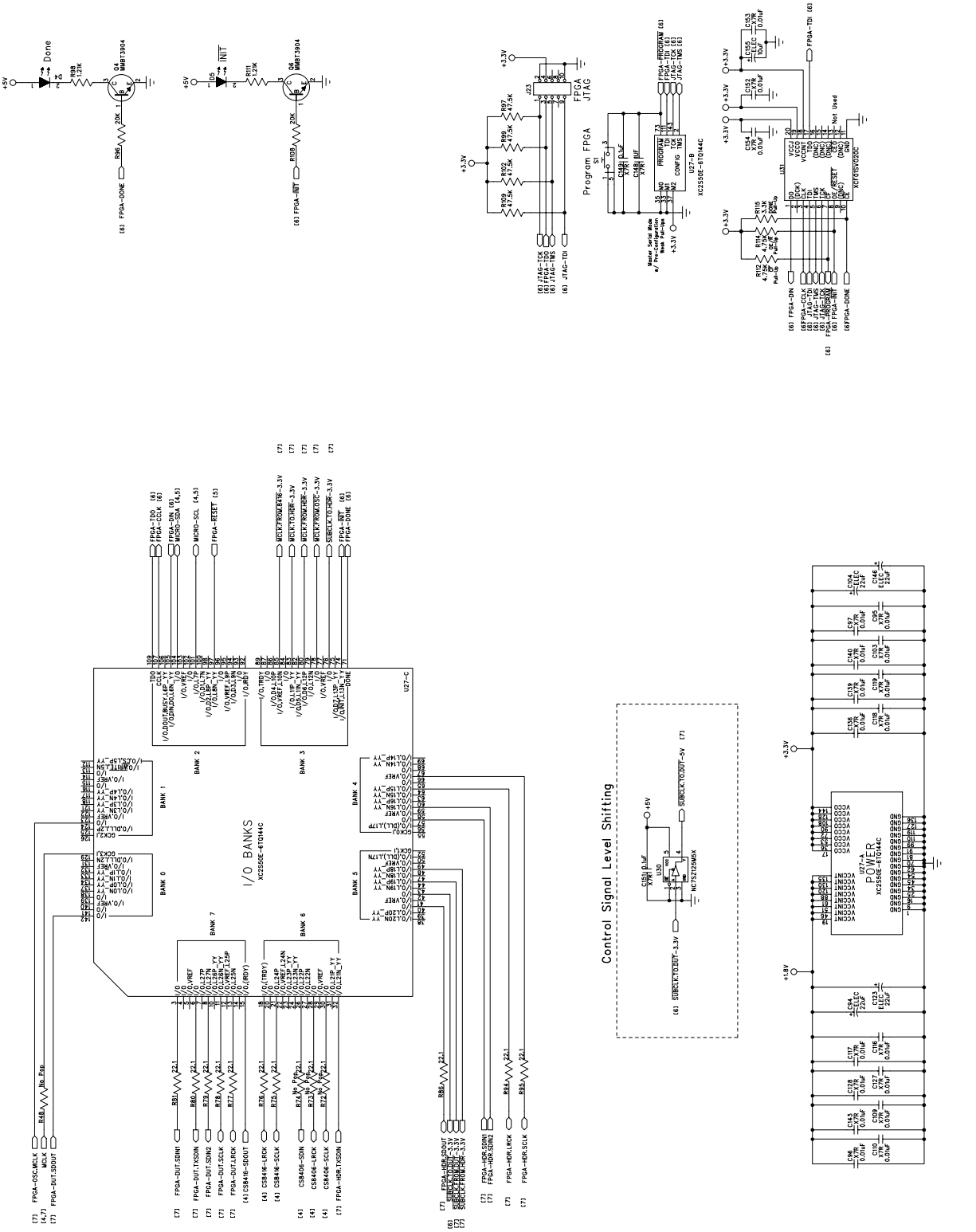

Figure 10. FPGA

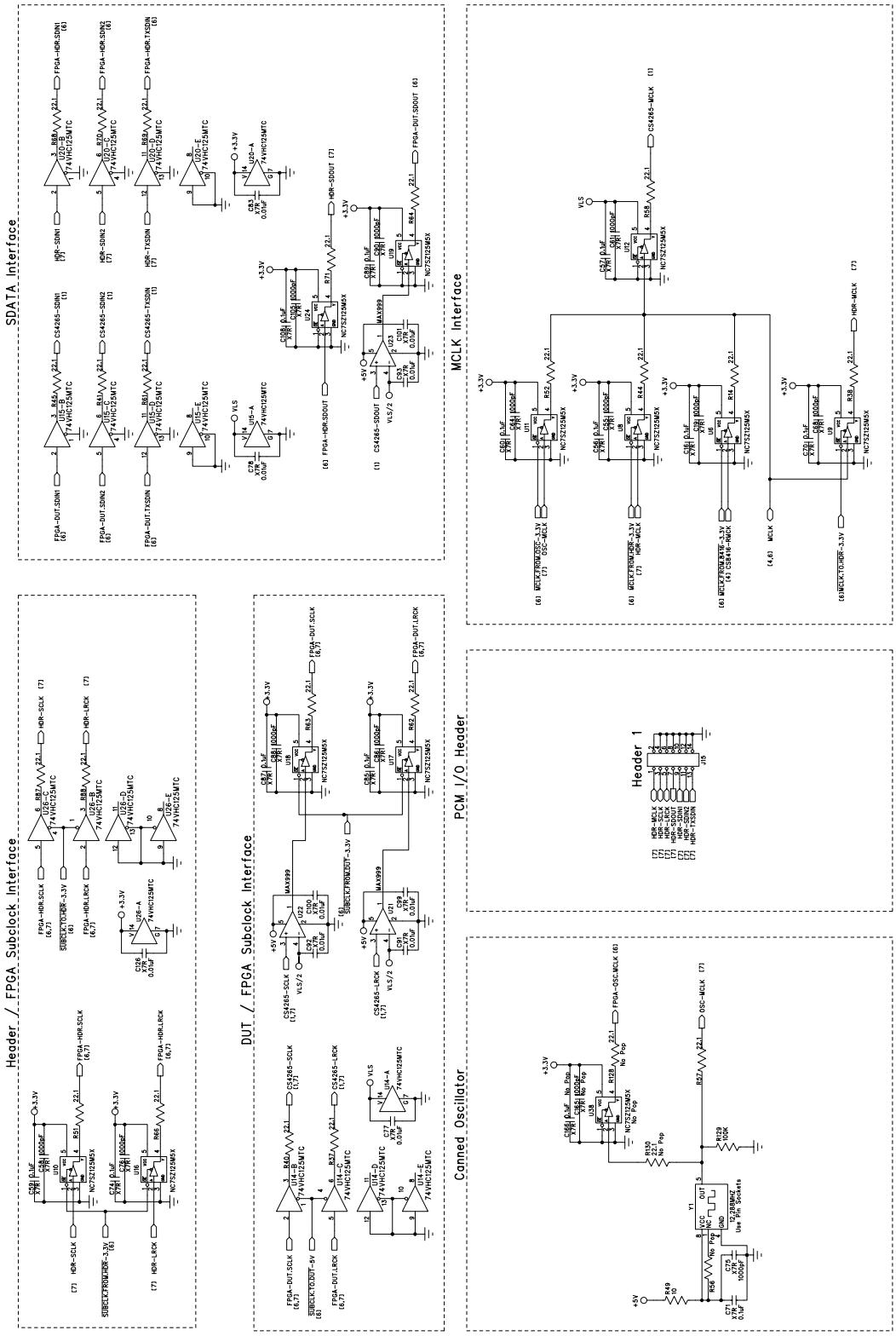

Figure 11. Discrete Clock Routing and Level Shifting

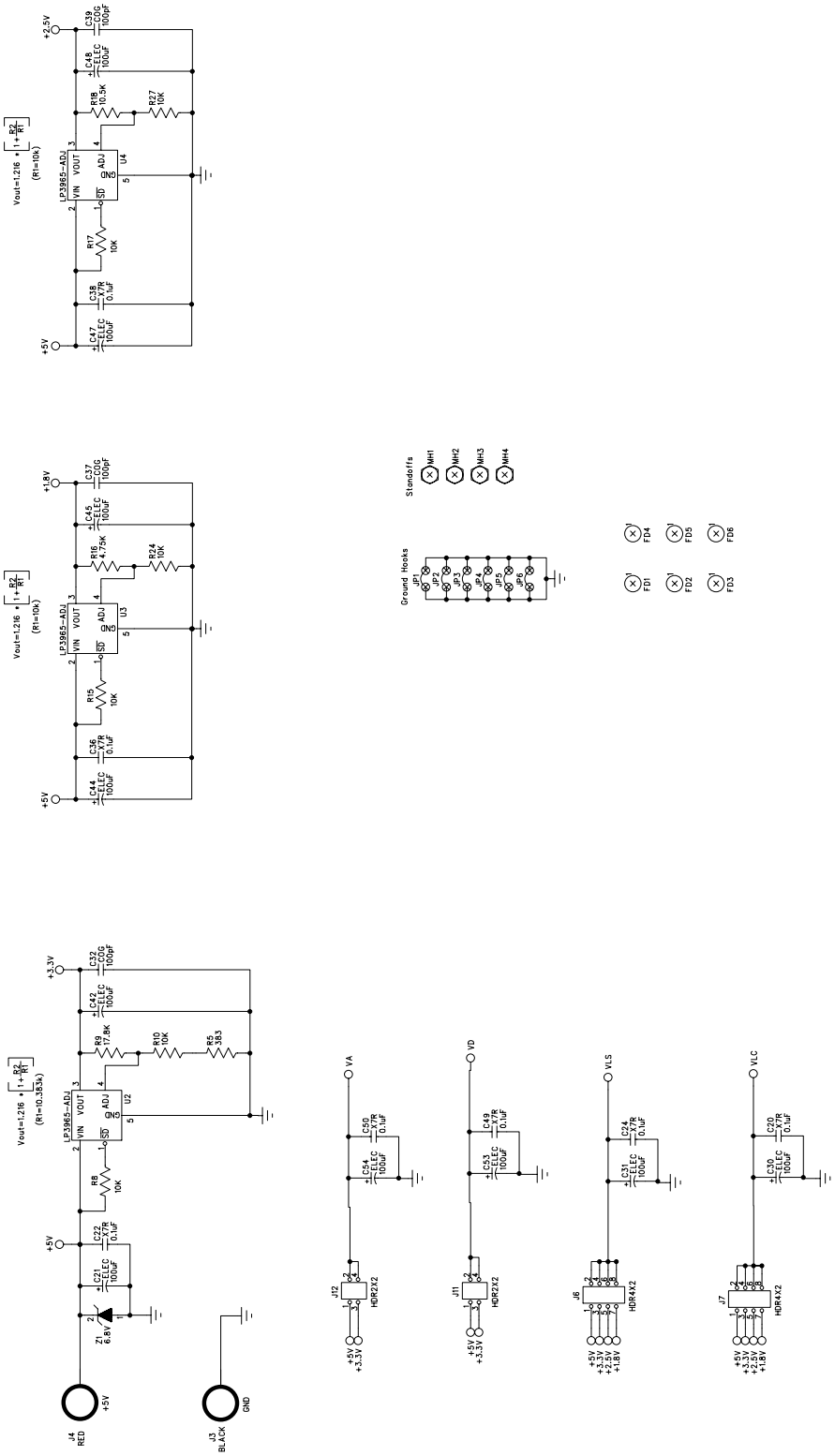

Figure 12. Power

9. CDB LAYOUT

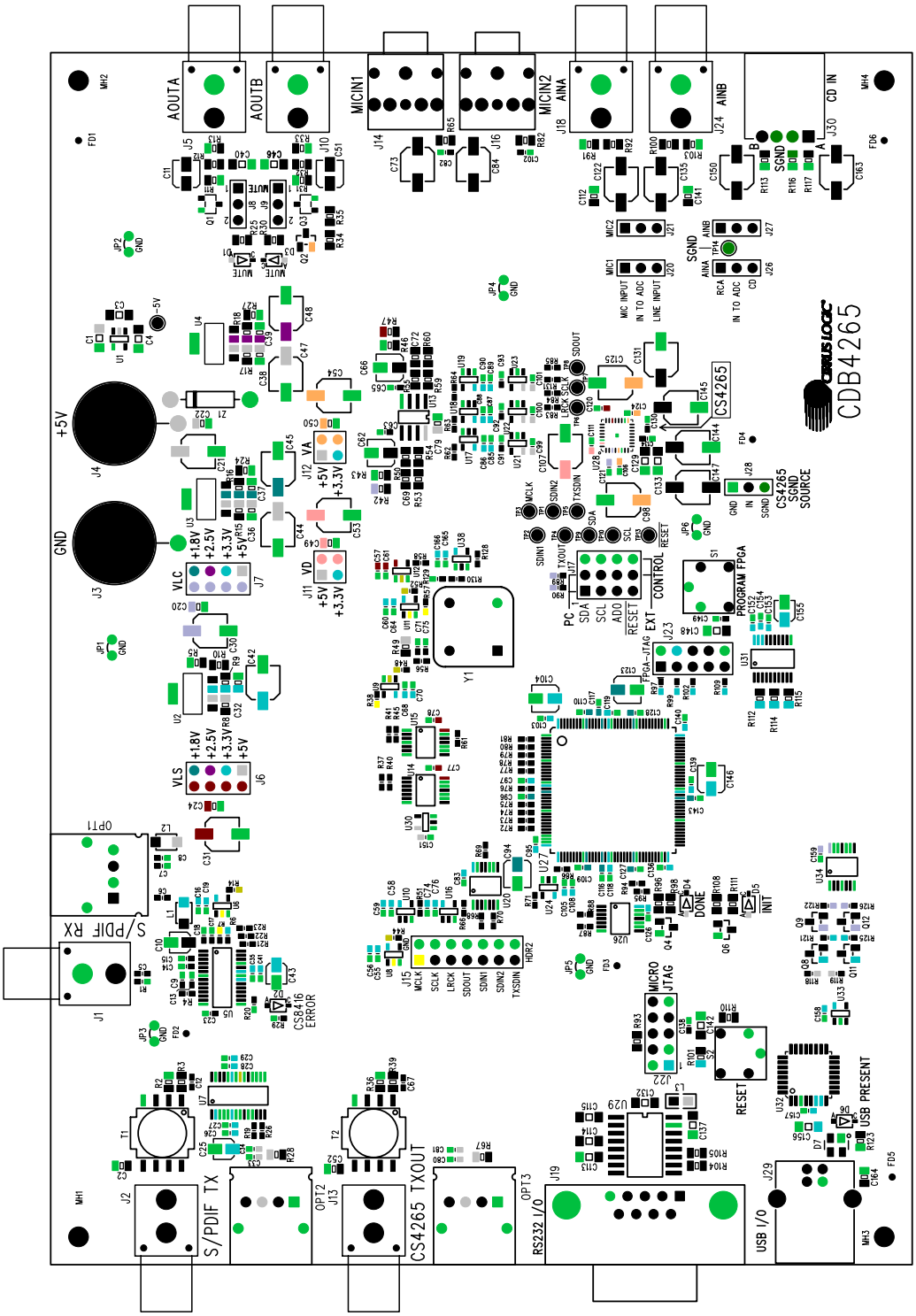

Figure 13. Silk Screen

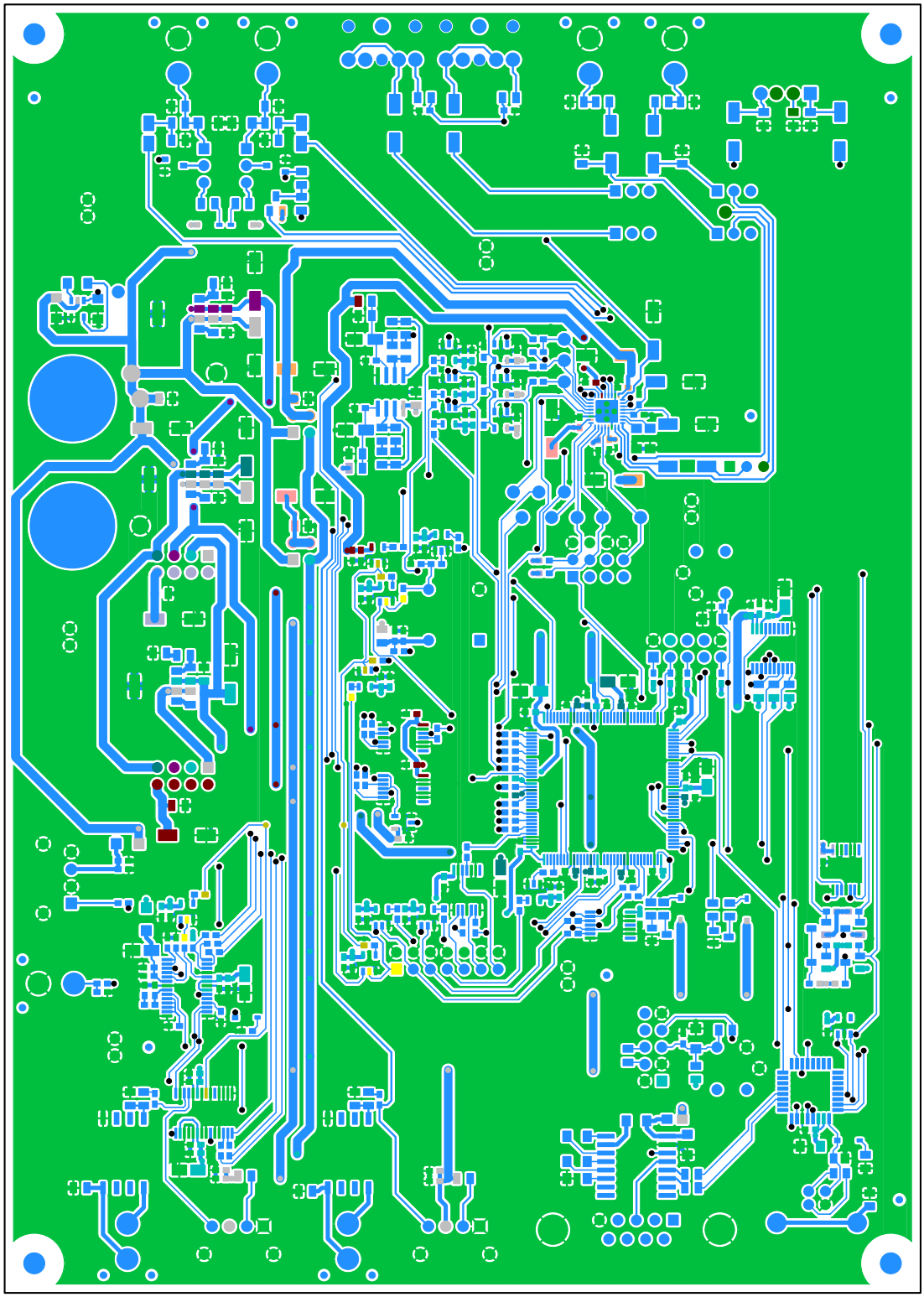

Figure 14. Topside Layer

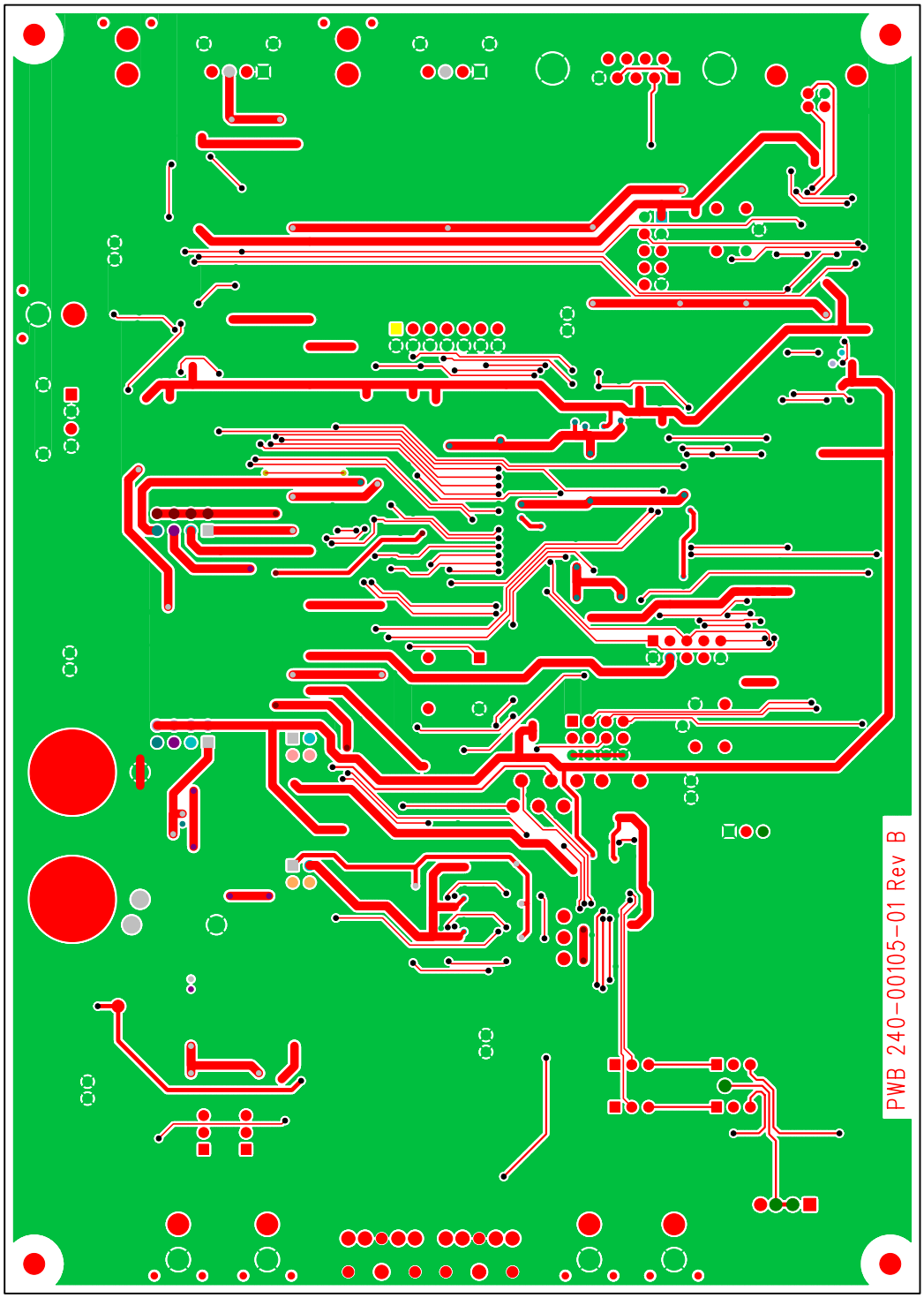

Figure 15. Bottom side Layer

10. REVISION HISTORY

Revision	Date	Changes
DB1	February 2005	Initial Release

Table 8. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**