

### General Description

The IDT8T49N105I is a highly flexible FemtoClock® NG general purpose, low phase noise Universal Frequency Translator / Synthesizer with alarm and monitoring functions suitable for networking and communications applications. It is able to generate any output frequency in the 0.98MHz - 312.5MHz range and most output frequencies in the 312.5MHz - 1,300MHz range (see Table 3 for details). A wide range of input reference clocks and a range of low-cost fundamental mode crystal frequencies may be used as the source for the output frequency.

The IDT8T49N105I has three operating modes to support a very broad spectrum of applications:

- 1) Frequency Synthesizer
  - Synthesizes output frequencies from a 16MHz - 40MHz fundamental mode crystal.
  - Fractional feedback division is used, so there are no requirements for any specific crystal frequency to produce the desired output frequency with a high degree of accuracy.
- 2) High-Bandwidth Frequency Translator
  - Applications: PCI Express, Computing, General Purpose
  - Translates any input clock in the 16MHz - 710MHz frequency range into any supported output frequency.
  - This mode has a high PLL loop bandwidth in order to track input reference changes, such as Spread-Spectrum Clock modulation, so it will not attenuate much jitter on the input reference.
- 3) Low-Bandwidth Frequency Translator
  - Applications: Networking & Communications.
  - Translates any input clock in the 8kHz - 710MHz frequency range into any supported output frequency.
  - This mode supports PLL loop bandwidths in the 10Hz - 580Hz range and makes use of an external crystal to provide significant jitter attenuation.

This device provides two factory-programmed default power-up configurations burned into One-Time Programmable (OTP) memory. The configuration to be used is selected by the CONFIG pin. The two configurations are specified by the customer and are programmed by IDT during the final test phase from an on-hand stock of blank devices. The two configurations may be completely independent of one another.

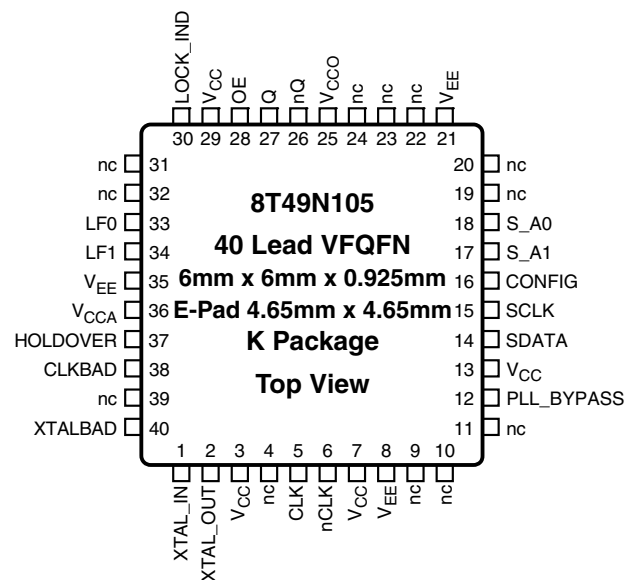
One usage example might be to install the device on a line card with two optional daughter cards: an OC-12 option requiring a 622.08MHz LVDS clock translated from a 19.44MHz input and a Gigabit Ethernet option requiring a 125MHz LVPECL clock translated from the same 19.44MHz input reference.

To implement other configurations, these power-up default settings can be overwritten after power-up using the I<sup>2</sup>C interface and the device can be completely reconfigured. However, these settings would have to be re-written next time the device powers-up.

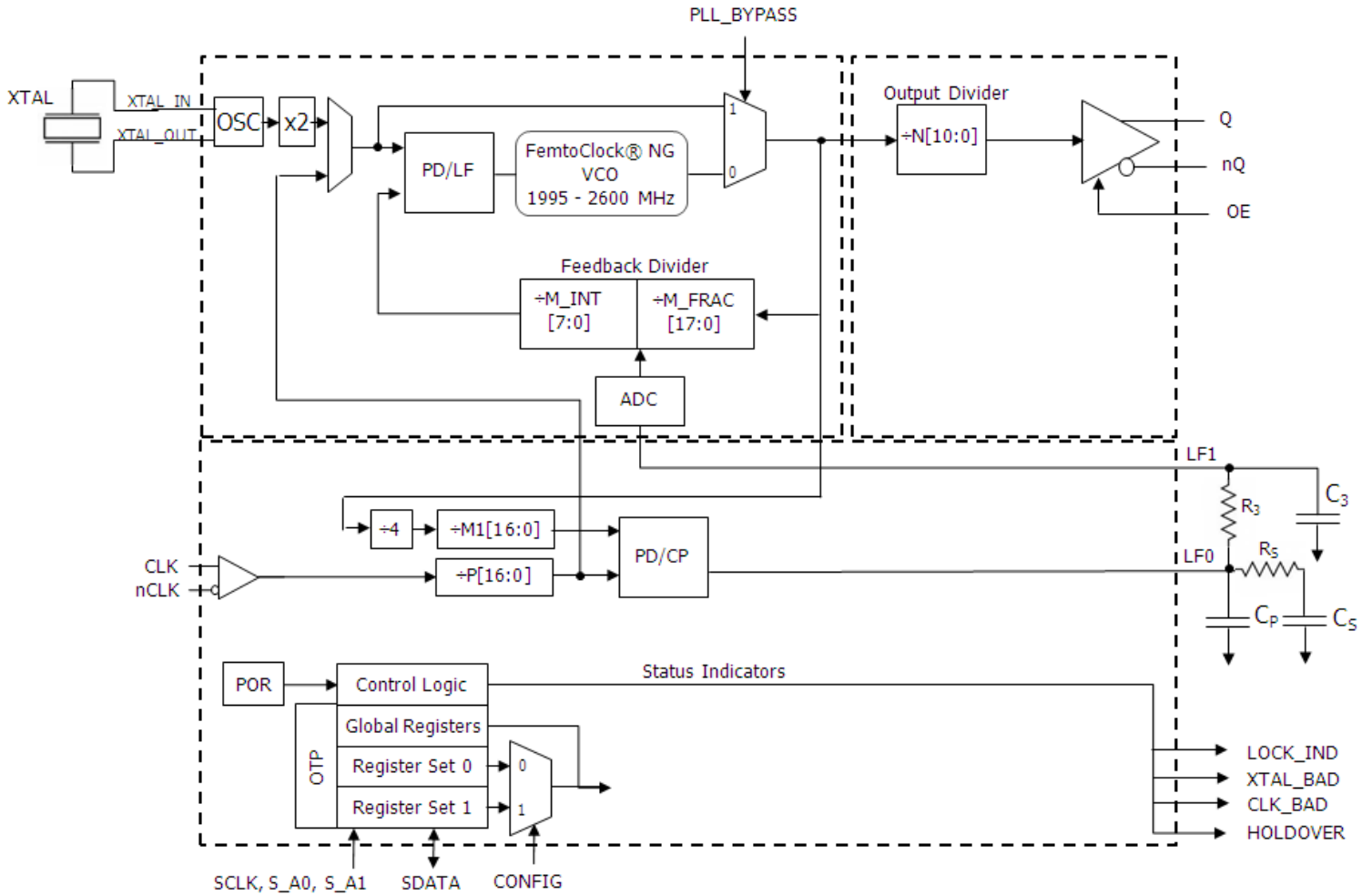
### Features

- Fourth generation FemtoClock® NG technology
- Universal Frequency Translator (UFT) / Frequency Synthesizer
- Single output (Q, nQ), programmable as LVPECL or LVDS
- Zero ppm frequency translation
- Single differential input supports the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Input frequency range: 8kHz - 710MHz
- Crystal input frequency range: 16MHz - 40MHz
- Two factory-set register configurations for power-up default state
  - Power-up default configuration pin or register selectable
  - Configurations customized via One-Time Programmable ROM
  - Settings may be overwritten after power-up via I<sup>2</sup>C
  - I<sup>2</sup>C Serial interface for register programming
- RMS phase jitter at 155.52MHz, using a 40MHz crystal LVDS Output (12kHz - 20MHz): 439fs (typical), Low Bandwidth Mode (FracN)
- RMS phase jitter at 400MHz, using a 40MHz crystal (12kHz - 40MHz): 285fs (typical), Synthesizer Mode (Integer FB)
- Output supply voltage modes:
  - $V_{CC}/V_{CCA}/V_{CCO}$
  - 3.3V/3.3V/3.3V
  - 3.3V/3.3V/2.5V (LVPECL only)
  - 2.5V/2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

### Pin Assignment



# Complete Block Diagram



**Table 1. Pin Descriptions**

Number	Name	Type		Description
1 2	XTAL_IN XTAL_OUT	Input		Crystal Oscillator interface designed for 12pF parallel resonant crystals. XTAL_IN (pin 1) is the input and XTAL_OUT (pin 2) is the output.
3, 7, 13, 29	V <sub>CC</sub>	Power		Core supply pins. All must be either 3.3V or 2.5V.
4, 9, 10, 11, 19, 20, 22, 23, 24, 31, 32, 39	nc	Unused		No connect. These pins are to be left unconnected.
8, 21, 35	V <sub>EE</sub>	Power		Negative supply pins.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating (set by the internal pullup and pulldown resistors).
12	PLL_BYPASS	Input	Pulldown	Bypasses the VCXO PLL. In bypass mode, outputs are clocked off the falling edge of the input reference. LVCMOS/LVTTL interface levels. 0 = PLL Mode (default) 1 = PLL Bypassed
14	SDATA	I/O	Pullup	I <sup>2</sup> C Data Input/Output. Open drain.
15	SCLK	Input	Pullup	I <sup>2</sup> C Clock Input. LVCMOS/LVTTL interface levels.
16	CONFIG	Input	Pulldown	Configuration Pin. Selects between one of two factory programmable pre-set power-up default configurations. The two configurations can have different output/input frequency translation ratios, different PLL loop bandwidths, etc. These default configurations can be overwritten after power-up via I <sup>2</sup> C if the user so desires. LVCMOS/LVTTL interface levels. 0 = Configuration 0 (default) 1 = Configuration 1
17	S_A1	Input	Pulldown	I <sup>2</sup> C Address Bit 1. LVCMOS/LVTTL interface levels.
18	S_A0	Input	Pulldown	I <sup>2</sup> C Address Bit 0. LVCMOS/LVTTL interface levels.
25	V <sub>CCO</sub>	Power		Output supply pins for Q, nQ output. Either 2.5V or 3.3V.
26, 27	nQ, Q	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
28	OE	Input	Pullup	Active High Output Enable for Q, nQ. LVCMOS/LVTTL interface levels. 0 = Output pins high-impedance 1 = Output switching (default)
30	LOCK_IND	Output		Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels.
33, 34	LF0, LF1	Analog I/O		Loop filter connection node pins. LF0 is the output. LF1 is the input.
36	V <sub>CCA</sub>	Power		Analog supply voltage. See Applications section for details on how to connect this pin.
37	HOLDOVER	Output		Alarm output reflecting if the device is in a holdover state. LVCMOS/LVTTL interface levels. 0 = Device is locked to a valid input reference 1 = Device is not locked to a valid input reference
38	CLK_BAD	Output		Alarm output reflecting the state of CLK. LVCMOS/LVTTL interface levels. 0 = Input Clock is switching within specifications 1 = Input Clock is out of specification
40	XTAL_BAD	Output		Alarm output reflecting the state of XTAL. LVCMOS/LVTTL interface levels. 0 = crystal is switching within specifications 1 = crystal is out of specification

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			3.5		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Functional Description

The IDT8T49N105I is designed to provide almost any desired output frequency within its operating range (0.98 - 1300MHz) from any input source in the operating range (8kHz - 710MHz). It is capable of synthesizing frequencies from a crystal or crystal oscillator source. The output frequency is generated regardless of the relationship to the input frequency. The output frequency will be exactly the required frequency in most cases. In most others, it will only differ from the desired frequency by a few ppb. IDT configuration software will indicate the frequency error, if any. The IDT8T49N105I can translate the desired output frequency from one of two input clocks. Again, no relationship is required between the input and output frequencies in order to translate to the output clock rate. In this frequency translation mode, a low-bandwidth, jitter attenuation option is available that makes use of an external fixed-frequency crystal or crystal oscillator to translate from a noisy input source. If the input clock is known to be fairly clean or if some modulation on the input needs to be tracked, then the high-bandwidth frequency translation mode can be used, without the need for the external crystal.

The input clock references and crystal input are monitored continuously and appropriate alarm outputs are raised both as register bits and hard-wired pins in the event of any out-of-specification conditions arising. Clock switching is supported in manual, revertive & non-revertive modes.

The IDT8T49N105I has two factory-programmed configurations that may be chosen from as the default operating state after reset. This is intended to allow the same device to be used in two different applications without any need for access to the I<sup>2</sup>C registers. These defaults may be over-written by I<sup>2</sup>C register access at any time, but those over-written settings will be lost on power-down. Please contact IDT if a specific set of power-up default settings is desired.

## Configuration Selection

The IDT8T49N105I comes with two factory-programmed default configurations. When the device comes out of power-up reset the selected configuration is loaded into operating registers. The IDT8T49N105I uses the state of the CONFIG pin or CONFIG register bit (controlled by the CFG\_PIN\_REG bit) to determine which configuration is active. When the output frequency is changed either via the CONFIG pin or via internal registers, the output behavior may not be predictable during the register writing and output settling periods. Devices sensitive to glitches or runt pulses may have to be reset once reconfiguration is complete.

Once the device is out of reset, the contents of the operating registers can be modified by write access from the I<sup>2</sup>C serial port. Users that have a custom configuration programmed may not require I<sup>2</sup>C access.

It is expected that the IDT8T49N105I will be used almost exclusively in a mode where the selected configuration will be used from device power-up without any changes during operation. For example, the device may be designed into a communications line card that supports different I/O modules such as a standard OC-12 module running at 622.08MHz or a (255/237) FEC rate OC-12 module running at 669.32MHz. The different I/O modules would result in a different level on the CONFIG pin which would select different divider

ratios within the IDT8T49N105I for the two different card configurations. Access via I<sup>2</sup>C would not be necessary for operation using either of the internal configurations.

## Operating Modes

The IDT8T49N105I has three operating modes which are set by the MODE\_SEL[1:0] bits. There are two frequency translator modes - low bandwidth and high bandwidth and a frequency synthesizer mode. The device will operate in the same mode regardless of which configuration is active.

Please make use of IDT-provided configuration applications to determine the best operating settings for the desired configurations of the device.

## Output Dividers & Supported Output Frequencies

In all 3 operating modes, the output stage behaves the same way, but different operating frequencies can be specified in the two configurations.

The internal VCO is capable of operating in a range anywhere from 1.995GHz - 2.6GHz. It is necessary to choose an integer multiplier of the desired output frequency that results in a VCO operating frequency within that range. The output divider stage N[10:0] is limited to selection of integers from 2 to 2046. Please refer to Table 3 for the values of N applicable to the desired output frequency.

**Table 3. Output Divider Settings & Frequency Ranges**

Register Setting	Frequency Divider	Minimum f <sub>OUT</sub> (MHz)	Maximum f <sub>OUT</sub> (MHz)
Nn[10:0]	N	(MHz)	(MHz)
000000000x	2	997.5	1300
0000000010	2	997.5	1300
0000000011	3	665	866.7
0000000100	4	498.75	650
0000000101	5	399	520
000000011x	6	332.5	433.3
000000100x	8	249.4	325
000000101x	10	199.5	260
000000110x	12	166.3	216.7
000000111x	14	142.5	185.7
000001000x	16	124.7	162.5
000001001x	18	110.8	144.4
...	Even N	1995 / N	2600 / N
111111111x	2046	0.98	1.27

### Frequency Synthesizer Mode

This mode of operation allows an arbitrary output frequency to be generated from a fundamental mode crystal input. For improved phase noise performance, the crystal input frequency may be doubled. As can be seen from the block diagram in Figure 1, only the upper feedback loop is used in this mode of operation. It is recommended that CLK be left unused in this mode of operation.

The upper feedback loop supports a delta-sigma fractional feedback divider. This allows the VCO operating frequency to be a non-integer multiple of the crystal frequency. By using an integer multiple only, lower phase noise jitter on the output can be achieved, however the use of the delta-sigma divider logic will provide excellent performance on the output if a fractional divisor is used.

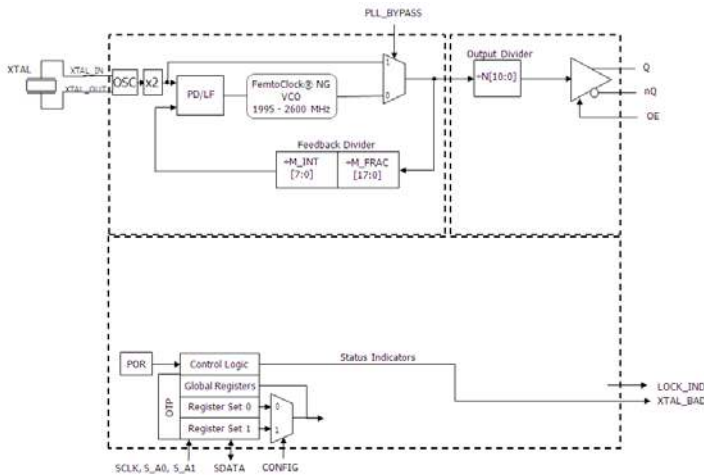


Figure 1. Frequency Synthesizer Mode Block Diagram

### High-Bandwidth Frequency Translator Mode

This mode of operation is used to translate the input clock of the same nominal frequency into an output frequency with little jitter attenuation. As can be seen from the block diagram in Figure 2, similarly to the Frequency Synthesizer mode, only the upper feedback loop is used.

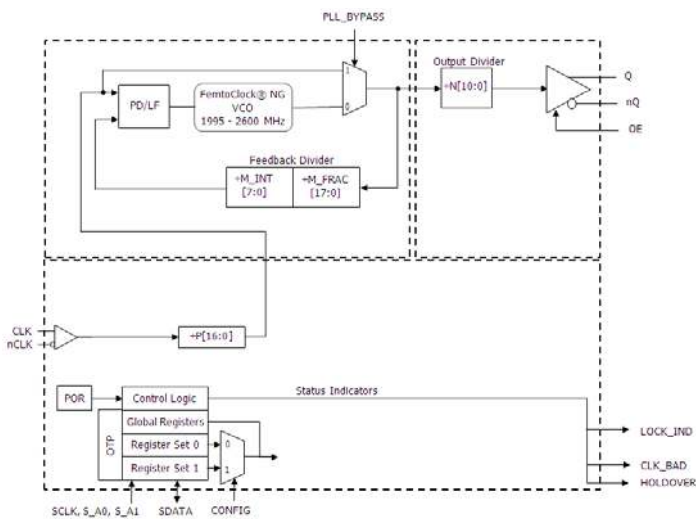


Figure 2. High Bandwidth Frequency Translator Mode Block Diagram

The input reference frequency range is now extended up to 710MHz. A pre-divider stage P is needed to keep the operating frequencies at the phase detector within limits.

### Low-Bandwidth Frequency Translator Mode

As can be seen from the block diagram in Figure 3, this mode involves two PLL loops. The lower loop with the large integer dividers is the low bandwidth loop and it sets the output-to-input frequency translation ratio. This loop drives the upper DCXO loop (digitally controlled crystal oscillator) via an analog-digital converter.

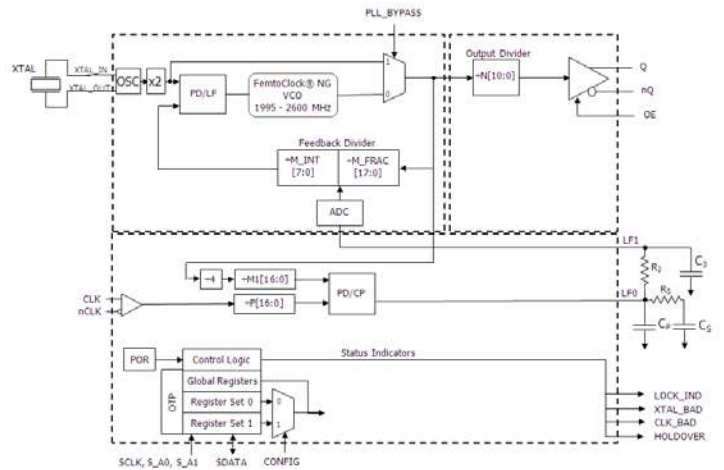


Figure 3. Low Bandwidth Frequency Translator Mode Block Diagram

The pre-divider stage is used to scale down the input frequency by an integer value to achieve a frequency in this range. By dividing down the feedback VCO operating frequency by the integer divider M1[16:0] to as close as possible to the same frequency, exact output frequency translations can be achieved. The phase detector of the lower loop is designed to work with frequencies in the 8kHz - 16kHz range. For improved phase noise performance, the crystal input frequency may be doubled.

### Alarm Conditions & Status Bits

The IDT8T49N105I monitors a number of conditions and reports their status via both output pins and register bits. All alarms will behave as indicated below in all modes of operation, but some of the conditions monitored have no valid meaning in some operating modes. For example, the status of CLK\_BAD is not relevant in Frequency Synthesizer mode. The output will still be active and it is left to the user to determine which to monitor and how to respond to them based on the known operating mode.

**LOCK\_IND** - This status is asserted on the pin & register bit when the PLL is locked to the appropriate input reference for the chosen mode of operation. The status bit will not assert until frequency lock has been achieved, but will de-assert once lock is lost.



XTAL\_BAD - indicates if valid edges are being received on the crystal input. Detection is performed by comparing the input to the feedback signal at the upper loop's Phase / Frequency Detector (PFD). If three edges are received on the feedback without an edge on the crystal input, the XTAL\_BAD alarm is asserted on the pin & register bit. Once an edge is detected on the crystal input, the alarm is immediately deasserted.

CLK\_BAD - indicates if valid edges are being received on the CLK reference input. Detection is performed by comparing the input to the feedback signal at the appropriate Phase / Frequency Detector (PFD). When operating in high-bandwidth mode, the feedback at the upper PFD is used. In low-bandwidth mode, the feedback at the lower PFD is used. If three edges are received on the feedback without an edge on the divided down ( $\div P$ ) CLK reference input, the CLK\_BAD alarm is asserted on the pin & register bit. Once an edge is detected on the CLK reference input, the alarm is deasserted.

HOLDOVER - indicates that the device is not locked to a valid input reference clock. This can occur in Manual switchover mode if the reference input has gone bad.

## Holdover / Free-run Behavior

When the input reference has failed, the IDT8T49N105I will enter holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state. In both cases, once the input reference is lost, the PLL will stop making adjustments to the output phase. If operating in Low Bandwidth Frequency Translation mode, the PLL will continue to reference itself to the local oscillator and will hold its output phase and frequency in relation to that source. Output stability is determined by the stability of the local oscillator in this case. However, if operating in High Bandwidth Frequency Translation mode, the PLL no longer has any frequency reference to use and output stability is now determined by the stability of the internal VCO. Once the input reference recovers, the IDT8T49N105I will switch back to that reference.

**Table 4A. I<sup>2</sup>C Device Slave Address**

1	1	0	1	1	S_A1	S_A0	R/W
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**Table 4B. Block Write Operation**

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W (0)	A C K	Address Byte (P)	A C K	Data Byte (P)	A C K	Data Byte (P+1)	A C K	Data Byte ...	A C K	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

## Output Configuration

The output voltage of the IDT8T49N105I may be less than or equal to the core voltage (3.3V or 2.5V) the rest of the device is operating from. The output voltage level used is supplied on the V<sub>CCO</sub> pin.

The output is selectable as an LVDS or LVPECL output type via the Q\_TYPE register bit. This selection bit is provided in each configuration to allow different output type settings under each configuration.

The output can be enabled also via both register control bits and input pins. When the OE register bit and OE pin are enabled, then the output is enabled. The OE register bit defaults to enabled so that by default the output can be directly controlled by the input pin. Similarly, the input pin is provisioned with weak pull-ups so that if they are left unconnected, the output state can be directly controlled by the register bit. When the differential output is in the disabled state, it will show a high impedance condition.

## Serial Interface Configuration Description

The IDT8T49N105I has an I<sup>2</sup>C-compatible configuration interface to access any of the internal registers (Table 4D) for frequency and PLL parameter programming. The IDT8T49N105I acts as a slave device on the I<sup>2</sup>C bus and has the address 0b11011xx, where xx is set by the values on the S\_A0 & S\_A1 pins (see Table 4A for details). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 4D) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see table 4B, 4C). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate I<sup>2</sup>C the read or write transfer after accessing byte #23.

For full electrical I<sup>2</sup>C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50k $\Omega$  typical.

Note: if a different device slave address is desired, please contact IDT.

Table 4C. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	A C K	Address Byte (P)	A C K	Repeated START	Slave Address	R (1)	A C K	Data Byte (P)	A C K	Data Byte (P+1)	A C K	Data Byte ...	A C K	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

## Register Descriptions

Please consult IDT for configuration software and/or programming guides to assist in selection of optimal register settings for the desired configurations.

Table 4D. I<sup>2</sup>C Register Map

Reg	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	MFRAC0[17]	MFRAC0[16]	MFRAC0[15]	MFRAC0[14]	MFRAC0[13]	MFRAC0[12]	MFRAC0[11]	MFRAC0[10]
1	00001	MFRAC1[17]	MFRAC1[16]	MFRAC1[15]	MFRAC1[14]	MFRAC1[13]	MFRAC1[12]	MFRAC1[11]	MFRAC1[10]
2	00010	MFRAC0[9]	MFRAC0[8]	MFRAC0[7]	MFRAC0[6]	MFRAC0[5]	MFRAC0[4]	MFRAC0[3]	MFRAC0[2]
3	00011	MFRAC1[9]	MFRAC1[8]	MFRAC1[7]	MFRAC1[6]	MFRAC1[5]	MFRAC1[4]	MFRAC1[3]	MFRAC1[2]
4	00100	MFRAC0[1]	MFRAC0[0]	MINT0[7]	MINT0[6]	MINT0[5]	MINT0[4]	MINT0[3]	MINT0[2]
5	00101	MFRAC1[1]	MFRAC1[0]	MINT1[7]	MINT1[6]	MINT1[5]	MINT1[4]	MINT1[3]	MINT1[2]
6	00110	MINT0[1]	MINT0[0]	P0[16]	P0[15]	P0[14]	P0[13]	P0[12]	P0[11]
7	00111	MINT1[1]	MINT1[0]	P1[16]	P1[15]	P1[14]	P1[13]	P1[12]	P1[11]
8	01000	P0[10]	P0[9]	P0[8]	P0[7]	P0[6]	P0[5]	P0[4]	P0[3]
9	01001	P1[10]	P1[9]	P1[8]	P1[7]	P1[6]	P1[5]	P1[4]	P1[3]
10	01010	P0[2]	P0[1]	P0[0]	M1_0[16]	M1_0[15]	M1_0[14]	M1_0[13]	M1_0[12]
11	01011	P1[2]	P1[1]	P1[0]	M1_1[16]	M1_1[15]	M1_1[14]	M1_1[13]	M1_1[12]
12	01100	M1_0[11]	M1_0[10]	M1_0[9]	M1_0[8]	M1_0[7]	M1_0[6]	M1_0[5]	M1_0[4]
13	01101	M1_1[11]	M1_1[10]	M1_1[9]	M1_1[8]	M1_1[7]	M1_1[6]	M1_1[5]	M1_1[4]
14	01110	M1_0[3]	M1_0[2]	M1_0[1]	M1_0[0]	N0[10]	N0[9]	N0[8]	N0[7]
15	01111	M1_1[3]	M1_1[2]	M1_1[1]	M1_1[0]	N1[10]	N1[9]	N1[8]	N1[7]
16	10000	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]	BW0[6]
17	10001	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]	BW1[6]
18	10010	BW0[5]	BW0[4]	BW0[3]	BW0[2]	BW0[1]	BW0[0]	RSVD	Q_TYPE0
19	10011	BW1[5]	BW1[4]	BW1[3]	BW1[2]	BW1[1]	BW1[0]	RSVD	Q_TYPE1
20	10100	MODE_SEL[1]	MODE_SEL[0]	CONFIG	CFG_PIN_REG	0	OE	Rsvd	Rsvd
21	10101	0	1	1	0	ADC_RATE[1]	ADC_RATE[0]	LCK_WIN[1]	LCK_WIN[0]
22	10110	1	0	1	0	DBL_XTAL	0	0	0
23	10111		HOLDOVER	RSVD	CLK_BAD	XTAL_BAD	LOCK_IND	Rsvd	Rsvd

## Register Bit Color Key

Configuration 0 Specific Bits
Configuration 1 Specific Bits
Global Control & Status Bits



The register bits described in Table 4E are duplicated, with one set applying for Configuration 0 and the other for Configuration 1. The functions of the bits are identical, but only apply when the

configuration they apply to is enabled. Replace the lowercase n in the bit field description with 0 or 1 to find the field's location in the bitmap in Table 4D.

**Table 4E. Configuration-Specific Control Bits**

Register Bits	Function
Q_TYPE <sub>n</sub>	Determines the output type for output pair Q, nQ for Configuration n. 0 = LVPECL 1 = LVDS
P <sub>n</sub> [16:0]	Reference Pre-Divider for Configuration n.
M1_ <sub>n</sub> [16:0]	Integer Feedback Divider in Lower Feedback Loop for Configuration n.
M_INT <sub>n</sub> [7:0]	Feedback Divider, Integer Value in Upper Feedback Loop for Configuration n.
M_FRAC <sub>n</sub> [17:0]	Feedback Divider, Fractional Value in Upper Feedback Loop for Configuration n.
N <sub>n</sub> [10:0]	Output Divider for Configuration n.
BW <sub>n</sub> [6:0]	Internal Operation Settings for Configuration n. Please use IDT IDT8T49N105I Configuration Software to determine the correct settings for these bits for the specific configuration. Alternatively, please consult with IDT directly for further information on the functions of these bits. The function of these bits are explained in Tables 4J and 4K.

**Table 4F. Global Control Bits**

Register Bits	Function
MODE_SEL[1:0]	PLL Mode Select 00 = Low Bandwidth Frequency Translator 01 = Frequency Synthesizer 10 = High Bandwidth Frequency Translator 11 = High Bandwidth Frequency Translator
CFG_PIN_REG	Configuration Control. Selects whether the configuration selection function is under pin or register control. 0 = Pin Control 1 = Register Control
CONFIG	Configuration Selection. Selects whether the device uses the register configuration set 0 or 1. This bit only has an effect when the CONFIG_PIN_REG bit is set to 1 to enable register control.
OE	Output Enable Control for Q, nQ output. Both the register bit and the corresponding Output Enable pin OE must be asserted to enable the Q, nQ output. 0 = Output Q, nQ disabled 1 = Output Q, nQ under control of the OE pin
Rsvd	Reserved bits - user should write a '0' to these bit positions if a write to these registers is needed
ADC_RATE[1:0]	Sets the ADC sampling rate in Low-Bandwidth Mode as a fraction of the crystal input frequency. 00 = Crystal Frequency / 16 01 = Crystal Frequency / 8 10 = Crystal Frequency / 4 (recommended) 11 = Crystal Frequency / 2
LCK_WIN[1:0]	Sets the width of the window in which a new reference edge must fall relative to the feedback edge: 00 = 2usec (recommended), 01 = 4usec, 10 = 8usec, 11 = 16usec
DBL_XTAL	When set, this bit will double the frequency of the crystal input before applying it to the Phase_Frequency Detector.

**Table 4G. Global Status Bits**

Register Bits	Function
CLK_BAD	Status Bit for input clock 0. This function is mirrored in the CLK_BAD pin. 0 = input CLK is good 1 = input CLK is bad. Self clears when input clock returns to good status
XTAL_BAD	Status Bit. This function is mirrored on the XTALBAD pin. 0 = crystal input good 1 = crystal input bad. Self-clears when the XTAL clock returns to good status
LOCK_IND	Status bit. This function is mirrored on the LOCK_IND pin. 0 = PLL unlocked 1 = PLL locked
HOLDOVER	Status Bit. This function is mirrored on the HOLDOVER pin. 0 = Input to phase detector is within specifications and device is tracking to it 1 = Phase detector input is not within specifications and DCXO is frozen at last value

**Table 4J. BW[6:0] Bits**

Mode	BW[6]	BW[5]	BW[4]	BW[3]	BW[2]	BW[1]	BW[0]
Synthesizer Mode	PLL2_LF[1]	PLL2_LF[0]	DSM_ORD	DSM_EN	PLL2_CP[1]	PLL2_CP[0]	PLL2_LOW_ICP
High-Bandwidth Mode	PLL2_LF[1]	PLL2_LF[0]	DSM_ORD	DSM_EN	PLL2_CP[1]	PLL2_CP[0]	PLL2_LOW_ICP
Low-Bandwidth Mode	ADC_GAIN[3]	ADC_GAIN[2]	ADC_GAIN[1]	ADC_GAIN[0]	PLL1_CP[1]	PLL1_CP[0]	PLL2_LOW_ICP

**Table 4K. Functions of Fields in BW[6:0]**

Register Bits	Function
PLL2_LF[1:0]	Sets loop filter values for upper loop PLL in Frequency Synthesizer & High-Bandwidth modes. Defaults to setting of 00 when in Low Bandwidth Mode. See Table 4L for settings.
DSM_ORD	Sets Delta-Sigma Modulation to 2nd (0) or 3rd order (1) operation
DSM_EN	Enables Delta-Sigma Modulator 0 = Disabled - feedback in integer mode only 1 = Enabled - feedback in fractional mode
PLL2_CP[1:0]	Upper loop PLL charge pump current settings: 00 = 173 $\mu$ A (defaults to this setting in Low Bandwidth Mode) 01 = 346 $\mu$ A 10 = 692 $\mu$ A 11 = reserved
PLL2_LOW_ICP	Reduces Charge Pump current by 1/3 to reduce bandwidth variations resulting from higher feedback register settings or high VCO operating frequency (>2.4GHz).
ADC_GAIN[3:0]	Gain setting for ADC in Low Bandwidth Mode.
PLL1_CP[1:0]	Lower loop PLL charge pump current settings (lower loop is only used in Low Bandwidth Mode): 00 = 800 $\mu$ A 01 = 400 $\mu$ A 10 = 200 $\mu$ A 11 = 100 $\mu$ A

**Table 4L. High Bandwidth Frequency and Frequency Synthesizer Bandwidth Settings**

Desired Bandwidth	PLL2_CP		PLL2_LOW_ICP	PLL2_LF					
<b>Frequency Synthesizer Mode</b>									
200kHz	00		1	00					
400kHz	01		1	01					
800kHz	10		1	10					
2MHz	10		1	11					
<b>High Bandwidth Frequency Translator Mode</b>									
200kHz	00		1	00					
400kHz	01		1	01					
800kHz	10		1	10					
4MHz	10		0	11					

NOTE: To achieve 4MHz bandwidth, reference to the phase detector should be 80MHz.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	3.63V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to 2V -0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$ (LVCMOS)	-0.5V to $V_{CCO} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	32.4°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 5A. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.30$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				332	mA
$I_{CCA}$	Analog Supply Current				30	mA

**Table 5B. LVPECL Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.30$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				332	mA
$I_{CCA}$	Analog Supply Current				30	mA

**Table 5C. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.26$	2.5	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				319	mA
$I_{CCA}$	Analog Supply Current				26	mA

**Table 5D. LVDS Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.30$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{CC}$	Power Supply Current				284	mA
$I_{CCA}$	Analog Supply Current				30	mA
$I_{CCO}$	Output Supply Current				22	mA

**Table 5E. LVDS Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.26$	2.5	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{CC}$	Power Supply Current				275	mA
$I_{CCA}$	Analog Supply Current				26	mA
$I_{CCO}$	Output Supply Current				22	mA

**Table 5F. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{CC} = 3.3\text{V}$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5\text{V}$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{CC} = 3.3\text{V}$	-0.3		0.8	V
			$V_{CC} = 2.5\text{V}$	-0.3		0.7	V
$I_{IH}$	Input High Current	CONFIG, PLL_BYPASS, S_A[0:1]	$V_{CC} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			150	$\mu\text{A}$
		OE, SCLK, SDATA	$V_{CC} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CONFIG, PLL_BYPASS, S_A[0:1]	$V_{CC} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		OE, SCLK, SDATA	$V_{CC} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage	LOCK_IND, HOLDOVER, SDATA, CLK_BAD, XTAL_BAD	$V_{CC} = 3.3\text{V} \pm 5\%$ , $I_{OH} = -8\text{mA}$	2.6			V
			$V_{CC} = 2.5\text{V} \pm 5\%$ , $I_{OH} = -8\text{mA}$	1.8			V
$V_{OL}$	Output Low Voltage	LOCK_IND, HOLDOVER, SDATA, CLK_BAD, XTAL_BAD	$V_{CC} = 3.3\text{V} \pm 5\%$ or $2.5\text{V} \pm 5\%$ , $I_{OL} = 8\text{mA}$			0.5	V

**Table 5G. Differential DC Characteristics,  $V_{CC} = V_{CCO} = 3.3\text{V} \pm 5\%$  or  $2.5\text{V} \pm 5\%$ ,  $V_{EE} = 0\text{V}$ ,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, nCLK	$V_{CC} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK	$V_{CC} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		nCLK	$V_{CC} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Voltage; Note 1			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2			$V_{EE} + 0.5$		$V_{CC} - 1.0$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3v.

NOTE 2: Common mode input voltage is defined as the crosspoint.

**Table 5H. LVPECL DC Characteristics,  $V_{CC} = V_{CCO} = 3.3\text{V} \pm 5\%$ ,  $V_{EE} = 0\text{V}$ ,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.1$		$V_{CCO} - 0.7$	V
$V_{OL}$	Output Low Voltage NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2\text{V}$ .



**Table 5I. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.1$		$V_{CCO} - 0.8$	V
$V_{OL}$	Output Low Voltage NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .**Table 5J. LVDS DC Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.125		1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 5K. LVDS DC Characteristics,  $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.125		1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 6. Input Frequency Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{IN}$	Input Frequency	XTAL_IN, XTAL_OUT; NOTE 1	16		40	MHz	
		CLK, nCLK	High Bandwidth Mode	16		710	MHz
			Low Bandwidth Mode	0.008		710	MHz
		SCLK				5	MHz

NOTE 1: For the input crystal and CLK, nCLK frequency range, the M value must be set for the VCO to operate within the 1995MHz to 2600MHz range.

**Table 7. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		16		40	MHz
Equivalent Series Resistance (ESR)				100	$\Omega$
Shunt Capacitance				7	pF
Load Capacitance (CL)			12		pF

## AC Electrical Characteristics

**Table 8. AC Characteristics**,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ , or  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$  (LVPECL Only),  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		0.98		1300	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter; NOTE 2 Integer Divide Ratio	Synth Mode (Integer FB), $f_{OUT} = 400MHz$ , 40MHz XTAL, Integration Range: 12kHz – 40MHz		285	446	fs
		Synth Mode (FracN FB), $f_{OUT} = 698.81MHz$ , 40MHz XTAL, Integration Range: 12kHz – 20MHz		363	521	fs
		HBW Mode, (NOTE 1) $f_{IN} = 133.33MHz$ , $f_{OUT} = 400MHz$ , Integration Range: 12kHz – 20MHz		313	490	fs
		LBW Mode (FracN), 40MHz XTAL, $f_{IN} = 19.44MHz$ , $f_{OUT} = 155.52MHz$ , Integration Range: 12kHz – 20MHz (LVDS Output)		439	670	fs
		LBW Mode (FracN), 40MHz XTAL, $f_{IN} = 25MHz$ , $f_{OUT} =$ 161.1328125MHz, Integration Range: 12kHz – 20MHz (LVDS Output)		450	670	fs
$f_{jit}(per)$	RMS Period Jitter NOTE 3	LVPECL Outputs		2.2	5.3	ps
		LVDS Output		5.1	8.7	ps
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 3	Frequency Synthesizer Mode			30	ps
		Frequency Translator Mode			40	ps
$t_R / t_F$	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	100	520	ps
		LVDS Outputs	20% to 80%	80	520	ps
odc	Output Duty Cycle	$f_{OUT} < 600MHz$	45		55	%
		$f_{OUT} \geq 600MHz$	40		60	%
$t_{SET}$	Output Re-configuration Settling Time	from falling edge of the 8th SCLK for a register change		200		ns
		from edge on CONFIG pin		10		ns

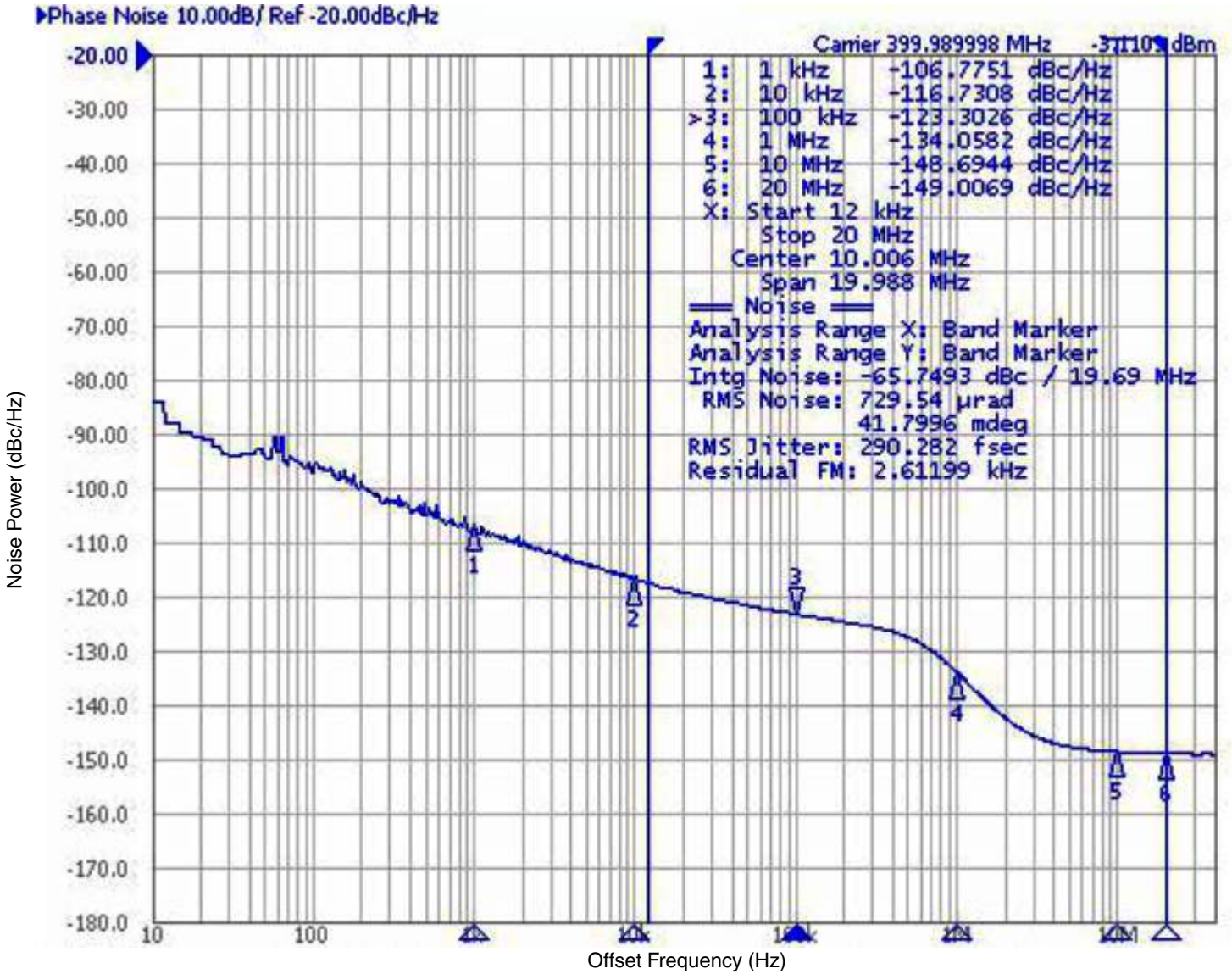
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured using a Rohde & Schwarz SMA100 Signal Generator, 9kHz to 6GHz as the input source.

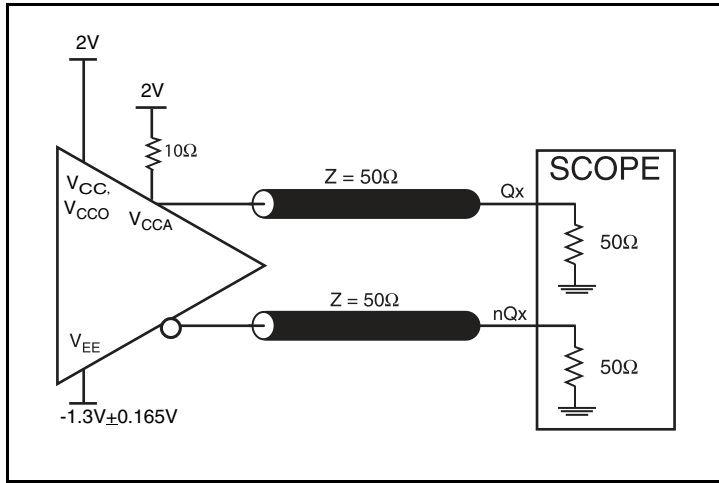
NOTE 2: RMS Phase Jitter are measured with DBL\_XTAL bit set to 1 and crystal CL = 12pf.

NOTE 3: This parameter is defined in accordance with Jedec Standard 65.

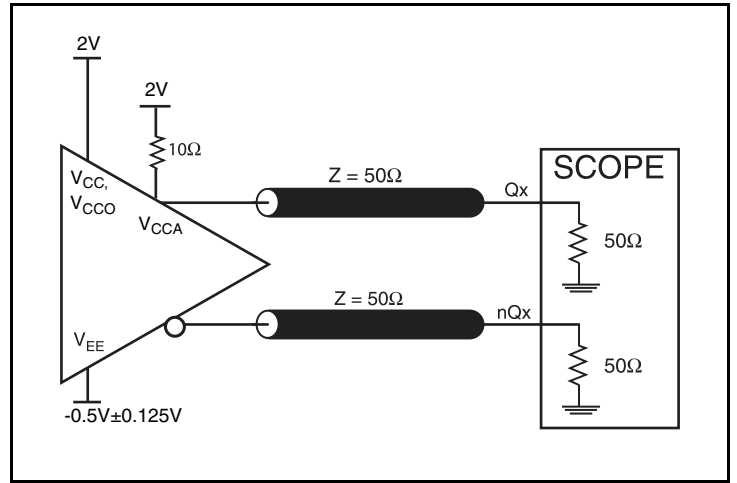
### Typical Phase Noise at 400MHz



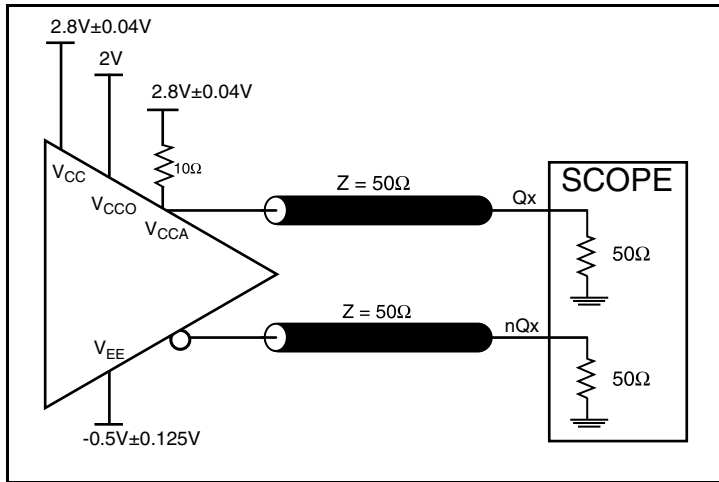
## Parameter Measurement Information



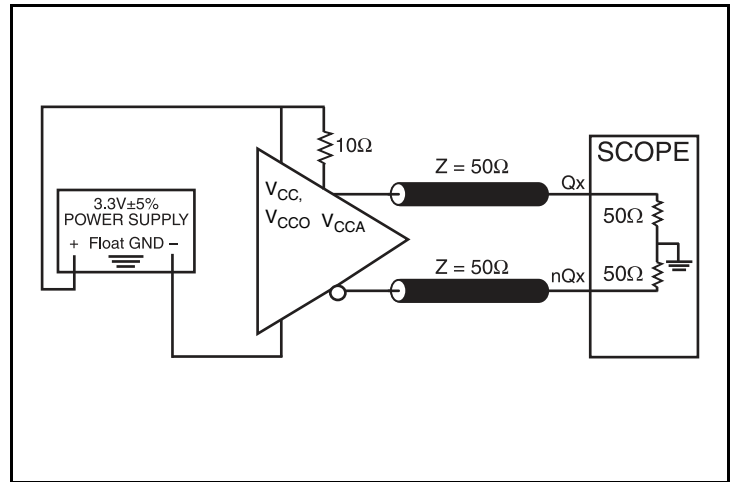
**3.3 Core/3.3V LVPECL Output Load Test Circuit**



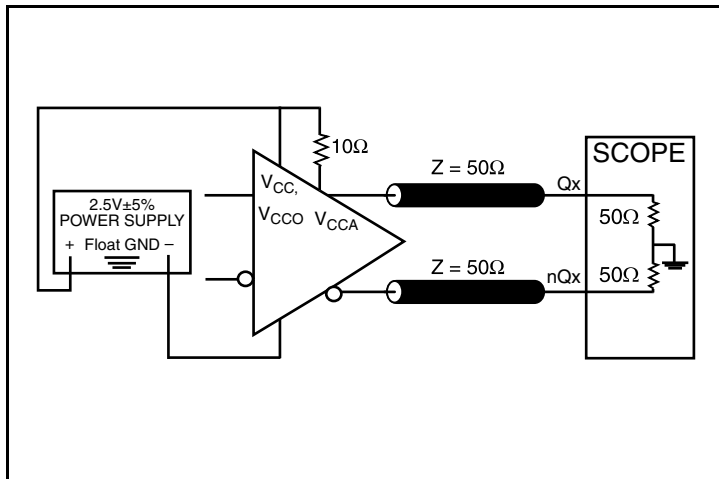
**2.5 Core/2.5V LVPECL Output Load Test Circuit**



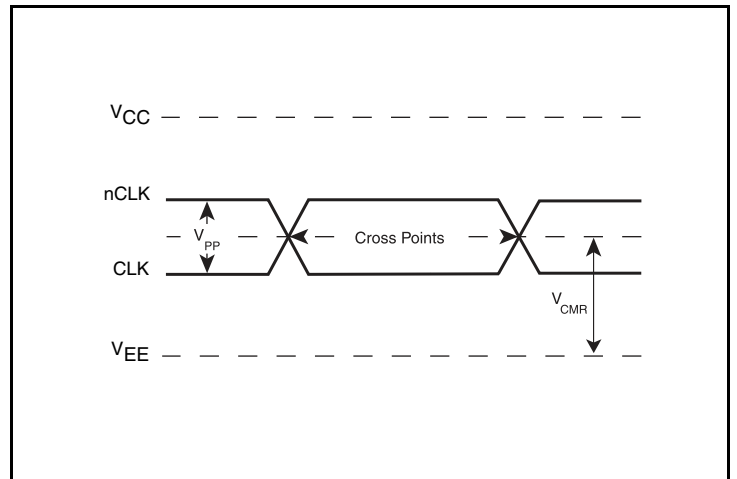
**3.3 Core/2.5V LVPECL Output Load Test Circuit**



**3.3 Core/3.3V LVDS Output Load Test Circuit**

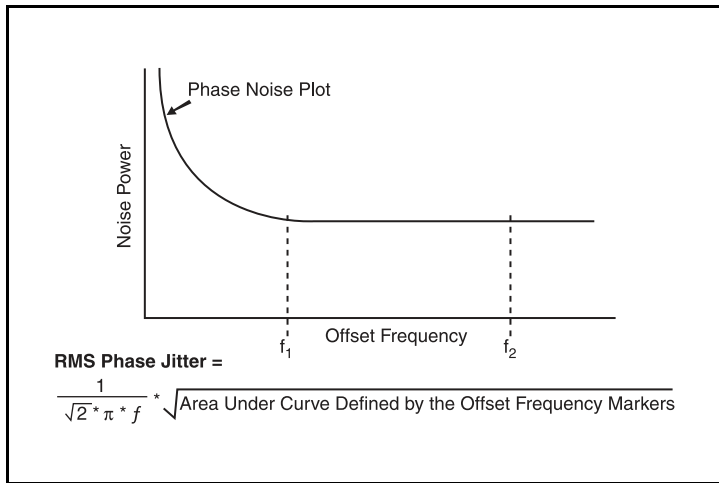


**2.5 Core/2.5V LVDS Output Load Test Circuit**

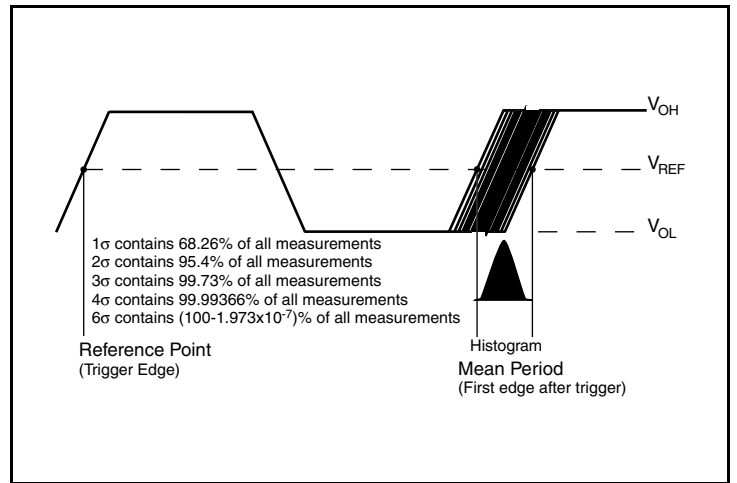


**Differential Input Levels**

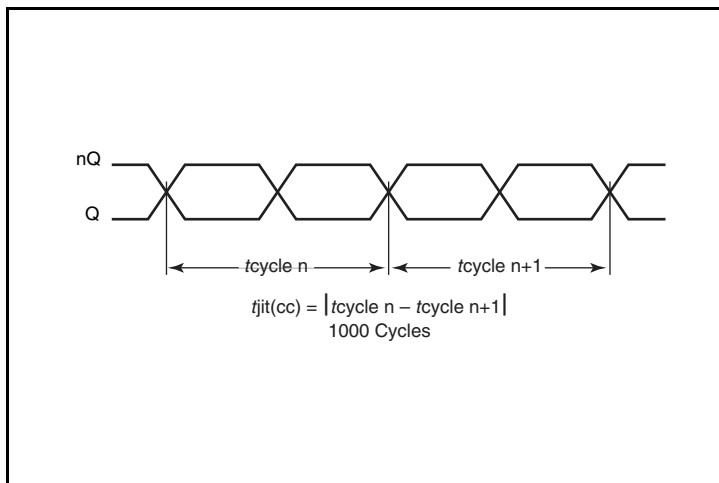
### Parameter Measurement Information, continued



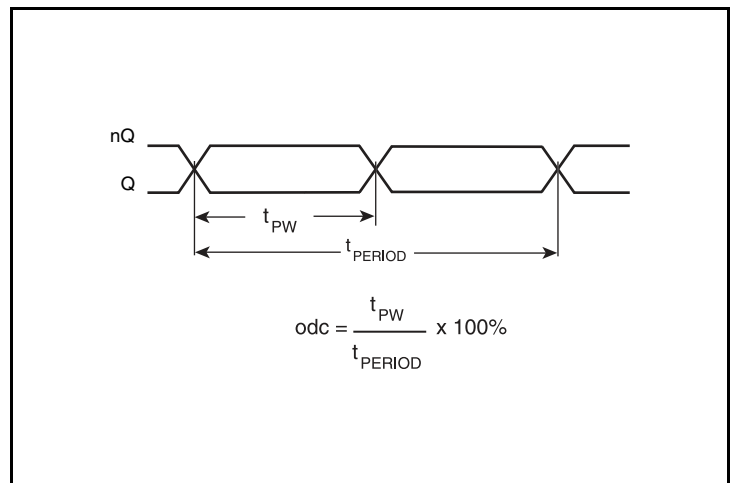
**RMS Phase Jitter**



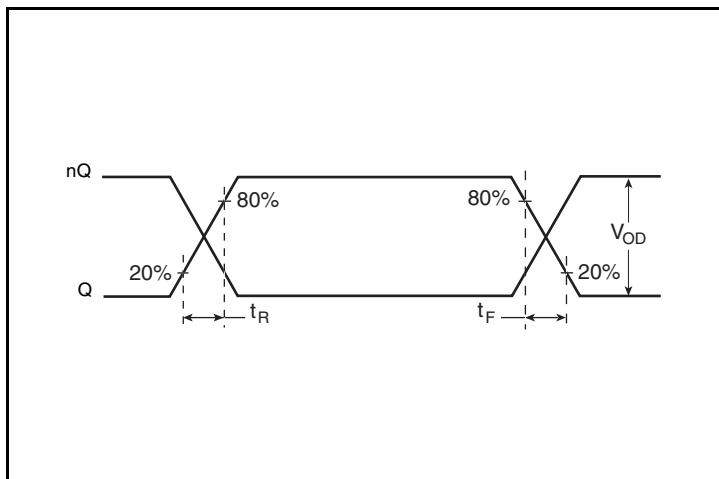
**Period Jitter**



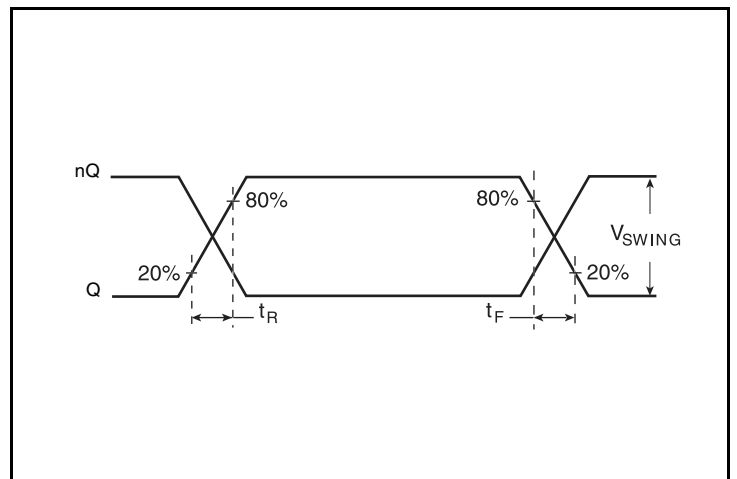
**Cycle-to-Cycle Jitter**



**Differential Output Duty Cycle/Output Pulse Width/Period**



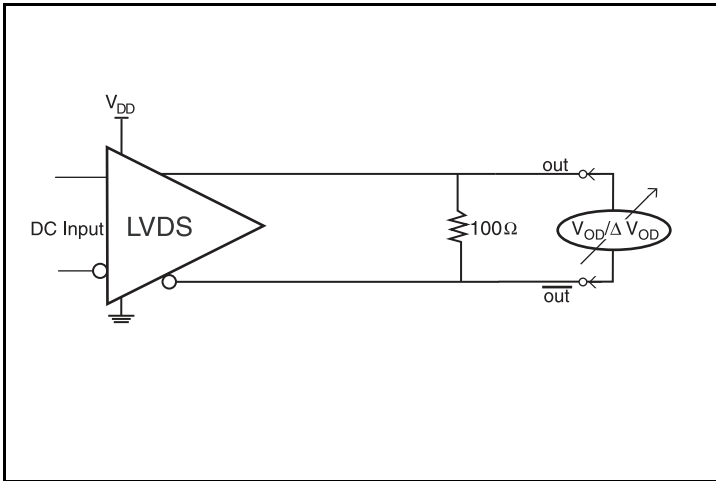
**LVDS Output Rise/Fall Time**



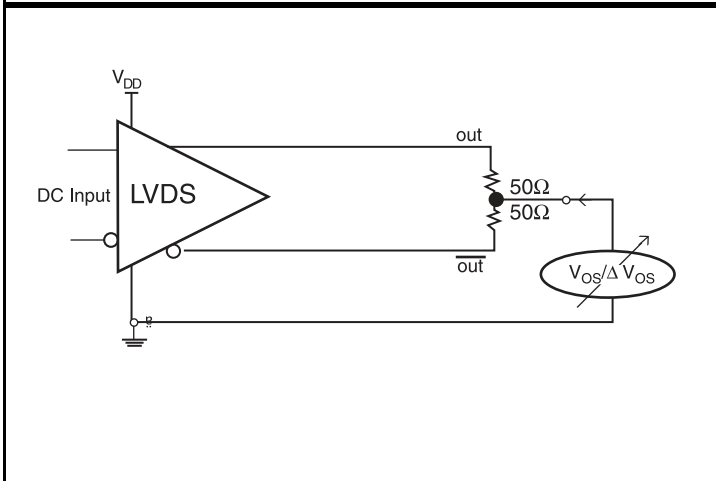
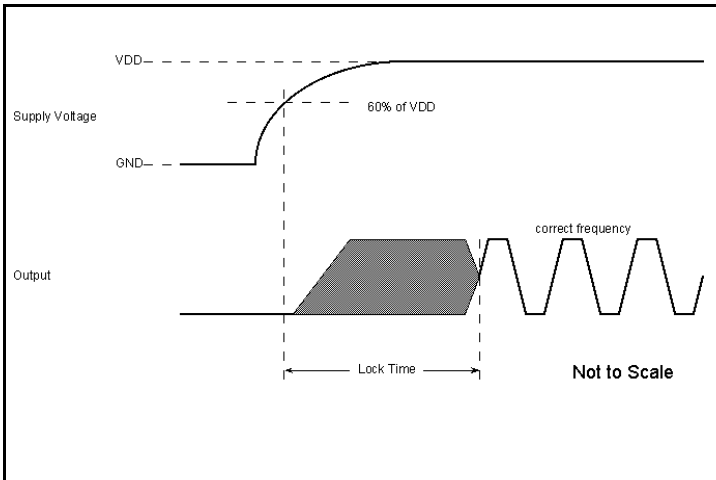
**LVPECL Output Rise/Fall Time**

# Parameter Measurement Information, continued

## Offset Voltage Setup



## Differential Output Voltage Setup





## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

##### CLK/nCLK Inputs

For applications not requiring the use of either differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground. It is recommended that CLK, nCLK be left unconnected in frequency synthesizer mode.

##### LVC MOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating there should be no trace attached.

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

### Recommended Values for Low-Bandwidth Mode Loop Filter

External loop filter components are not needed in Frequency Synthesizer or High-Bandwidth modes. In Low-Bandwidth mode, the loop filter structure and components are recommended. Please consult IDT if other values are needed.

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

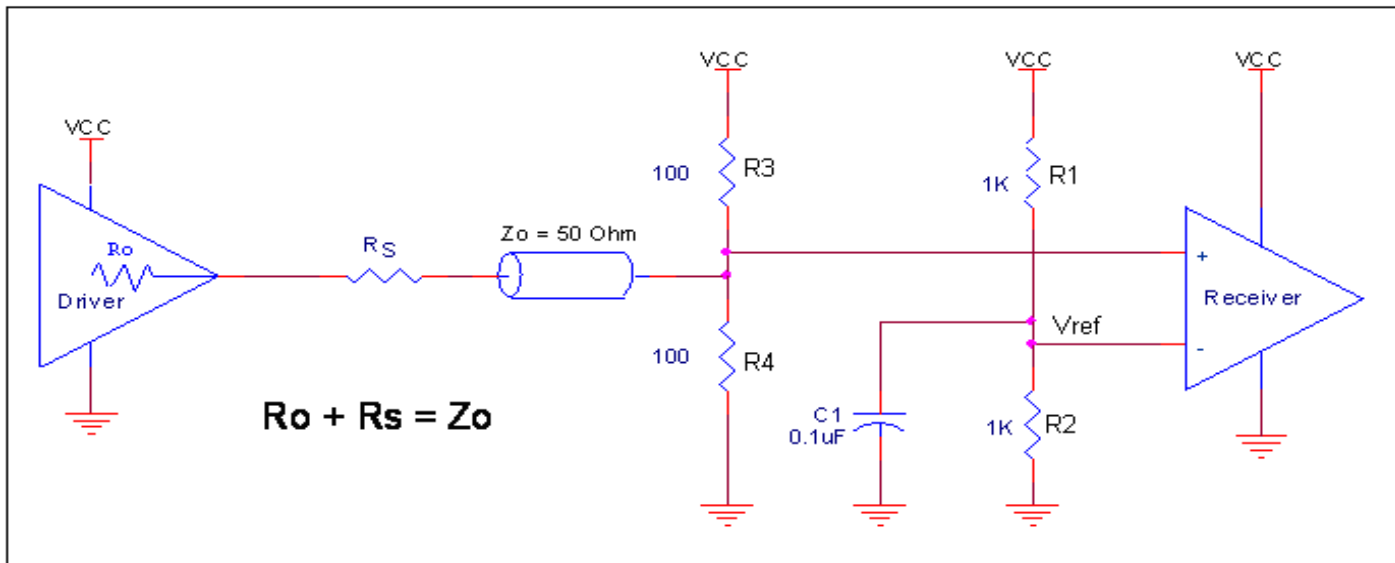
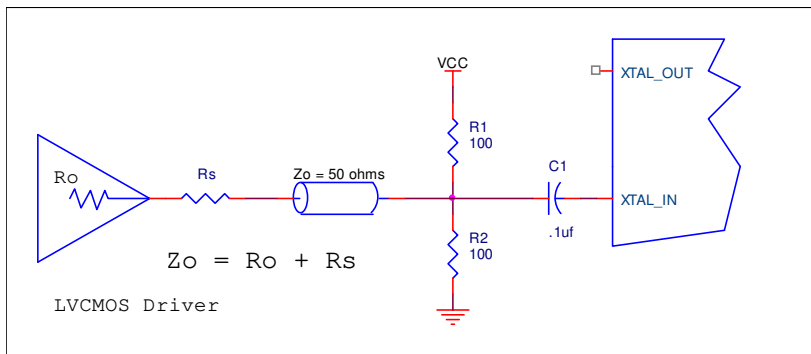


Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

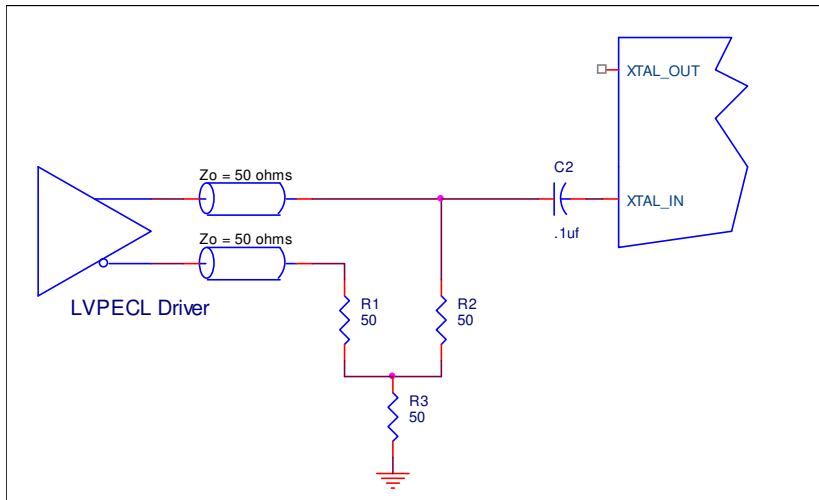
## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 5A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 5B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 5A. General Diagram for LVCMOS Driver to XTAL Input Interface**

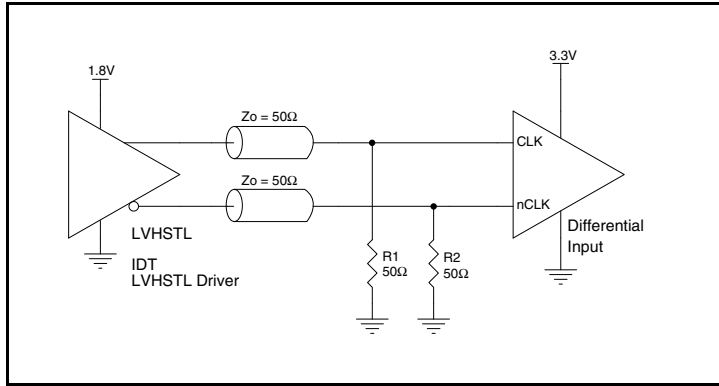


**Figure 5B. General Diagram for LVPECL Driver to XTAL Input Interface**

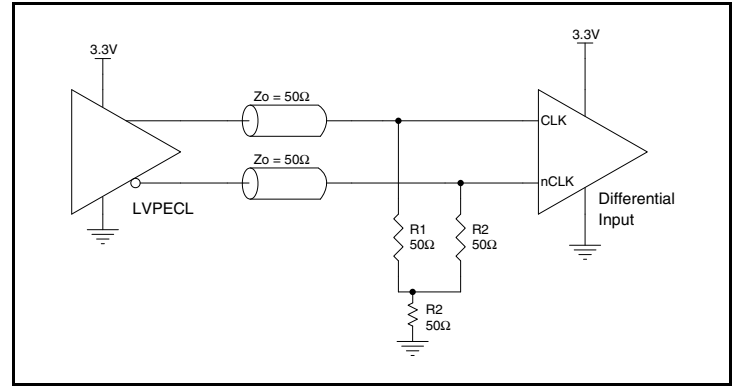
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 6A to 6E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

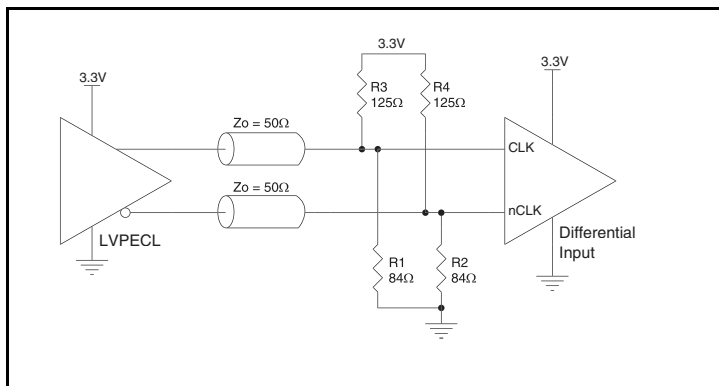
with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 6A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



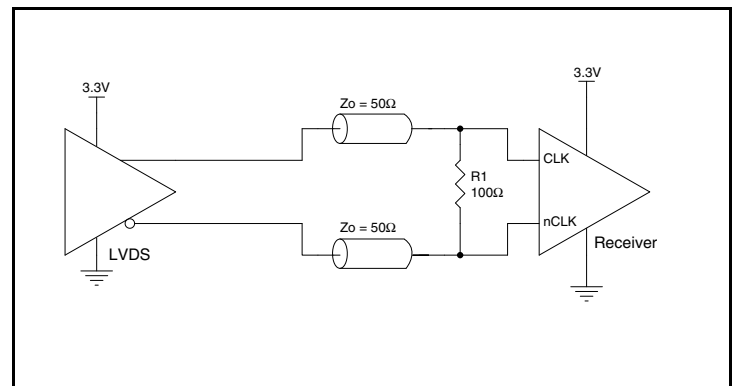
**Figure 6A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



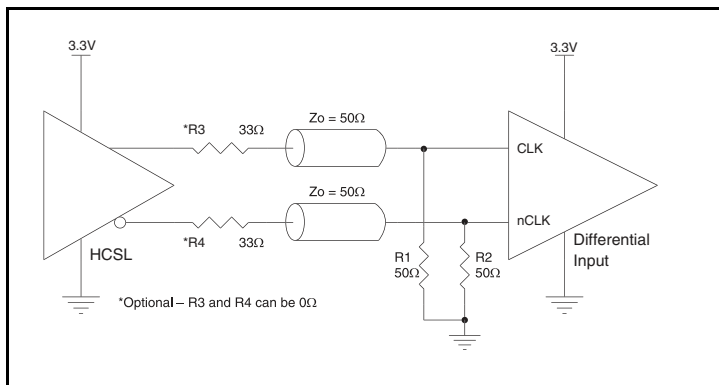
**Figure 6B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 6C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 6D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

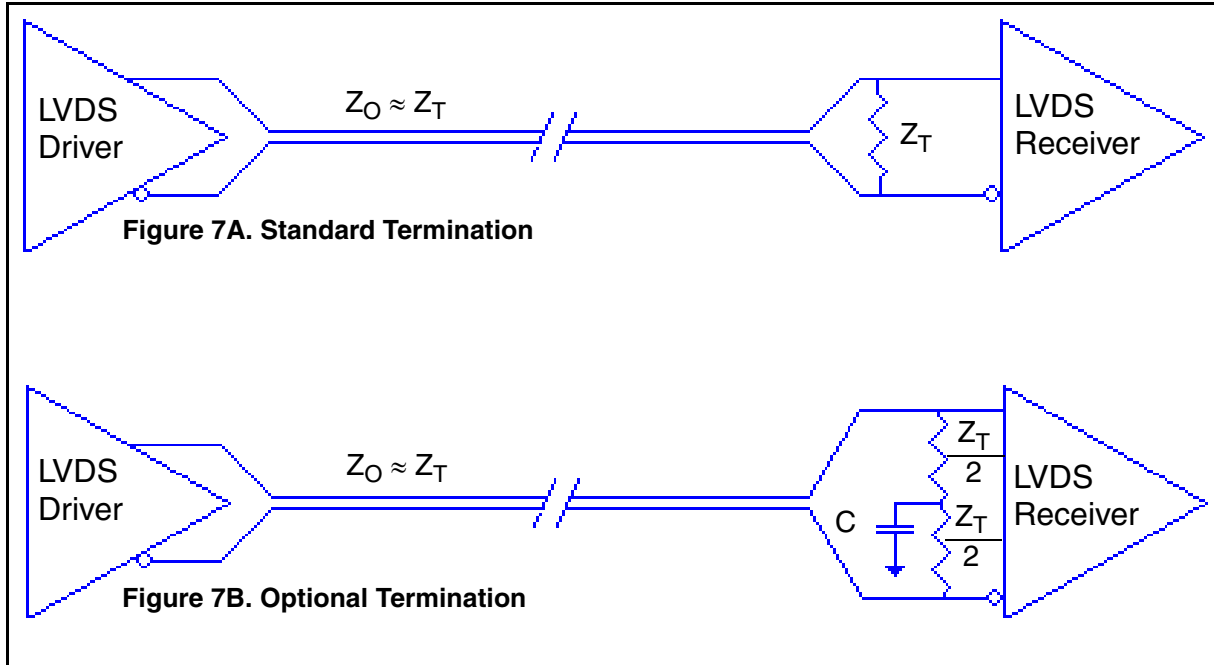


**Figure 6E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 7A* can be used with either type of output structure. *Figure 7B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

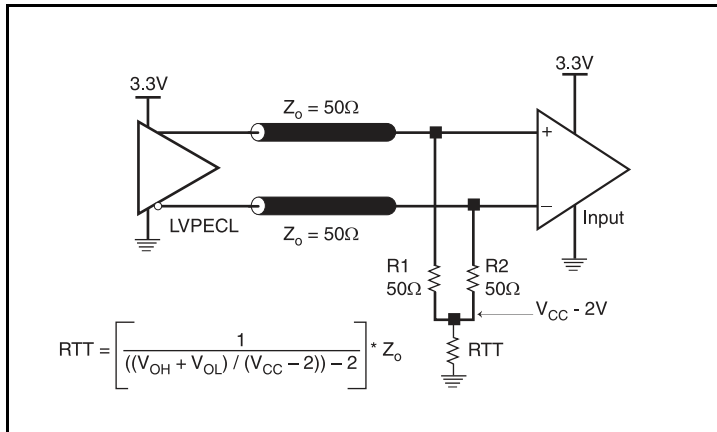


Figure 8A. 3.3V LVPECL Output Termination

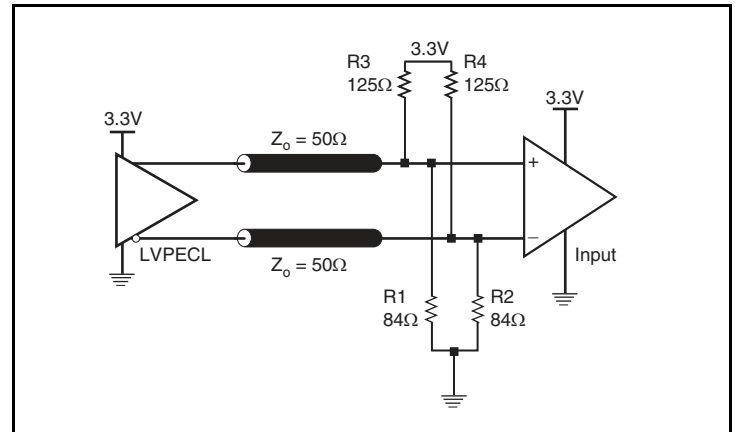


Figure 8B. 3.3V LVPECL Output Termination



### Termination for 2.5V LVPECL Outputs

Figure 9A and Figure 9B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC0} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to ground

level. The R3 in Figure 9B can be eliminated and the termination is shown in Figure 9C.

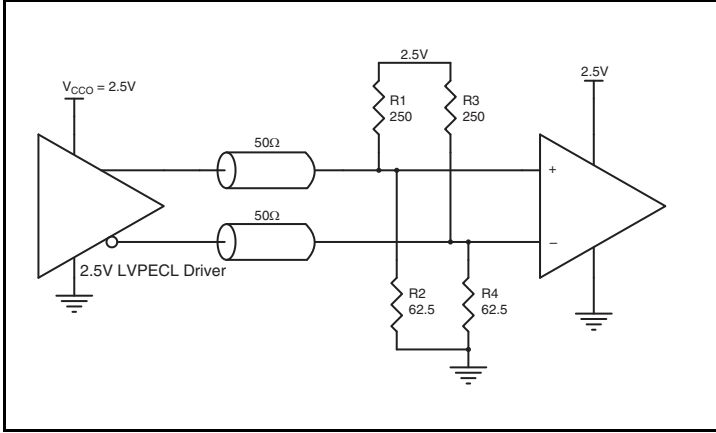


Figure 9A. 2.5V LVPECL Driver Termination Example

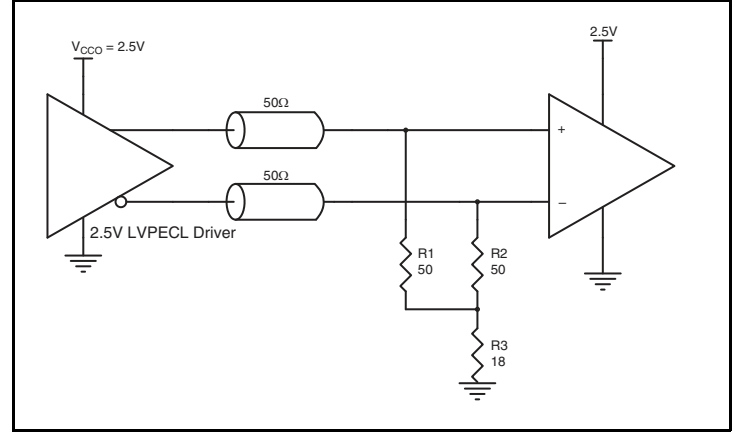


Figure 9B. 2.5V LVPECL Driver Termination Example

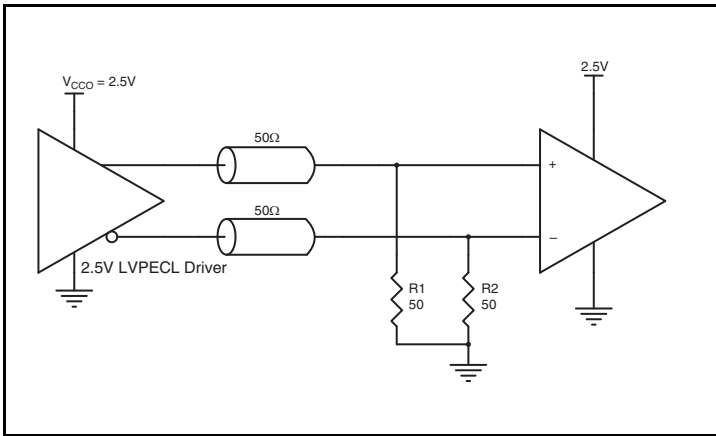


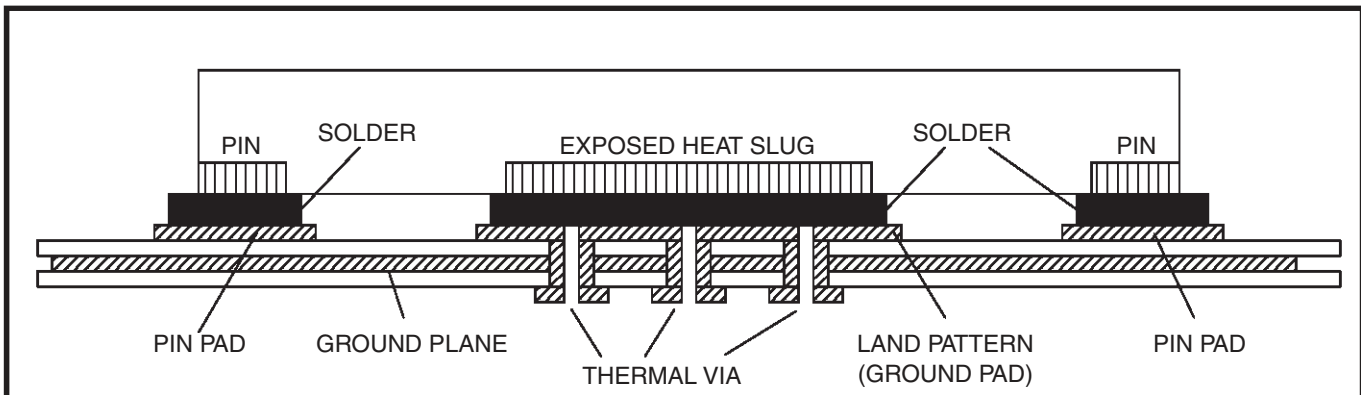
Figure 9C. 2.5V LVPECL Driver Termination Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 10*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.



**Figure 10. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Schematic Example

Figure 11 shows an example of IDT8T49N105 application schematic. In this example, the device is operated at  $V_{DD} = V_{DDA} = 3.3V$  and  $V_{DDO\_x} = 2.5V$ . The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance,  $C1 = 5pF$  and  $C2 = 5pF$ , are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the Xtal\_In and Xtal\_Out pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2.

The ePAD provides a low thermal impedance connection between the internal device and the PCB. It also provides an electrical connection to the die and must be connected to ground.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance,

power supply isolation is required. The IDT8T49N105 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

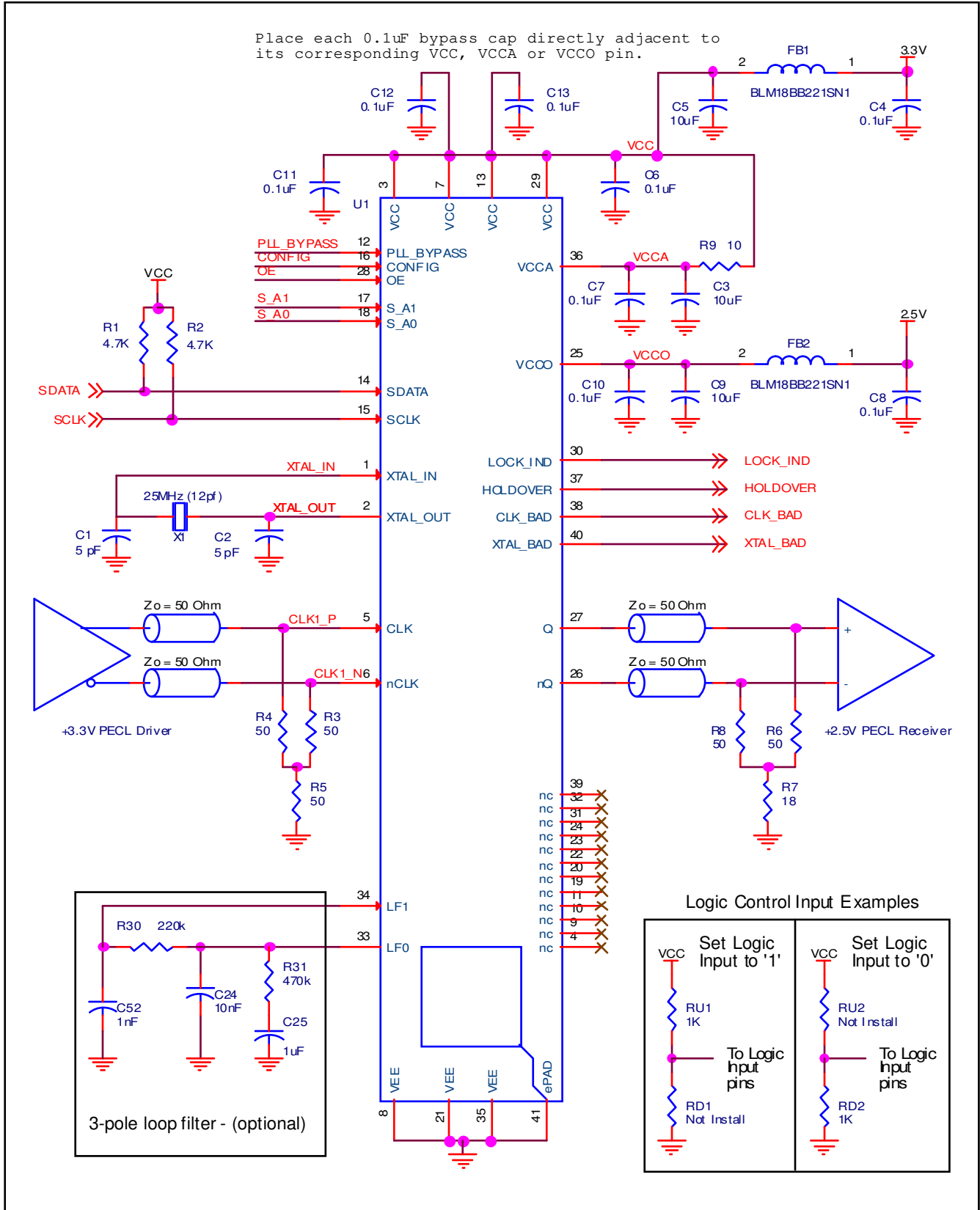


Figure 11. IDT8T49N105I Schematic Example

## LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N105I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T49N105I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 332mA = \mathbf{1150.4W}$
- Power (outputs)<sub>MAX</sub> = **33.2mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) = 1150.4mW + 33.2mW = **1183.6mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 9 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.184\text{W} * 32.4^\circ\text{C/W} = 123.4^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

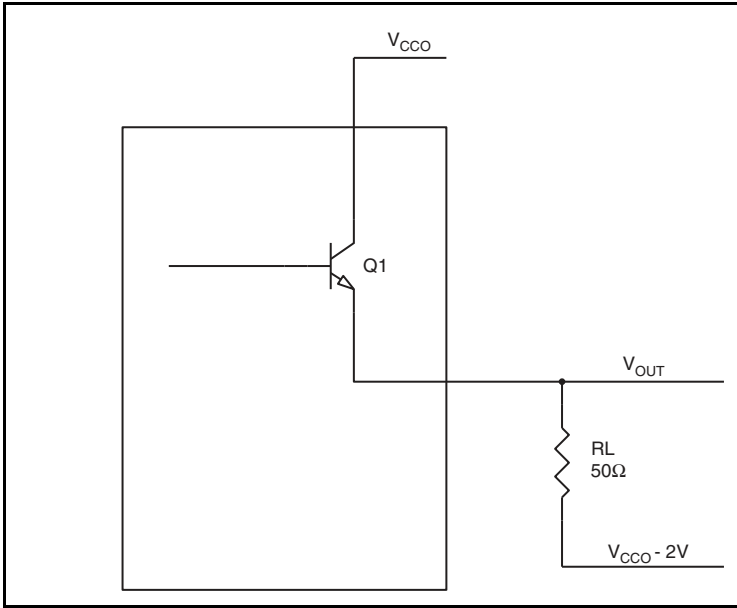
**Table 9. Thermal Resistance  $\theta_{JA}$  for 40 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 12*.



**Figure 12. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.7V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.7V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.5V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.5V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.7V)/50\Omega] * 0.7V = \mathbf{18.2mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V = \mathbf{15mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{33.2mW}$

## LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N203I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T49N203I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * (I_{CC\_MAX} + I_{CCA\_MAX}) = 3.465V * (284mA + 30mA) = \mathbf{1088.01mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{CCO\_MAX} * I_{CCO\_MAX} = 3.465V * 22mA = \mathbf{76.23mW}$

**Total Power**<sub>MAX</sub> = 1088.01mW + 76.23mW = **1164.33mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 10 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.164\text{W} * 32.4^\circ\text{C/W} = 122.7^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 10. Thermal Resistance  $\theta_{JA}$  for 40 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

## Reliability Information

**Table 11.  $\theta_{JA}$  vs. Air Flow Table for a 40 Lead VFQFN**

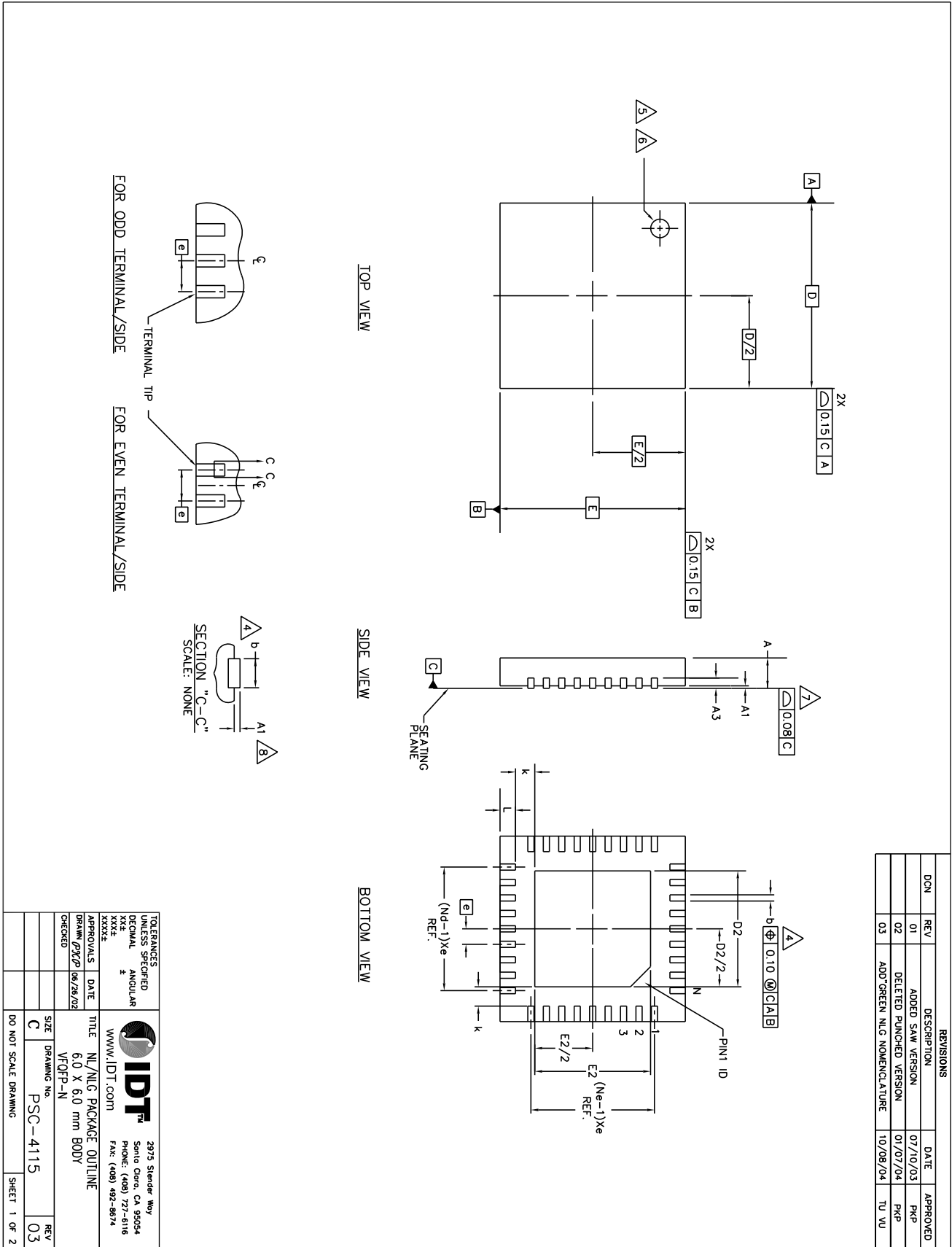
$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

## Transistor Count

The transistor count for IDT8T49N105I is: TBD



# 40 Lead VFQFN Package Outline and Package Dimensions



# 40 Lead VFQFN Package Outline and Package Dimensions, continued

5 A B C D E F G H I J K L	JEDEC VARIATION VJUC-3			N <sub>01</sub> E	5 A B C D E F G H I J K L	JEDEC VARIATION VJUD-5			N <sub>01</sub> E
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
ⓐ	0.65	BSC			ⓐ	0.50	BSC		
N	28			2	N	40		3	
Nd				2	Nd	10		3	
Ne	7			2	Ne	10		3	
b	0.25		0.35	4	b	0.18	0.25	0.30	4
D2				10	D2				10
E2				10	E2				10


5 A B C D E F G H I J K L	COMMON DIMENSIONS			N <sub>01</sub> E
	MIN.	NOM.	MAX.	
A	0.00	0.90	1.00	7
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
K	0.20			
L	0.35	0.40	0.45	

**NOTES:**

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M - 1994.
2. N IS THE NUMBER OF TERMINALS.  
ND IS THE NUMBER OF TERMINALS IN X-DIRECTION &  
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-220, VARIATION VJUC-3 & VJUD-5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.

**40 Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm**

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD "GREEN" NLG NOMENCLATURE	10/08/04	TU VU

TOLERANCES UNLESS SPECIFIED			2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-9674
DECIMAL	ANGULAR		
XXX	±	WWW.IDT.COM	
XXXX		TITLE	NL/NLG PACKAGE OUTLINE
XXXX		DRAWN	gxp/06/28/02
		DATE	06/28/02
		APPROVALS	VFQFN-N
		CHECKED	
		SIZE	C
		DRAWING No.	PSC-4115
		DO NOT SCALE DRAWING	
		REV	03
		SHEET	2 OF 2

## Ordering Information

**Table 12. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N105A-dddNLGI	IDT8T49N105A-dddNLGI	"Lead-Free" 40 Lead VFQFN	Tray	-40°C to +85°C
8T49N105A-dddNLGI8	IDT8T49N105A-dddNLGI	"Lead-Free" 40 Lead VFQFN	Tape & Reel	-40°C to +85°C

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

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