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December 2014

FAN8831
Sinusoidal Piezoelectric Actuator Driver with Step-Up DC-DC Converter

Features

Step-Up DC-DC Converter

- Integrated Step-up Power Switch up to 36 V
- Wide Operating Voltage Range of 2.7 to 5.5 V
- Adjustable Step-up Output Voltage
- Adjustable Step-up Current Limit
- Zero Current Detector (ZCD)
- Internal Soft-Start
- Built-in Protection Circuit
  - Over Voltage Protection (OVP)
  - Thermal Shutdown (TSD)

Piezo Actuator Driver

- Integrated Full-Bridge Switches (V_{DS}=75 V)
- Digitally Implemented Sine Modulator

Package Information

- Small 4.0 mm × 4.0 mm MLP

Description

The FAN8831 is a single-chip piezoelectric actuator driver consisting of step-up DC-DC converter with integrated 36 V boost switch and a full-bridge output stage. The device is capable of driving a Piezo bi-directionally at 120 V peak-to-peak from a single 3 V lithium cell. The step-up DC-DC converter operates in Critical Conduction Mode (CRM) and is optimized to work in a coupled inductor configuration to provide output voltages in excess of 60 V. Over-voltage protection, over-current protection and thermal shutdown are all provided. An internal ready is used to enable the full-bridge gate driver when step-up DC-DC converter output voltage reaches the proper level with hysteresis.

The boost voltage is set using external resistors, and step-up current limit is programmable via the external resistor at OCP pin.

The output H-bridge features four integrated 75 V P and N-channel for sine wave drive of the Piezo actuator.

Applications

- Piezo Actuator

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN8831MPX	-40°C to +125°C	24-Lead, MLP	Tape & Reel

Application Diagram

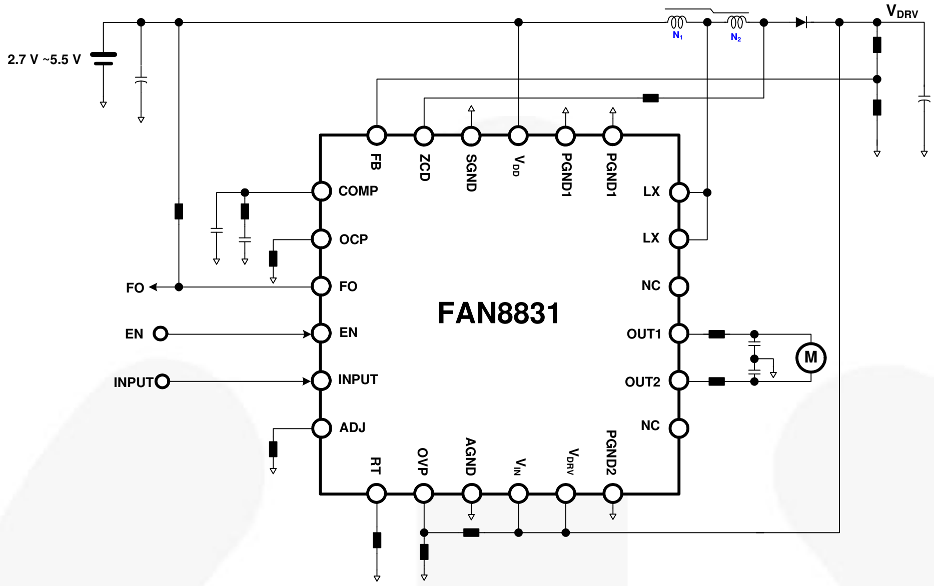


Figure 1. Typical Application Circuit for Piezo Actuator Driver

Internal Block Diagram

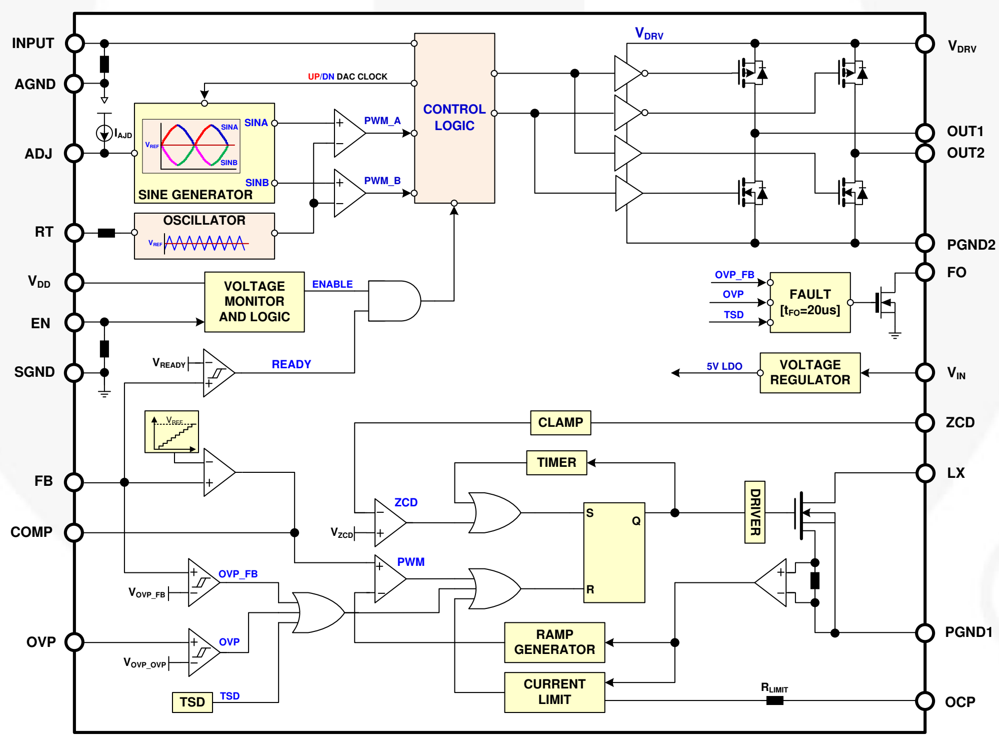


Figure 2. Functional Block Diagram

Pin Configuration

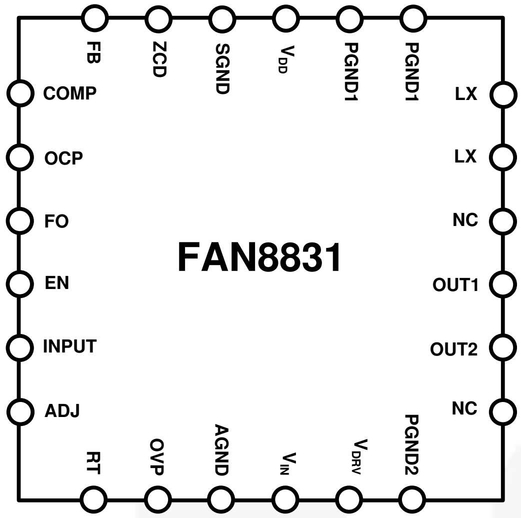


Figure 3. Pin Assignments

Pin Definitions

Pin #	Name	Description
1,2	PGND1	Power Ground 1. It is connected to the source of the step-up switch.
3	V_{DD}	Power supply of step-up DC-DC converter.
4	SGND	Signal Ground. The signal ground for step-up DC-DC converter circuitry.
5	ZCD	The input of the zero current detection.
6	FB	Step-up DC-DC converter output voltage feedback input.
7	COMP	Output of the transconductance error amplifier.
8	OCP	Sets Step-up DC-DC converter current limit.
9	FO	Fault Output.
10	EN	Enable pin to turn on and off the overall system. (Active Low Shutdown Mode).
11	INPUT	Logic input for sinusoidal waveform.
12	ADJ	Output voltage adjust control pin. Connect to internal current source to change output voltage using an external resistor. Connect a small capacitor (1 nF).
13	RT	Oscillator frequency control pin.
14	OVP	Voltage sense input of Step-up DC-DC converter for Over-Voltage Protection.
15	AGND	Analog Ground. The signal ground for full-bridge driver circuitry.
16	V_{IN}	Power supply of 5 V LDO.
17	V_{DRV}	Power supply of full-bridge driver.
18	PGND2	Power Ground 2. The power ground for full-bridge driver .
19	NC	Not Connected
20	OUT2	Output 2 for full-bridge driver.
21	OUT1	Output 1 for full-bridge driver.
22	NC	Not Connected
23, 24	L_X	Switch Node. This pin is connected to the inductor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DRV}	DC Link Input Voltage Drain-Source Voltage of each MOSFET			75	V
V_{DD}	DC Supply Voltage for DC-DC Converter		-0.3	5.5	V
$V_{IN,DCDC}$	EN, INPUT, FB and COMP to SGND		-0.3	V_{DD} +0.3	V
V_{IN}	DC Supply Voltage for LDO		-0.3	75	V
V_{LX}	LX to PGND		-0.3	36	V
P_D	Power Dissipation(2)	1S0P with thermal vias(3)		0.98	W
		1S2P with thermal vias(4)		2.9	
θ_{JA}	Thermal Resistance Junction-Air(2)	1S0P with thermal vias(3)		127	°C/W
		1S2P with thermal vias(4)		43	
T_A	Operating Ambient Temperature Range		-40	125	°C
T_J	Operating Junction Temperature		-55	150	°C
T_{STG}	Storage Temperature Range		-55	150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2	KV
		Charged Device Model, JESD22-C101		500	V

Notes:
1. All voltage values, except differential voltages, are given with respect to SGND, AGND and PGND pin.
2. JEDEC standard: JESD51-2, JESD51-3. Mounted on 76.2×114.3×1.6mm PCB (FR-4 glass epoxy material).
3. 1S0P with thermal vias: one signal layer with zero power plane and thermal vias.
4. 1S2P with thermal vias: one signal layer with two power plane and thermal vias.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DRV}	Supply Voltage for Full-Bridge Driver	30		60	V
V_{LX}	Boost Switch Voltage	10		30	V
V_{DD}	Operating Voltage for DC-DC Converter	2.7	3.0	3.3	V
V_{IN}	Operating Voltage for Voltage Regulator	10		60	V
R_{OCP}	Current Limit Control Resistor	7.0		150	kΩ

Electrical Characteristics

V_{DD}=3.0 V, V_{IN}=15.0 V, V_{DRV}=60 V, R_T=70 KΩ and T_A=-40°C to +125°C. Typical values T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply Section						
$I_{Q,DD}$	Quiescent Current for V_{DD}[5]	V_{EN}=V_{COMP}=V_{DD}, V_{FB}=1.0 V Device not switching		700	1200	µA
$I_{Q,IN}$	Quiescent Current for V_{IN}			300	500	µA
$I_{Q,DRV}$	Quiescent Current for V_{DRV}			200	300	µA
$I_{SD,DD}$	Shutdown Current for V_{DD}	V_{EN}=0 V, V_{DD}=V_{IN}=V_{DRV} =3 V			1	µA
$I_{SD,IN}$	Shutdown Current for V_{IN}				1	µA
$I_{SD,DRV}$	Shutdown Current for V_{DRV}			5	10	µA
$V_{DDSTART}$	Start Threshold Voltage		2.6	2.7	2.8	V
$V_{DDUVHYS}$	V_{DD} UVLO Hysteresis Voltage		0.1	0.2	0.3	V
Error Amplifier Section						
V_{FB}	Feedback Reference Voltage	T_A=25°C	0.99	1.0	1.01	V
I_{FB}	FB pin Bias Current	V_{FB}=0 V ~ 2 V			1	µA
ΔV_{FB1}	Feedback Voltage Line Regulation[6]	2.7 V < V_{DD} < 5 V		0.5	1.5	%/V
G_m	Transconductance	T_A=25°C		800		µmho
Zero Current Detect Section						
V_{ZCD}	Input Voltage Threshold[7]		1.65	1.83	2.00	V
V_{CLAMPH}	Input High Clamp Voltage	I_{DET}=2.3 mA	3.0	3.5	4.0	V
V_{CLAMPL}	Input Low Clamp Voltage	I_{DET}= -2.3 mA	-0.30	0.12	0.50	V
$I_{ZCD,SR}$	Source Current Capability				-2.3	mA
$I_{ZCD,SK}$	Sink Current Capability				2.3	mA
$t_{ZCD,D}$	Delay From ZCD to Output Turn-On[7]			50	200	ns
Maximum On-Time Section						
$t_{ON,MAX}$	Maximum On-Time		15	25	35	µs
Restart / Maximum Switching Frequency Limit Section						
t_{RST}	Restart Timer		15	25	35	µs
f_{MAX}	Maximum Switching Frequency[7]			900	1000	KHz
Soft-Start Timer Section						
t_{SS}	Internal Soft-Start		16	28	40	ms
Current Limit Comparator Section						
I_{OCP}	OCP Trip Current	R_{OCP}=3.3 KΩ, V_{DD}=3.3 V	1.85	2.00	2.15	A
		R_{OCP}=22 KΩ,V_{DD}=3.3 V	0.9	1.0	1.1	A
t_{CS_BLANK}	Comparator Leading-Edge Blanking Time[7]		80	130	180	ns

Notes:

5. This is the VDD current consumed when active but not switching. Does not include gate-drive current
6. The line regulation is calculated based on $\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{1}{V_{OUT}}$
7. This parameter, although guaranteed by design, is not tested in production.

Electrical Characteristics

V_{DD}=3.0 V, V_{IN}=15.0 V, V_{DRV}=60 V, R_T=70 KΩ and T_A=-40°C to +125°C. Typical values T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Step-Up Switch Section						
R_{DSON}	N-Channel On Resistance	V_{DD}=3.3 V, T_A=25°C		0.2	0.5	Ω
I_{LK_LX}	LX Leakage Current	V_{LX}=36 V			1.0	µA
Oscillator Section						
f_{OSC}	Operating Frequency	R_T=58 KΩ	40	50	60	KHz
		R_T=121 KΩ	20	25	30	KHz
Logic (EN and INPUT) Section						
V_{INPUT+}	INPUT Logic High Threshold Voltage		1.34			V
V_{INPUT-}	INPUT Logic Low Threshold Voltage				0.5	V
I_{INPUT-}	Input Low Current for INPUT and EN	V_{EN}=0 V			1	µA
I_{INPUT+}	Input High Current for INPUT and EN	V_{EN}=V_{DD}	8	12	16	µA
R_{INPUT}	Input Logic Pull-Down Resistance	V_{EN}= V_{INPUT}=3 V		250	375	K Ω
f_{INPUT}	Input Logic Operating Frequency(8)		20		1000	Hz
Full-Bridge Switch Section						
$R_{DS,ONP}$	Output Upper-Side On Resistance	T_A=25°C		3.0	5.0	Ω
$R_{DS,ONN}$	Output Low-Side On Resistance	T_A=25°C		3.0	5.0	Ω
Output Control Section						
$V_{ADJ,MAX}$	Analog Output Control Maximum Voltage(8)	V_{DRV}=100% of Target		1.0		V
$V_{ADJ,MIN}$	Analog Output Control Minimum Voltage(8)			0.1		V
I_{ADJ+}	Internal Current Source for ADJ Pin	T_A=25°C	9	10	11	µA
Protection (Ready, OVP and TSD)						
V_{READY}	Output Ready Threshold Voltage		0.75	0.80	0.85	V
HY_{READY}	Output Ready Hysteresis			0.2		V
V_{OVP_FB}	OVP Threshold Voltage at FB Pin		1.05	1.10	1.15	V
HY_{OVP_FB}	OVP Hysteresis Voltage at FB Pin			0.1		V
V_{OVP_OVP}	OVP Threshold Voltage at OVP Pin		1.10	1.15	1.20	V
HY_{OVP_OVP}	OVP Hysteresis Voltage at OVP Pin			0.15		V
T_{SD}	Thermal Shutdown Temperature(8)			150		°C
T_{HYS}	Hysteresis Temperature of TSD(8)			50		°C
T_{FO}	Fault Output Duration			20	30	µs
V_{FOL}	Fault Output Low Level Voltage	R_{PU}=50 KΩ, V_{PU}=3 V		0.1	0.4	V

Note:

8. This parameter, although guaranteed by design, is not tested in production.

Typical Performance Characteristics

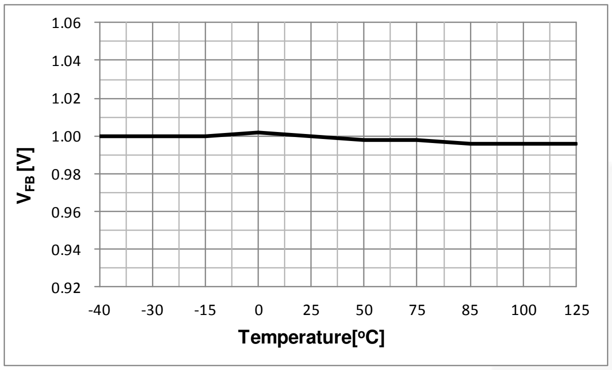


Figure 4. Reference Voltage vs. Temperature

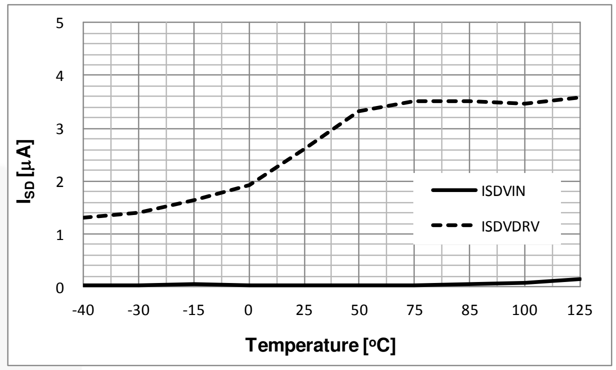


Figure 5. Shutdown Current for V_{DRV} & V_{IN} vs. Temperature

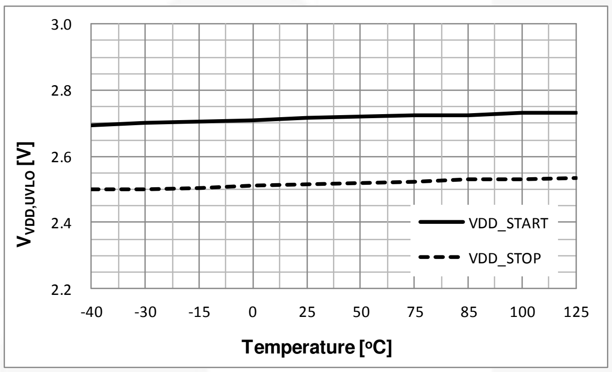


Figure 6. V_{DD} UVLO vs. Temperature

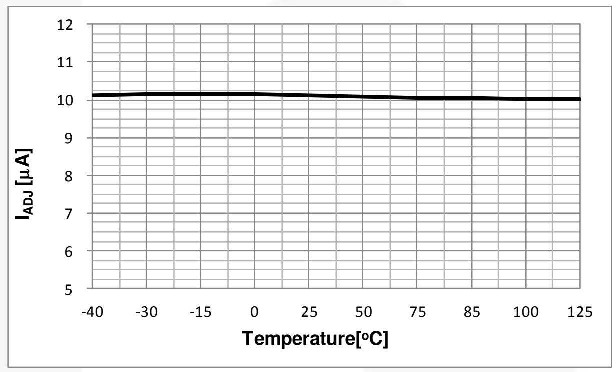


Figure 7. ADJ Current vs. Temperature

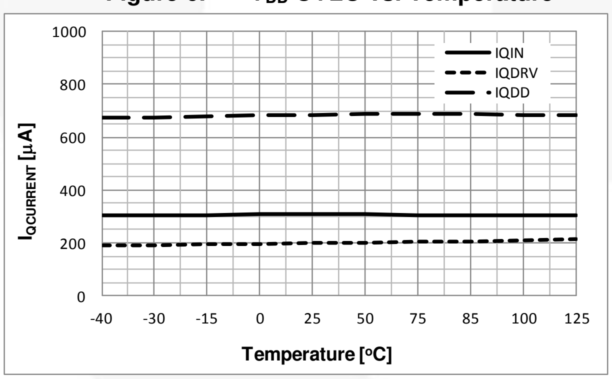


Figure 8. Quiescent Current for V_{DD}, V_{DRV}, & V_{IN} vs. Temperature

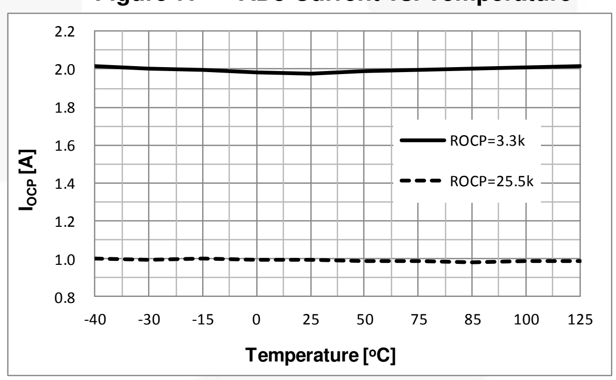


Figure 9. OCP Current vs. Temperature

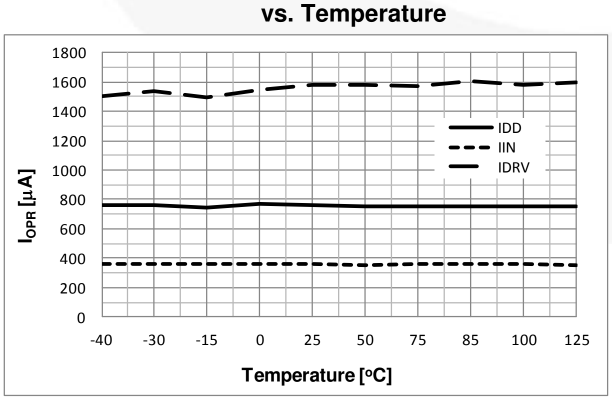


Figure 10. Operating Current for V_{DD}, V_{DRV}, & V_{IN} vs. Temperature

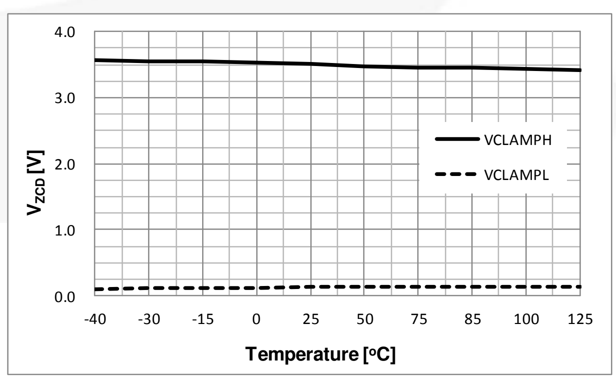


Figure 11. ZDC Clamp Voltage vs. Temperature

Typical Performance Characteristics

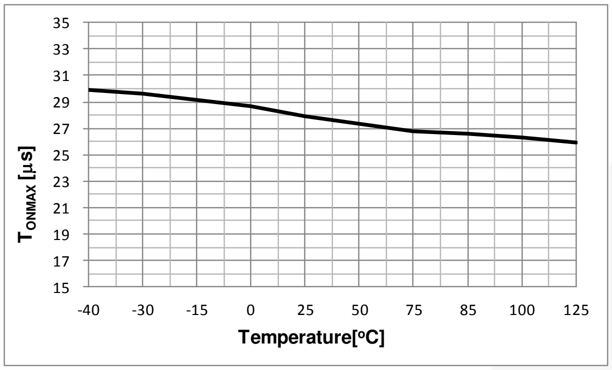


Figure 12. Maximum On-Time vs. Temperature

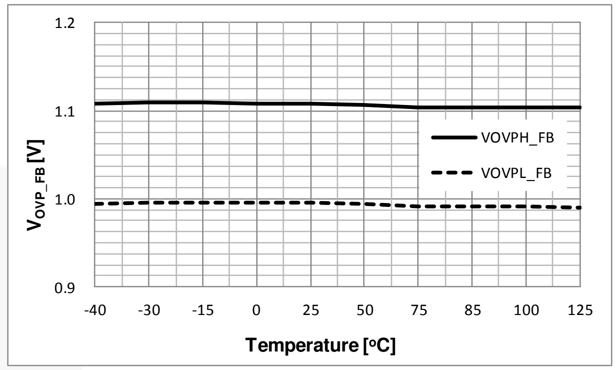


Figure 13. Fist OVP (FB) vs. Temperature

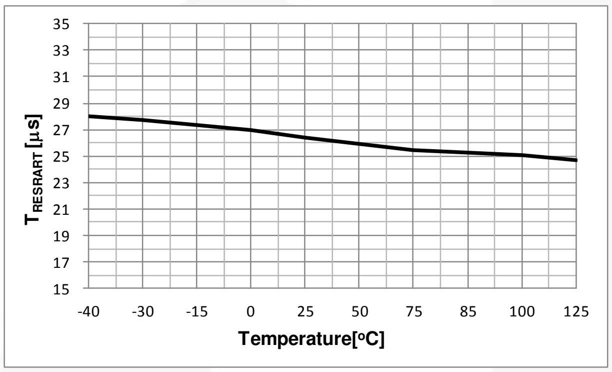


Figure 14. Restart-Time vs. Temperature

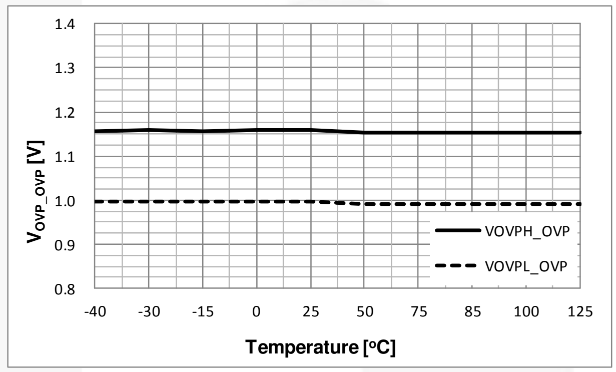


Figure 15. Second (OVP) vs. Temperature

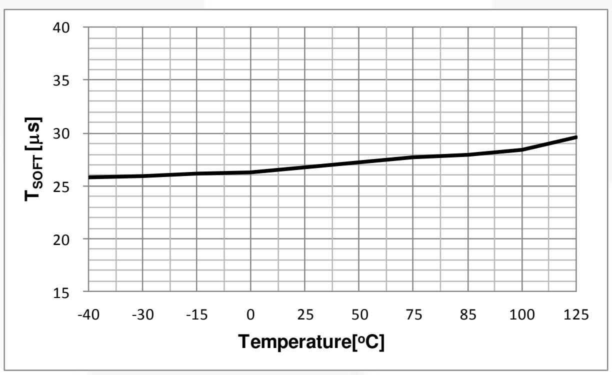


Figure 16. Soft-Start Time vs. Temperature

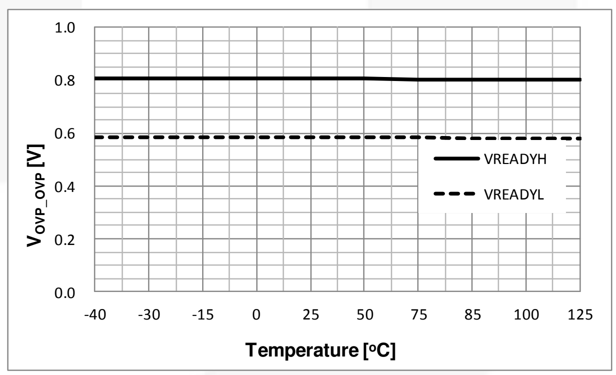


Figure 17. Ready Voltage vs. Temperature

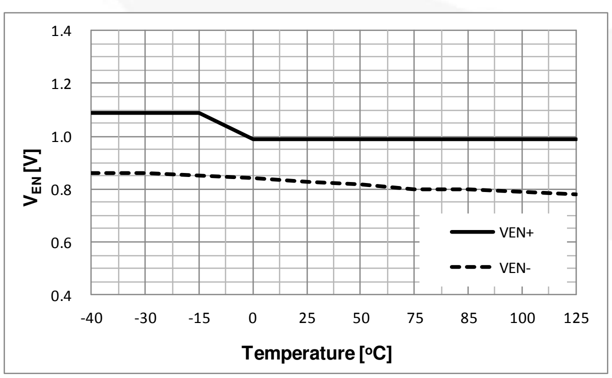


Figure 18. Enable (EN) Threshold Voltage vs. Temperature

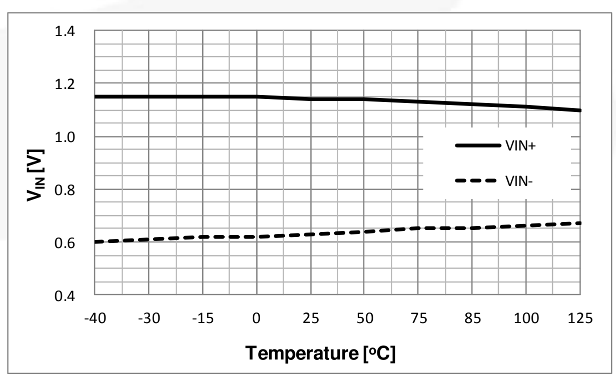


Figure 19. INPUT Threshold Voltage vs. Temperature

Typical Performance Characteristics

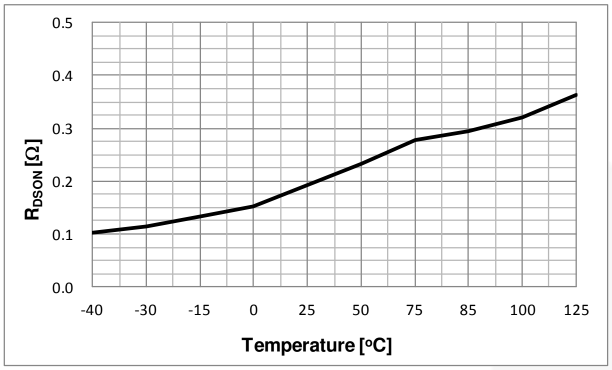


Figure 20. Boost Switch R_{DSON} vs. Temperature

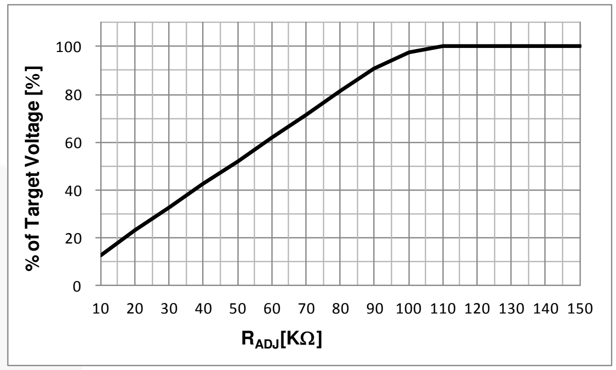


Figure 21. % of Sine Amplitude vs. R_{ADJ}

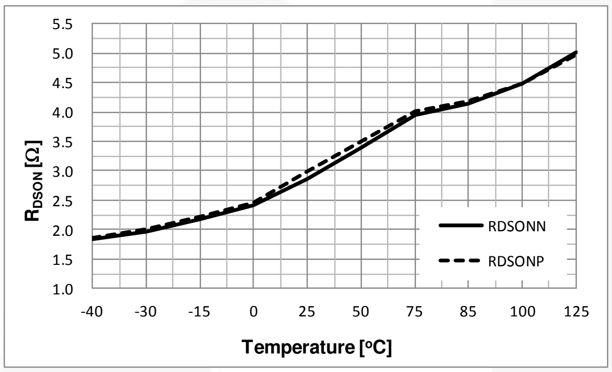


Figure 22. Full-Bridge Switch R_{DSON} vs. Temperature

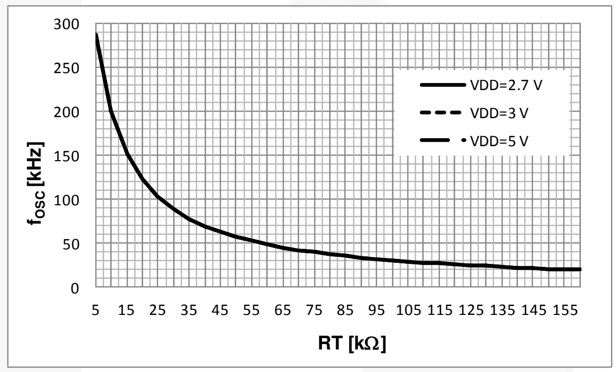


Figure 23. f_{OSC} vs. RT

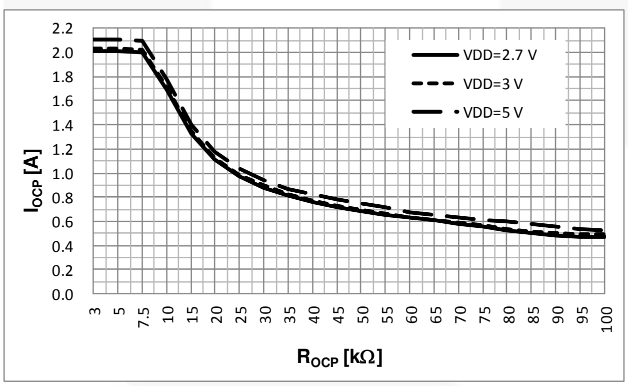
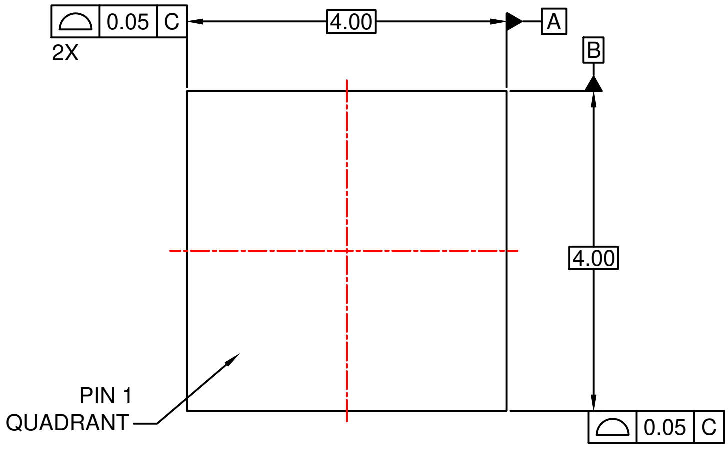
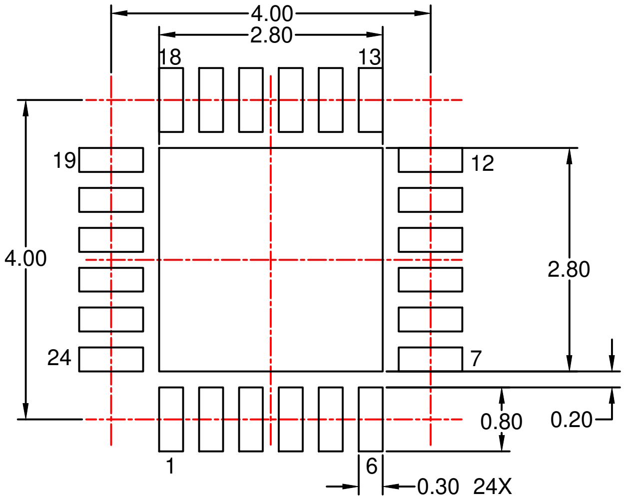


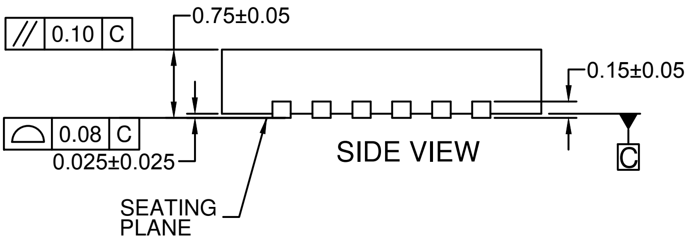
Figure 24. I_{OCP} vs. R_{OCP}

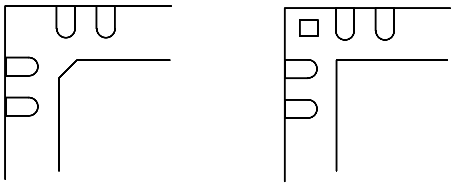


TOP VIEW

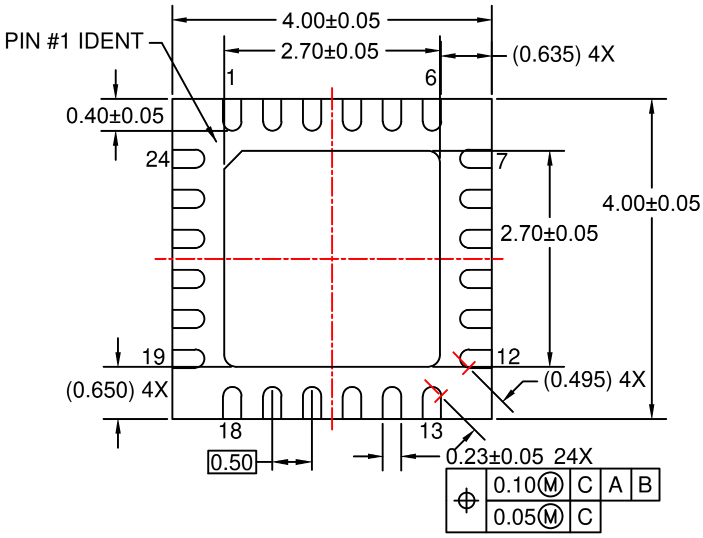


RECOMMENDED LAND PATTERN





BOTTOM VIEW PIN ONE OPTIONS



BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WGGD-6.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN IPC REFERENCE : QFN50P400X400X80-25W6N.

E. DRAWING FILENAME: MKT-MLP24Erev5.

PUBLICATION ORDERING INFORMATION

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