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NTE4063B
Integrated Circuit
CMOS, 4–Bit Magnitude Comparator

Description:

The NTE4063B is a 4–bit magnitude comparator in a 14–Lead DIP type package designed for use in computer and logic applications that require the comparison of two 4–bit words. This logic circuit determines whether one 4–bit word (Binary or BCD) is “less than”, “equal to”, or “greater than” a second 4–bit word.

This device has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single NTE4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, NTE4063B devices may be cascaded by connecting the outputs of the less–significant comparator to the corresponding cascading inputs of the more–significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

Features:

- Expansion to 8, 12, 16 . . . 4N Bits by Cascading Units
- Medium–Speed Operation: Compares Two 4–Bit Words in 250ns (Typ) at 10V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package Temperature Range)
  = 1V at V_{DD} = 5V
  = 2V at V_{DD} = 10V
  = 2.5V at V_{DD} = 15V

Applications:

- Servo Motor Controls
- Process Controllers

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range, All Inputs . . . . . −0.5 to V_{DD}+0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation (T_A = −55° to +100°C), P_D 500mW
T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 1/16” ±1/32” from case, 10sec Max), T_L . . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For T_A = Full package Temperature)	3	–	18	V

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	100	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input High Voltage V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm 10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time Comparing Inputs to Outputs	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	625	1250	ns
		V_{DD} = 10V	–	250	500	ns
		V_{DD} = 15V	–	175	350	ns
Cascading Inputs to Outputs		V_{DD} = 5V	–	500	1000	ns
		V_{DD} = 10V	–	200	400	ns
		V_{DD} = 15V	–	140	280	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Truth Table:

Inputs							Outputs		
Comparing				Cascading					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care
Logic 1 = High Level
Logic 0 = Low Level

Pin Connection Diagram