TAS3308EVM-LC

Low-Cost (LC) Evaluation Module (EVM) for TAS3308 Digital Audio Processor

User's Guide

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Contents

Preface **5**

1 Overview **7**

1.1 TAS3308EVM-LC Features 8

1.2 TAS3308EVM-LC Block Diagram 8

1.3 TAS3308EVM-LC PCB Component Mapping 9

2 Quick Setup **11**

2.1 Unpacking the EVM 12

2.2 Power-Supply Setup 12

2.3 PurePath GDE Software Installation 12

2.4 Developing Process Flow on the EVM 12

2.4.1 Default Configuration 12

2.4.2 Configuring the EVM 13

2.4.3 Master/Slave Mode Operation 14

2.4.4 Loading the Process Flow (.pfw) 14

2.4.5 Running Process Flow 15

3 System Interfaces **17**

3.1 Control Interface 18

3.2 Digital Audio Interface 18

3.2.1 Digital Input 18

3.2.2 Digital Audio Output Interface (J3) 19

3.3 Analog Audio Interface 19

3.3.1 Analog Input 19

3.3.2 PWM Analog Output 20

Important Notices **21**

List of Figures

1-1 TAS3308EVM-LC Block Diagram 8
1-2 TAS3308EVM-LC Component Mapping 9

List of Tables

1 Related TI Documentation 5
3-1 Control Interface (J9) 18
3-2 Digital Audio Input Interface (J1) 18
3-3 Digital Audio Output Interface (J3) 19
3-4 Analog Input Interface (J4) 19
3-5 PWM Analog Output Interface (J6) 20

Read This First

About This Manual

This manual describes the operation of the TAS3308 low-cost (LC) evaluation module (EVM) from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Overview
- Chapter 2 – Quick Setup
- Chapter 3 – System Interfaces

Information About Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

Table 1 contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS3308EVM-LC. The data manuals can be obtained at www.ti.com.

Table 1. Related TI Documentation

DEVICE	LITERATURE NUMBER
TAS3308	SLES215
TUSB3210	SLLS466
TPA66110A2	SLOS314
TPS3808	SBVS050
SN74LVC1G08	SCES217
TPS79533	SLVS350

Additional Documentation

- Graphical Design Environment Tool for TAS3308
- General application reports

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Overview

The TAS3308EVM PurePath Digital™ customer evaluation module demonstrates the TAS3308 digital audio processor from Texas Instruments (TI).

The TAS3308 is a fully programmable high-performance audio processor. It uses an efficient, custom, multi-instruction programming environment optimized for digital audio processing algorithms. The TAS3308 architecture provides high-quality audio processing by using a 48-bit data path, 28-bit filter coefficients, and a single-cycle 28-bit × 48-bit multiplier with a 76-bit accumulator. An embedded 8051 microprocessor provides algorithm and data control for the TAS3308. The TAS3308 is the commercial version intended for home audio and other commercial applications.

The TAS3308 is well suited for inclusion in digital televisions, home theater systems, mini-component audio systems, and professional audio systems.

Topic **Page**

1.1 TAS3308EVM-LC Features 8
1.2 TAS3308EVM-LC Block Diagram..... 8
1.3 TAS3308EVM-LC PCB Component Mapping..... 9

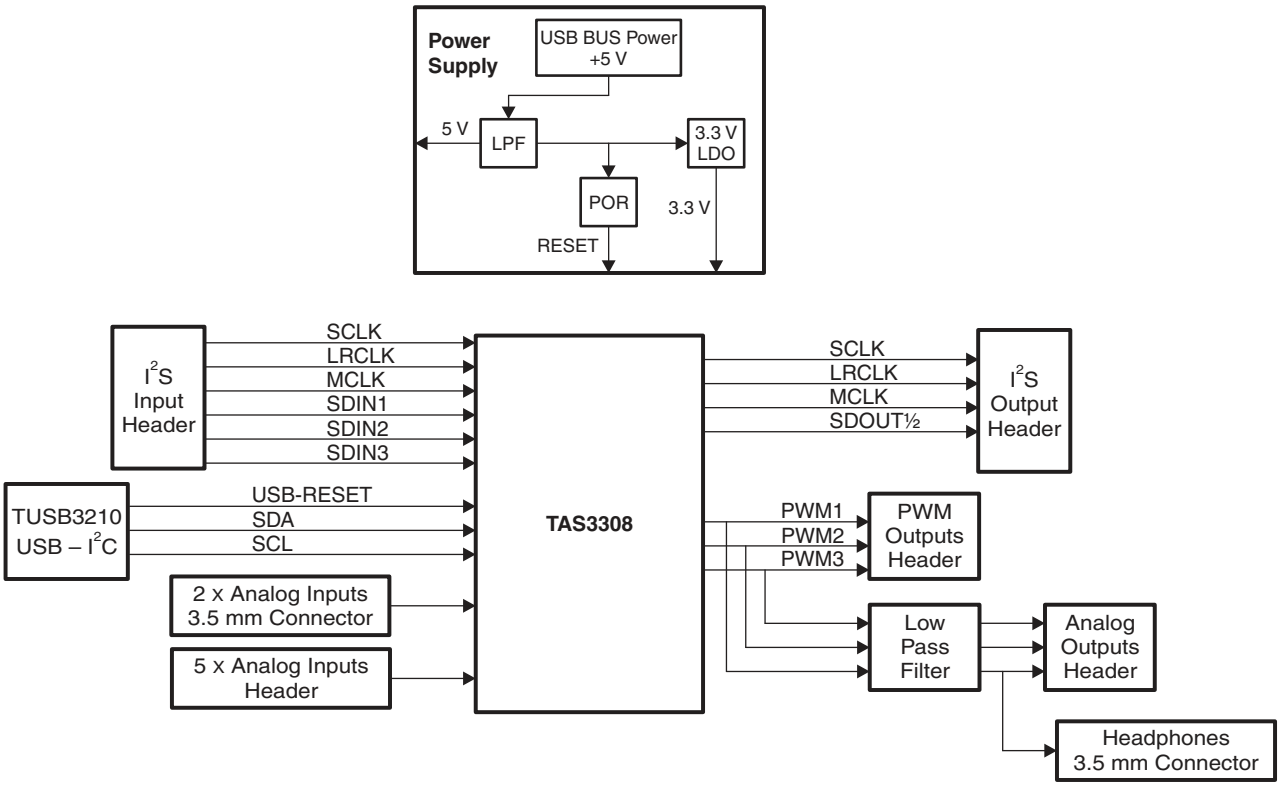
1.1 TAS3308EVM-LC Features

- Six digital input channels, four digital output channels
- Digital input/output format: I^2S, right justified, or left justified
- Three analog stereo inputs multiplexed to one analog-to-digital converter (ADC)
- Three analog stereo pulse width modulated (PWM) digital-to-analog converter (DAC) outputs
- One PWM stereo headphone output
- One stereo line in
- Bus-powered USB interface for I^2C control via graphical development environment (GDE)
- Double-sided plated-through PCB layout
- Demonstrates complete PurePath Digital audio stream from input to output
- Three LED status indicators for reset, I^2C, and USB link

The primary usage mode of the EVM is to provide a software development platform that receives the control and signal processing flow descriptions from a PC running the PurePath Studio™ graphical development environment or integrated development environment (IDE) through the USB interface.

In this mode of operation, the user develops a signal processing flow (applications) and components using PurePath Studio. The resulting programs can be loaded into the EVM EPROM. The TAS3308 then loads the EPROM contents and executes the signal processing flows. During execution, many of the TAS3308 signal processing flow parameters can be dynamically changed using the PurePath Studio GDE. Additional information on using the EVM with the PurePath Studio development environment is included in subsequent sections of this document and in the PurePath Studio online documentation.

1.2 TAS3308EVM-LC Block Diagram



Engineering evaluation only

Figure 1-1. TAS3308EVM-LC Block Diagram

1.3 TAS3308EVM-LC PCB Component Mapping

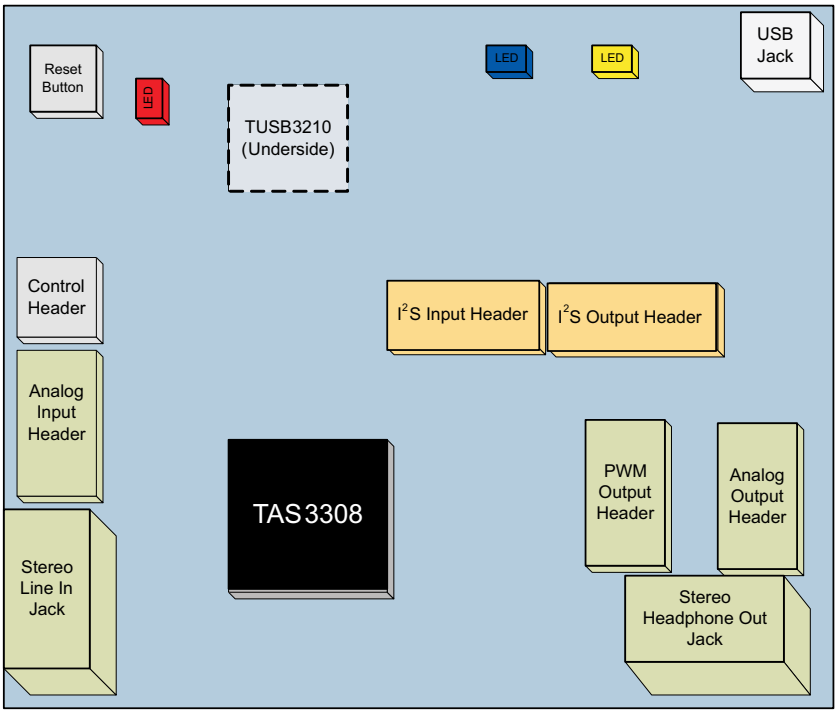


Figure 1-2. TAS3308EVM-LC Component Mapping

Quick Setup

This chapter provides a step-by-step guide to configuring the TAS3308EVM-LC for device evaluation.

This chapter describes the TAS3308EVM-LC board in regards to power-supply requirements and system interfaces. The chapter provides information regarding handling and unpacking, and absolute operating conditions.

Topic **Page**

2.1 **Unpacking the EVM** 12
2.2 **Power-Supply Setup** 12
2.3 **PurePath GDE Software Installation** 12
2.4 **Developing Process Flow on the EVM** 12

Electrostatic Discharge (ESD) Warning

Many of the components on the TAS3308EVM-LC are susceptible to damage by ESD. Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

2.1 Unpacking the EVM

Upon opening the TAS3308EVM-LC package, please check that the following items are included:

- One TAS3308EVM-LC board using one TAS3308PZT
- One CD-ROM containing GDE software, application reports, user's guides, gerber files, and PC software tools
- One USB-type A-to-mini cable

Note: If any of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.2 Power-Supply Setup

The TAS3308EVM-LC is powered via the universal serial bus (USB) connection from the host PC.

2.3 PurePath GDE Software Installation

The TAS3308 is programmed and configured using PurePath Studio. PurePath Studio is composed of a GDE, an integrated development environment (IDE), and component publisher.

- The GDE permits the user to program TAS3308 using predefined signal processing components that are placed and connected graphically in the GDE pallet. PurePath Studio runs on a Windows XP computer.
- The IDE is software development environment that permits the user to construct and test the code for a new GDE component.
- The component publisher is used to create the component and to define the component's control interface and the ways in which the component can be used.

PurePath Studio software is supplied on the TAS3308 software CD-ROM. The latest version of PurePath Studio is always available on the TI extranet for registered users.

2.4 Developing Process Flow on the EVM

2.4.1 Default Configuration

The TAS3308 is placed into the default configuration by receiving a reset. The reset signal comes from one of the following methods:

- Pressing the reset button
- Sending a reset signal through the USB interface via the GDE

Note: Following receipt of the reset, TAS3308 loads the contents of the EEPROM1 and configures the SAP clock in master mode.

2.4.2 Configuring the EVM

After completing the software installation connect the USB cable to J7 on the TAS3308EVM-LC board. This connection powers the EVM and automatically enumerates the TUSB3210 USB serial controller required for communication between the host PC and the TAS3308 digital audio processor.

Start the GDE using the Start Menu. The program will take a few seconds to load on the host PC.

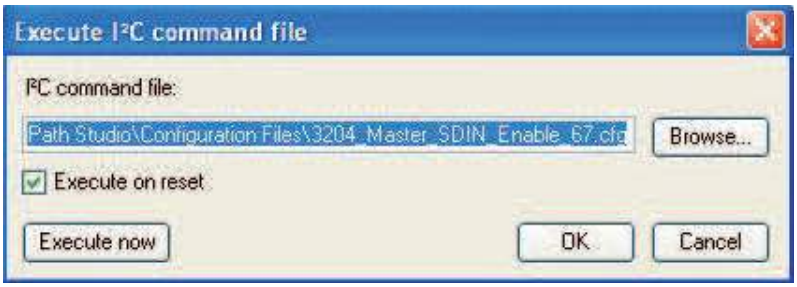
A sample configuration script, which configures the TAS3308 for operation as a I^2S Clock Master, and an I^2S Clock Slave, is provided on the CD-ROM .

The TAS3308EVM-LC PCB is hardwired as an I^2S Clock Master.

Note: Always verify that an initialization file is specified in the Execute I2C command file window before loading a process flow.

The configuration tool is available under the Tools Menu in the GDE.

Tools >> I^2C Command Tool



2.4.3 Master/Slave Mode Operation

The TAS3308PZTcan be configured for both I²S Clock Master and I²S Clock Slave modes via the SAP/Clock register. By default, the TAS3308 is configured for master mode. The TAS3308 can be changed to operate in slave mode by loading the correct SAP/Clock register settings via the configuration file.

Example master and slave configuration scripts can be found on the CD-ROM included with the TAS3308EVM-LC.

Note: Make sure to verify check the 'Execute on reset' box before closing the configuration tool.

2.4.3.1 TAS3308EVM-LC Operation in Master Mode

In master mode, the MCLK, SCLK, and LRCLK for the system are internally generated by the external crystal and are available on header J1. Serial digital audio is input in to the TAS3308EVM-LC via the serial digital input header (J1). Additionally analog data can be input on the analog input header (J4), the line in jack (J2).

2.4.3.2 TAS3308EVM-LC Operation in Slave Mode

In slave mode, the master clock, MCLK, SCLK, and LRCLK for the system must be externally provided by the user's system controller on the serial digital input header (J1). DSP, MCU, and I²C clocks are still internally derived from the external crystal. Serial digital audio is input in to the TAS3308EVM-LC via the serial digital input header (J1). Additionally analog data can be input on the analog input header (J4) and the line in jack (J2).

Note: Audio performance in slave mode depends on the quality of the I²S clocks. It is recommended that the clocks be buffered before TAS3308. The lowest sampling frequency for acceptable audio performance in slave mode is 44.1 kHz.

2.4.4 Loading the Process Flow (.pfw)

The process flow can be built using the TAS3308 application framework, TAS3308 I/O components, and audio processing components.

Note: The TAS3308 Application Framework must be loaded into the pallet before any other components can be added.

The CD-ROM included with the TAS3308EVM-LC comes with a sample process flow that allows the device to stream audio from input to output. This process flow can be loaded from the file menu.

File >> Open

Browse to the A2DD2A.pfw using Windows Explorer and open the process flow. The TAS3308 is designed to stream an audio signal from The Analog-to-Digital Converter (ADC) or the I²S Serial Audio Port (SAP) through the DSP to all the available outputs.

By default the ADC is selected. Refer to the software configuration for details.

2.4.5 Running Process Flow

To run the process flow use build menu and select run.

Build >> Run

The GDE generates and assembles the code for process flow, downloads it to the EVM, then runs the TAS3308LC board. At this point, the GDE switches from Edit Mode to Run Mode, and streams audio from analog inputs or digital inputs to analog outputs or digital output.

For more advanced use of the GDE, refer to GDE online help, release notes, and the TAS3xxx MCU programmer's reference guide.

System Interfaces

This chapter describes the TAS3308EVM-LC board with regard to system interfaces.

Topic **Page**

3.1 Control Interface 18
3.2 Digital Audio Interface 18
3.3 Analog Audio Interface 19

3.1 Control Interface

This interface connects the TAS3308EVM-LC board to an internal controller. This is a general-purpose interface.

Table 3-1. Control Interface (J9)

SIGNAL NAME	SCHEMATIC NET NAME	PIN ASSIGNMENT
Serial data	SDA	1
Serial clock	SCL	2
Ground	GND	3
Reset	RST	4
General purpose input/output 1	GPIO1	5
General purpose input/output 2	GPIO2	6

3.2 Digital Audio Interface

The digital audio interface contains the digital I^2S clocks and data. Please refer to the TAS3308 Data Manual for signal timing an overview of the I^2S protocol.

3.2.1 Digital Input

Table 3-2. Digital Audio Input Interface (J1)

SIGNAL NAME	SCHEMATIC NET NAME	PIN ASSIGNMENT
Master clock input	MCLKIN	1
Ground	GND	2
Serial clock input	SCLKIN	3
Ground	GND	4
Left/right clock input	LRCLKIN	5
Ground	GND	6
Serial data 1 input	SDIN1	7
Ground	GND	8
Serial data 2 input	SDIN2	9
Ground	GND	10
Serial data 3 input	SDIN3	11
Ground	GND	12

3.2.2 Digital Audio Output Interface (J3)

Table 3-3. Digital Audio Output Interface (J3)

SIGNAL NAME	SCHEMATIC NET NAME	PIN ASSIGNMENT
Not connected	N.C.	1
Digital ground	GND	2
Serial data 2 output	SDOUT2	3
Digital ground	GND	4
Serial data 1 output	SDOUT1	5
Digital ground	GND	6
Serial clock output	SCLKOUT	7
Digital ground	GND	8
Left/right clock output	LRCLKOUT	9
Digital ground	GND	10
Master clock output	MCLKOUT	11
Digital ground	GND	12

3.3 Analog Audio Interface

3.3.1 Analog Input

Table 3-4. Analog Input Interface (J4)

SIGNAL NAME	SCHEMATIC NET NAME	PIN ASSIGNMENT
Analog ground	GND	1
Line 1 left input	LINEIN1L	2
Analog ground	GND	3
Line 1 right input	LINEIN1R	4
Analog ground	GND	5
Line 2 left input	LINEIN2L	6
Analog ground	GND	7
Line 2 right input	LINEIN2R	8
Analog ground	GND	9
Line 3 left input	LINEIN3L	10
Analog ground	GND	11
Line 3 right input	LINEIN3R	12

3.3.2 PWM Analog Output

Table 3-5. PWM Analog Output Interface (J6)

SIGNAL NAME	SCHEMATIC NET NAME	PIN ASSIGNMENT
PWM3 right analog output	N/A	1
Analog ground	GND	2
PWM3 left analog output	N/A	3
Analog ground	GND	4
PWM2 right analog output	N/A	5
Analog ground	GND	6
PWM2 left analog output	N/A	7
Analog ground	GND	8
PWM1 right analog output	N/A	9
Analog ground	GND	10
PWM1 left analog output	N/A	11
Analog ground	GND	12

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –0.5 V to 3.8 V and the output voltage range of –0.5 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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