User’s Manual

ISL8117ADEMO3Z

User’s Manual: Demonstration Board

Industrial Analog and Power

Rev.0.00 Aug 2017

ISL8117ADEMO3Z

Demonstration Board

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1. Overview

The ISL8117ADEMO3Z demonstration board (shown in Figure 4) features the ISL8117A. The ISL8117A is a 60V high voltage synchronous buck controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. Its current mode control architecture keeps peripheral component count minimal. Programmable switching frequency ranging from 100kHz to 2MHz helps to optimize inductor size while the strong gate driver delivers up to 30A for the buck output.

1.1 Key Features

- Small, compact design
- Wide input range: 6V to 60V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/CCM operation
- Supports prebias output with SR soft-start
- External frequency sync
- PGOOD indicator
- OCP, OVP, OTP, and UVP protection

1.2 Specifications

The ISL8117ADEMO3Z demonstration board is designed for high current applications. The current rating of the ISL8117ADEMO3Z is limited by the FETs and inductor selected. The electrical ratings of the ISL8117ADEMO3Z are shown in Table 1.

Table 1. Electrical Ratings

Parameter	Rating
Input Voltage	6V to 60V
Switching Frequency	300kHz
Output Voltage	5V
Output Current	6A
OCP Set Point	Minimum 8A at ambient room temperature

1.3 Ordering Information

Part Number	Description
ISL8117ADEMO3Z	High voltage PWM step-down synchronous buck controller

1.4 Related Literature

- For a full list of related documents, visit our website
  - ISL8117A product page

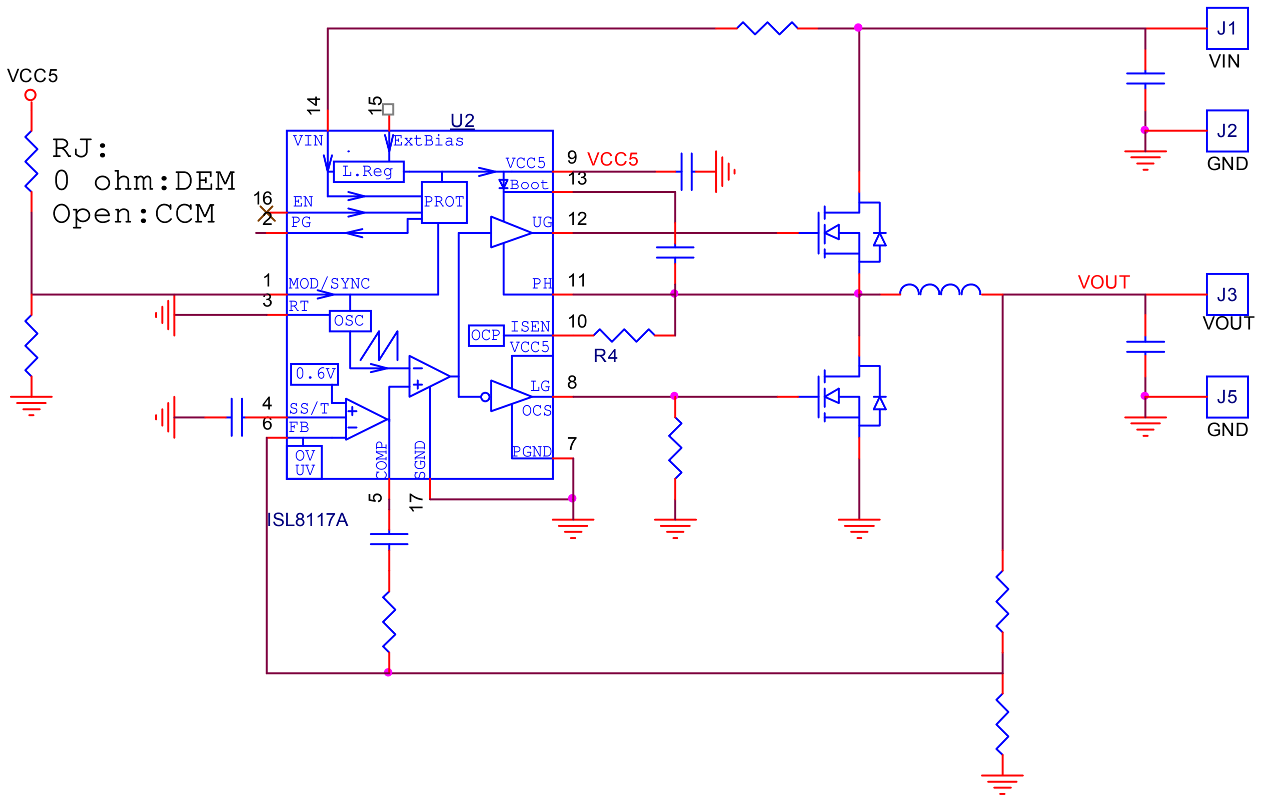


Figure 1. ISL8117ADEMO3Z Block Diagram

2. Functional Description

The ISL8117ADEMO3Z is a compact design with high efficiency and high power density.

As shown in Figure 3 on page 7, 6V to 60V V_{IN} is supplied to J1 (+) and J2 (-). The regulated 5V output on J3 (+) and J5 (-) can supply up to 6A to the load.

2.1 Recommended Testing Equipment

The following materials are recommended to perform testing:

- 0V to 60V power supply with at least 10A source current capability
- Electronic loads capable of sinking current up to 10A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

2.2 Quick Test Guide

(1) Ensure that the circuit is correctly connected to the supply and electronic loads prior to applying any power. Refer to Figure 3 for proper setup.

(2) Turn on the power supply.

(3) Adjust the input voltage, V_{IN}, within the specified range and observe output voltage. The output voltage variation should be within 3%.

(4) Adjust load current within the specified range and observe output voltage. The output voltage variation should be within 3%.

(5) Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, refer to Figure 2 for proper test setup.

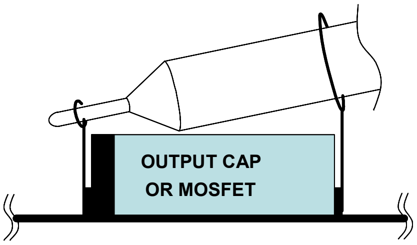


Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

2.3 Operating Range

The input voltage range is from 6V to 60V for an output voltage of 5V. The rated load current is 6A with the OCP point set at minimum 8A at room temperature ambient conditions.

The operating temperature range of ISL8117A is -40°C to +125°C. Please note that airflow is needed.

2.3.1 Evaluating the Other Output Voltages

The ISL8117ADEMO3Z demonstration board output is preset to 5V, however, the output can be adjusted from 1.8V to 5V. The output voltage programming resistor, R_2, will depend on the desired output voltage of the regulator and the value of the feedback resistor R_1, as shown in Equation 1.

$$R_2 = R_1\left(\frac{0.6}{V_{OUT} - 0.6}\right) \quad \text{(EQ. 1)}$$

Table 2 shows the component selection that should be used for the respective V_{OUT} of 1.8V, 3.3V, and 5V.

Table 2. External Component Selection

V_{OUT} (V)	R_2 (kΩ)
1.8	24.9
3.3	11
5	6.8

Notes:

1. If V_{OUT} < 3.3V, the minimal V_{IN} is about 4.5V for full load. If V_{OUT} = 5V, the minimal V_{IN} is about 6V for full load.
2. Unless V_{OUT} = 5V, R11 should be removed.

3. PCB Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL8117A based DC/DC converter. The ISL8117A switches at a very high frequency and therefore the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

There are three sets of critical components in a DC/DC converter using the ISL8117A:

- The controller
- The switching power components
- The small signal components

The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer printed circuit board is recommended.

3.1 Layout Considerations

(1) The input capacitors, upper FET, lower FET, inductor, and output capacitor should be placed first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitors very close to the MOSFETs.

(2) If signal components and the IC are placed in a separate area to the power train, it is recommended to use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for power ground and small signal ground. Connect the SGND and PGND together close to the IC. DO NOT connect them together anywhere else.

(3) The loop formed by the input capacitor, the top FET, and the bottom FET must be kept as small as possible.

(4) Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and the output capacitor are as short as possible with maximum allowable trace widths.

(5) Place the PWM controller IC close to the lower FET. The LGATE connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop currents in this area.

(6) Place a VCC5V bypass capacitor very close to the VCC5V pin of the IC and connect its ground to the PGND plane.

(7) Place the gate drive components (optional BOOT diode and BOOT capacitors) together near the controller IC.

(8) The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect the output capacitors to load to avoid inductance and resistances.

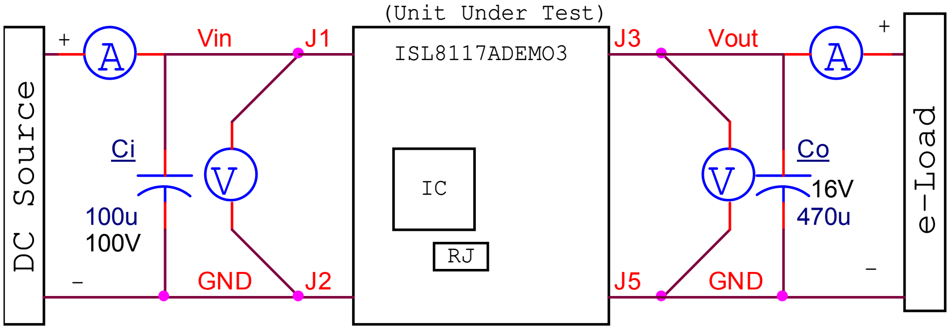
(9) Use copper filled polygons or wide but short trace to connect the junction of the upper FET, lower FET, and output inductor. Also keep the PHASE node connection to the IC short. DO NOT unnecessarily oversize the copper islands for the PHASE node. Since the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise.

(10) Route all high-speed switching nodes away from the control circuitry.

(11) Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths including feedback resistors, current limit setting resistor, soft-starting capacitor, and EN pull-down resistor should be connected to this SGND plane.

(12) Separate the current sensing trace from the PHASE node connection.

(13) Ensure the feedback connection to the output capacitor is short and direct.



RJ:
Close:DEM
Open:CCM [Default]

Figure 3. Proper Test Setup

3.2 ISL8117ADEMO3Z Demonstration Board

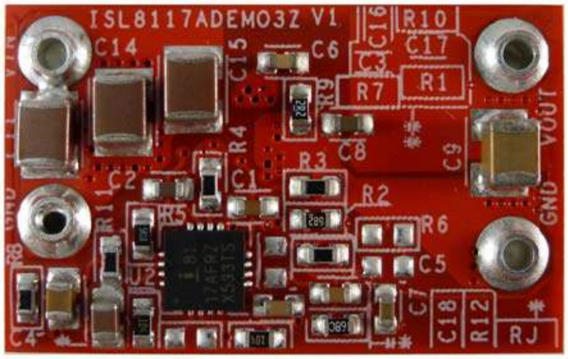


Figure 4. ISL8117ADEMO3Z Top Side

Figure 5. ISL8117ADEMO3Z Bottom Side

3.3 Schematic

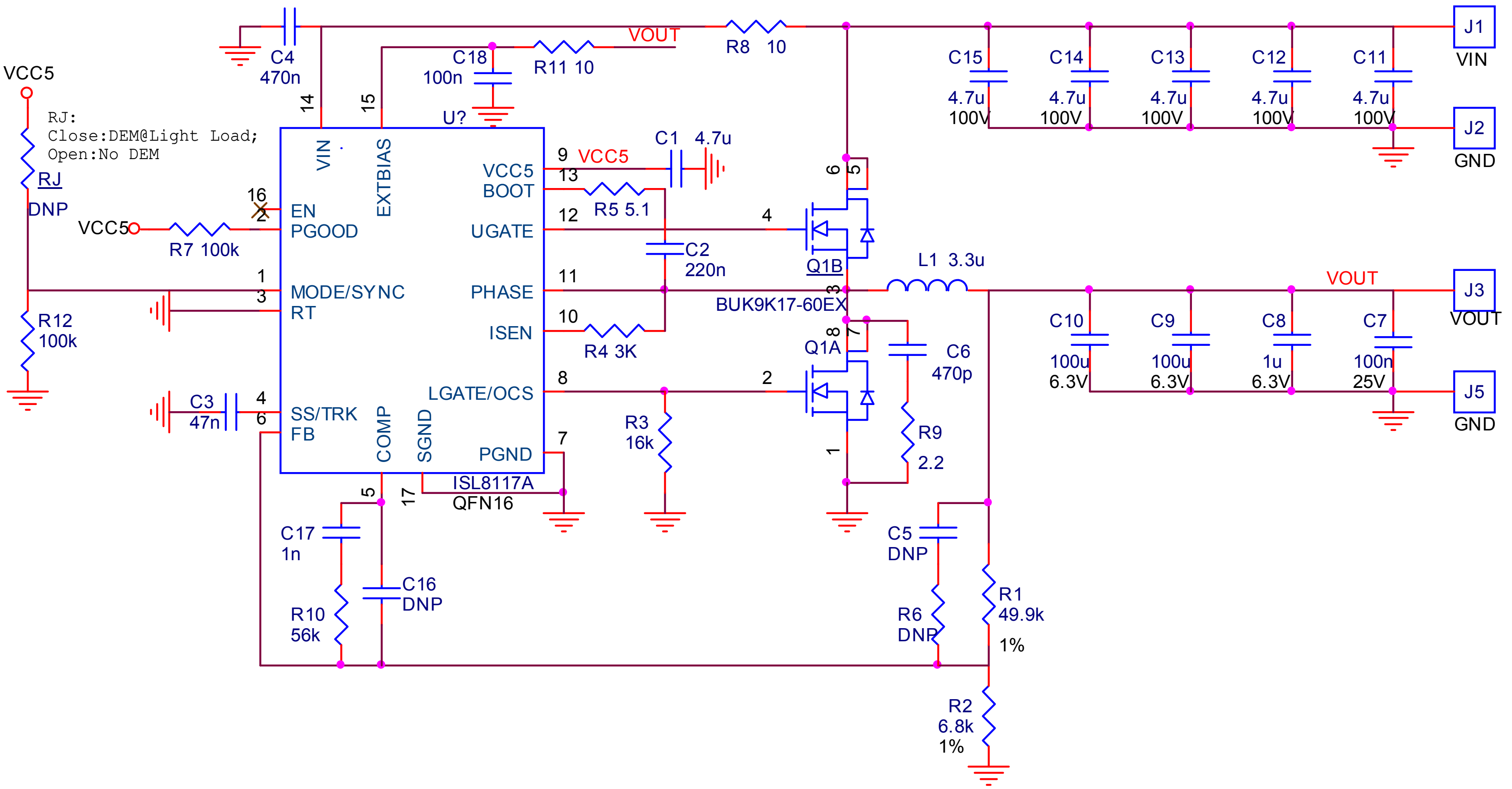


Figure 6. ISL8117ADEMO3Z Schematic

3.4 ISL8117ADEMO3Z Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	C17	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, RoHS	AVX	06035C102KAT2A
1	C7	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E104KA01D
1	C8	CAP, SMD, 0603, 1µF, 6.3V, 10%, X5R, ROHS	Panasonic	ECJ1VB0J105K
1	C2	CAP, SMD, 0603, 0.22µF, 25V, 10%, X7R, ROHS	TDK	C1608X7R1E224K
1	C6	CAP, SMD, 0603, 470pF, 100V, 10%, X7R, ROHS	Vishay	VJ0603Y471KXBA
1	C3	CAP, SMD, 0603, 0.047µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E473KA01D
1	C1	CAP, SMD, 0603, 4.7µF, 10V, 10%, X5R, ROHS	Venkel	CR0603-16W-4701FT
0	C5, C16	CAP, SMD, 0603, DNP-Place Holder, ROHS		
1	C18	CAP, SMD, 0805, 0.1µF, 100V, 10%, X7R, ROHS	TDK	C2012X7R2A104K
1	C4	CAP, SMD, 0805, 0.47µF, 100V, 10%, X7R, ROHS	Murata	GRM21BR72A474KA73L
2	C9, C10	CAP, SMD, 1210, 100µF, 6.3V, 10%, X5R, ROHS	AVX	12106D107KAT2A
5	C11, C12, C13, C14, C15	CAP, SMD, 1210, 4.7µF, 100V, 10%, X7S, ROHS	TDK	CGA6M3X7S2A475K200AB
1	L1	COIL-PWR INDUCTOR, SMD, 8.4x7.9, 3.3µH, 20%, 14A, ROHS	Wurth Electronics	7443340330
1	J1, J2, J3, J5	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
1	U2	IC-55V SWITCHING CONTROLLER, 16P, QFN, ROHS	Intersil	ISL8117AFRZ
1	Q1	TRANSIST-MOS, DUAL N-CHANNEL, SMD, 8P, 56LFPAK, 60V, 26A, ROHS	NXP Semiconductor	BUK9K17-60EX
2	R8, R11	RES, SMD, 0603, 10Ω, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT10R0F
1	R9	RES, SMD, 0603, 2.2Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3RQF2R2V
1	R5	RES, SMD, 0603, 5.1Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-05R1FT
2	R7, R12	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1003FT
1	R3	RES, SMD, 0603, 16k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-16W-1602FT
1	R4	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-073KL
1	R1	RES, SMD, 0603, 49.9k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-4992FT
1	R10	RES, SMD, 0603, 56k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5602V
1	R2	RES, SMD, 0603, 6.8k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-076K8L
0	R6, RJ	RES, SMD, 0603, DNP-Place Holder, ROHS		

3.5 ISL8117ADEMO3Z PCB Layout

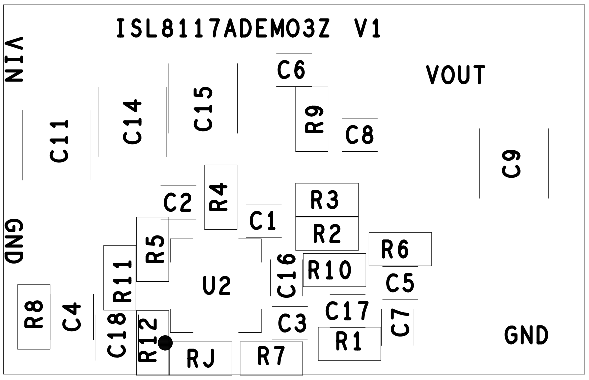


Figure 7. Assembly Top

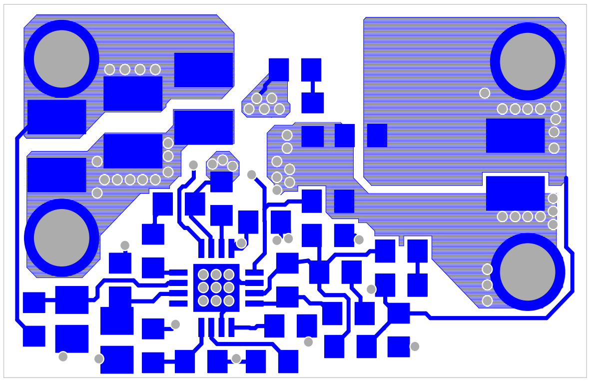


Figure 8. Top Layer

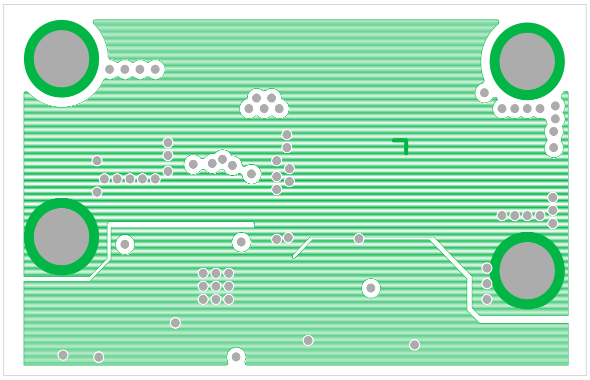


Figure 9. Second Layer (Solid Ground)

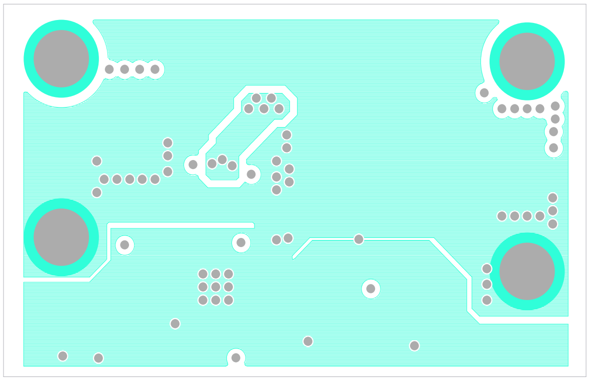


Figure 10. Third Layer

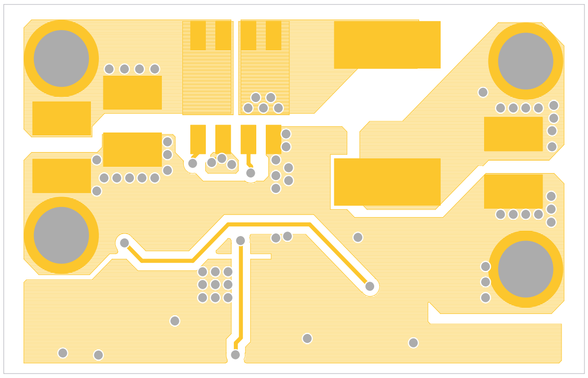


Figure 11. Bottom Layer

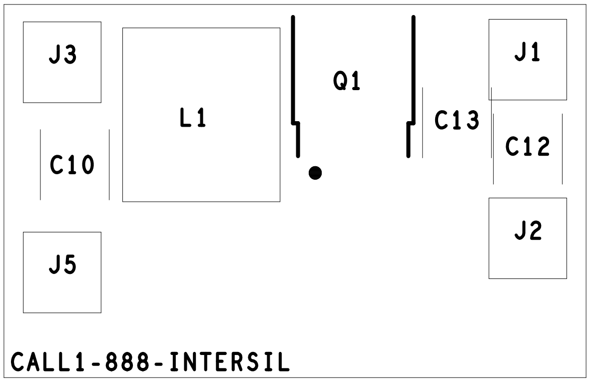


Figure 12. Assembly Bottom

3.6 Typical Demonstration Board Performance Curves

V_{IN} = 24V, V_{OUT} = 5V, unless otherwise noted.

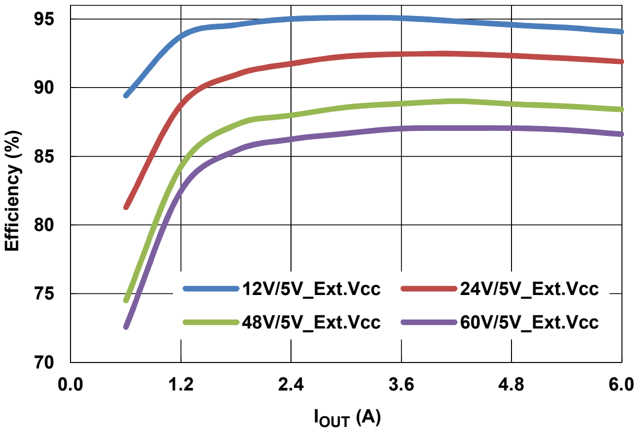


Figure 13. CCM Efficiency

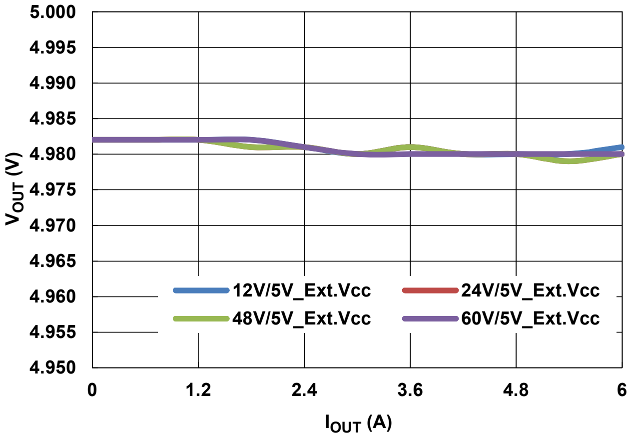


Figure 14. CCM Load Regulation

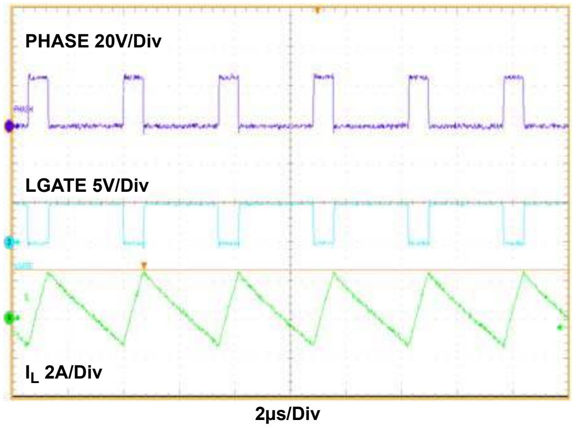


Figure 15. PHASE, LGATE, and Inductor Current Waveforms, I_O = 0A

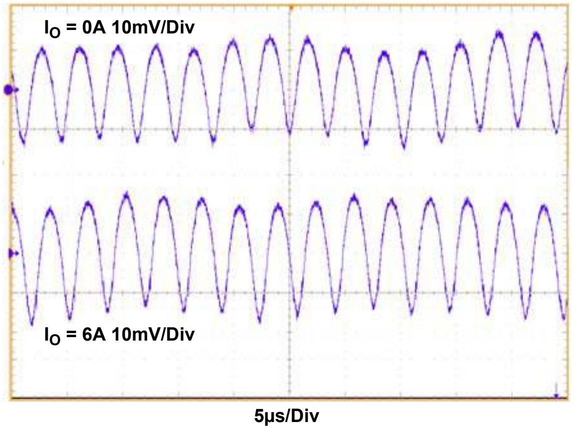


Figure 16. Output Ripple, Mode = CCM

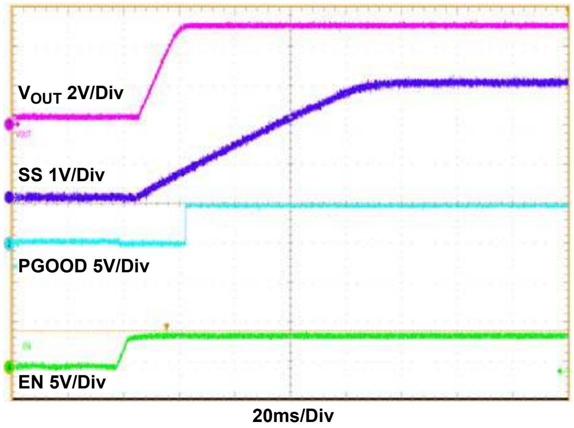


Figure 17. CCM Start-Up Waveforms: V_{OUT}, SS, PGOOD, EN, I_O = 0A

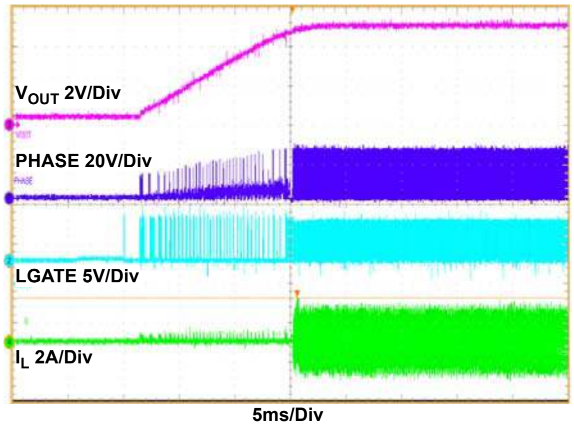


Figure 18. CCM Start-Up Waveforms: V_{OUT}, PHASE, LGATE, I_L, I_O = 0A

V_{IN} = 24V, V_{OUT} = 5V, unless otherwise noted. **(Continued)**

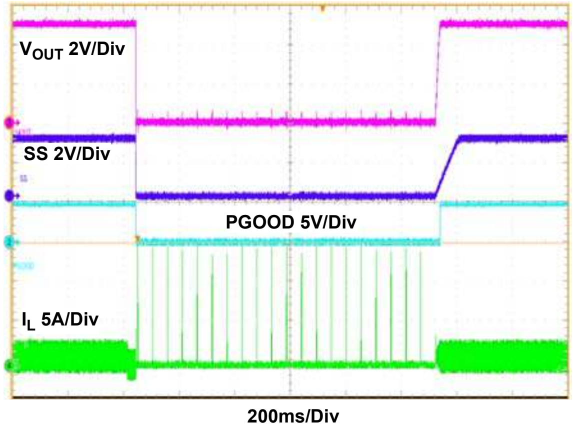


Figure 19. Short-Circuit Waveforms

4. Revision History

Rev.	Date	Description
0.00	Aug 3, 2017	Initial release

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