STK12C68

64 Kbit (8 K x 8) AutoStore nvSRAM

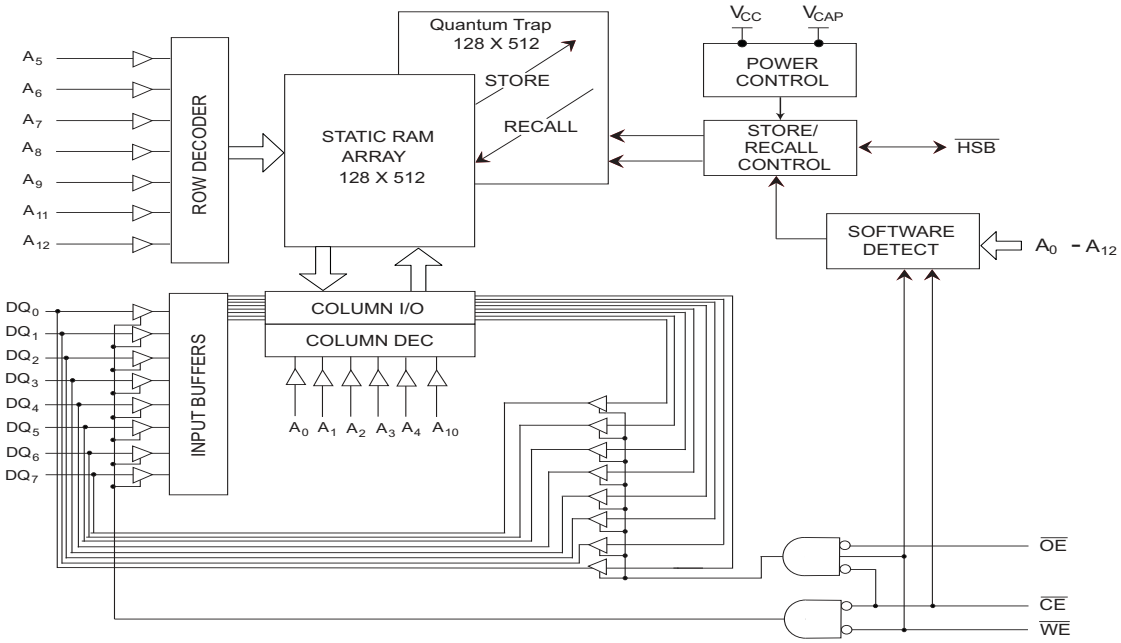
Features

- 25 ns, 35 ns, and 45 ns access times
- Hands off automatic STORE on power-down with external 68 µF capacitor
- STORE to QuantumTrap nonvolatile elements is initiated by software, hardware, or AutoStore on power-down
- RECALL to SRAM initiated by software or power-up
- Unlimited read, write, and recall cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5 V ± 10% operation
- Commercial and industrial temperatures
- 28-pin (330 mil) SOIC, 28-pin (300 mil) PDIP, 28-pin (600 mil) PDIP packages
- 28-pin (300 mil) CDIP and 28-pad (350 mil) LCC packages
- RoHS compliance

Functional Description

The Cypress STK12C68 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the $\overline{HSB}$ pin.

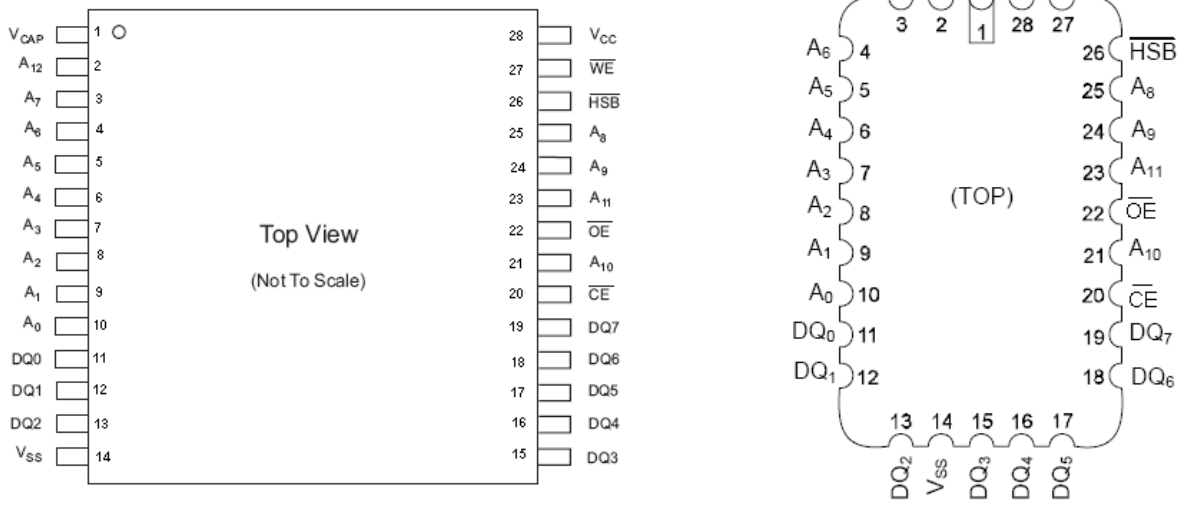
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 28-Pin SOIC/DIP and LLC



Pin Definitions

Pin Name	Alt	I/O Type	Description
A_0–A_{12}		Input	**Address Inputs.** Used to select one of the 8,192 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data I/O Lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$		Input or Output	**Hardware Store Busy ($\overline{HSB}$)**. When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V_{CAP}		Power Supply	**AutoStore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The STK12C68 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM Read and Write operations are inhibited. The STK12C68 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

SRAM Read

The STK12C68 performs a Read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-12} determines the 8,192 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (Read cycle 1). If the Read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A Write cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the Write cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled Write or before the end of an $\overline{CE}$ controlled Write. Keep $\overline{OE}$ HIGH during the entire Write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The STK12C68 stores data to nvSRAM using one of three storage operations:

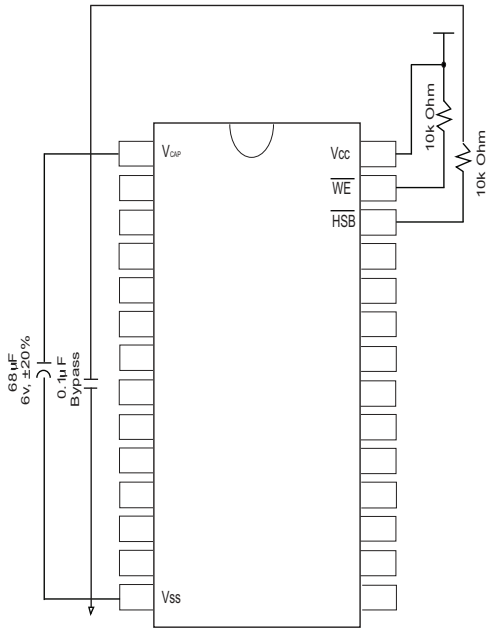
1. Hardware store activated by $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power-down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the STK12C68.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. A charge storage capacitor between 68 µF and 220 µF (±20%) rated at 6 V should be provided. The voltage on the V_{CAP} pin is driven to 5 V by a charge pump internal to the chip. A pull-up is placed on $\overline{WE}$ to hold it inactive during power-up.

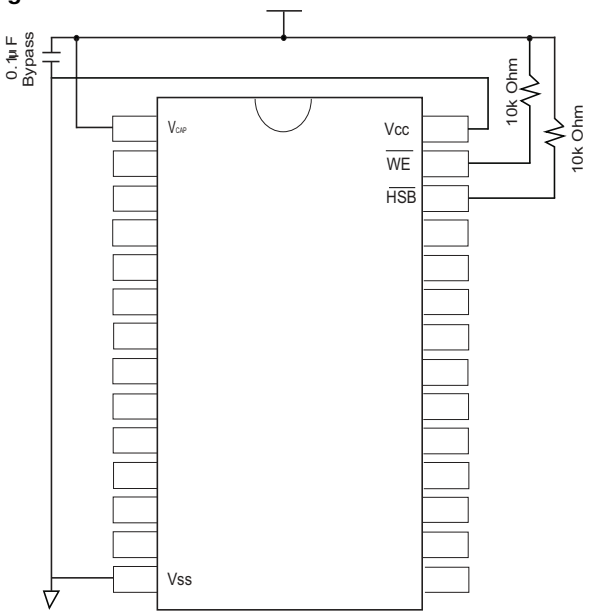
Figure 2. AutoStore Mode



In system power mode, both V_{CC} and V_{CAP} are connected to the +5 V power supply without the 68 µF capacitor. In this mode, the AutoStore function of the STK12C68 operates on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6 V during the 10 ms STORE cycle.

To reduce unnecessary nonvolatile stores, AutoStore, and Hardware Store operations are ignored, unless at least one Write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a Write operation has taken place. An optional pull-up resistor is shown connected to HSB. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 3. AutoStore Inhibit Mode



If the power supply drops faster than 20 us/volt before V_{cc} reaches V_{SWITCH}, then a 2.2 Ω resistor should be connected between V_{CC} and the system supply to avoid momentary excess of current between V_{CC} and V_{CAP}.

AutoStore Inhibit Mode

If an automatic STORE on power loss is not required, then V_{CC} is tied to ground and +5 V is applied to V_{CAP} (Figure 3). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK12C68 is operated in this configuration, references to V_{CC} are changed to V_{CAP} throughout this data sheet. In this mode, STORE operations are triggered through software control or the HSB pin. To enable or disable Autostore using an I/O port pin see Preventing Store on page 6. It is not permissible to change between these three options “on the fly”.

Hardware STORE ($\overline{HSB}$) Operation

The STK12C68 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The HSB pin is used to request a hardware STORE cycle. When the HSB pin is driven LOW, the STK12C68 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a Write to the SRAM takes place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress.

SRAM Read and Write operations, that are in progress when HSB is driven LOW by any means, are given time to complete before the STORE operation is initiated. After HSB goes LOW, the STK12C68 continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM Read operations take place. If a Write is in progress when HSB is pulled LOW, it allows a time, t_{DELAY} to complete. However, any SRAM Write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH.

During any STORE operation, regardless of how it is initiated, the STK12C68 continues to drive the HSB pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK12C68 remains disabled until the HSB pin returns HIGH.

If $\overline{HSB}$ is not used, it is left unconnected.

Hardware RECALL (Power-up)

During power-up or after any low power condition (V_{CC} < V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the STK12C68 is in a Write state at the end of power-up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 kΩ resistor is connected either between WE and system V_{CC} or between CE and system V_{CC}.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK12C68 software STORE cycle is initiated by executing sequential CE controlled Read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of Reads from specific addresses is used for STORE initiation, it is important that no other Read or Write accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following Read sequence is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence is clocked with CE controlled Reads or OE controlled Reads. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that Read cycles and not Write cycles are used in the sequence. It is not necessary that OE is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for Read and Write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of Read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled Read operations is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for Read and Write operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

Data Protection

The STK12C68 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and Write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the STK12C68 is in a Write mode (both CE and WE are low) at power-up after a RECALL or after a STORE, the Write is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power-up or brown out conditions.

Noise Considerations

The STK12C68 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Hardware Protect

The STK12C68 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When V_{CAP}<V_{SWITCH}, all externally initiated STORE operations and SRAM Writes are inhibited. AutoStore can be completely disabled by tying VCC to ground and applying +5 V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode, STOREs are only initiated by explicit request using either the software sequence or the HSB pin.

Low Average Active Power

CMOS technology provides the STK12C68 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 shows the relationship between I_{CC} and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5 V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK12C68 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The V_{CC} level
- I/O loading

Figure 4. Current Versus Cycle Time (Read)

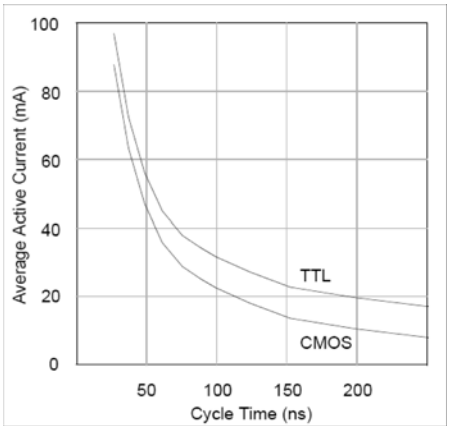
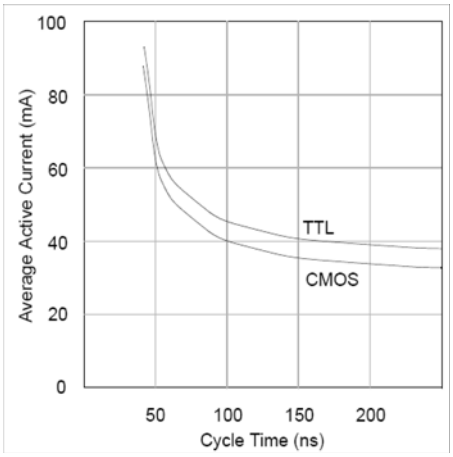


Figure 5. Current Versus Cycle Time (Write)



Preventing Store

The STORE function is disabled by holding HSB high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2 V, because it must overpower the internal pull-down device. This device drives HSB LOW for 20 µs at the onset of a STORE. When the STK12C68 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 attempts to pull HSB LOW. If HSB does not actually get below V_{IL}, the part stops trying to pull HSB LOW and abort the STORE attempt.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger V_{CAP} value to make sure there is extra store charge should discuss their V_{CAP} size selection with Cypress.

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{HSB}$	A12–A0	Mode	I/O	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active[3]
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	I_{CC2}[1]
L	H	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[2, 3]
L	H	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[2, 3]

Notes
1. $\overline{HSB}$ STORE operation occurs only if an SRAM Write is done since the last nonvolatile cycle. After the STORE (If any) completes, the part goes into standby mode, inhibiting all operations until $\overline{HSB}$ rises.
2. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.
3. I/O state assumes $\overline{OE} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{OE}$.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Temperature under Bias ..... –55 °C to +125 °C

Voltage on Input Relative to GND..... –0.5 V to 7.0 V

Voltage on Input Relative to V_{SS} ..... –0.6 V to V_{CC} + 0.5 V

Voltage on DQ_{0-7} or $\overline{HSB}$ ..... –0.5 V to V_{CC} + 0.5 V

Power Dissipation..... 1.0 W

DC output Current (1 output at a time, 1s duration) .... 15 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	4.5 V to 5.5 V
Industrial	–40 °C to +85 °C	4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range (V_{CC} = 4.5V to 5.5V) [4]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.		–	85 75 65	mA mA mA
I_{CC2}	Average V_{CC} current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}		–	3	mA
I_{CC3}	Average V_{CC} current at t_{RC}= 200 ns, 5 V, 25 °C Typical	$\overline{WE} \geq (V_{CC} - 0.2\ V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.		–	10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}		–	2	mA
I_{SB1} [5]	V_{CC} standby current (standby, cycling TTL input levels)	t_{RC} = 25 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 35 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 45 ns, $\overline{CE} \geq V_{IH}$		–	27 24 20	mA mA mA
I_{SB2} [5]	V_{CC} standby current	$\overline{CE} \geq (V_{CC} - 0.2\ V)$. All others $V_{IN} \leq 0.2$ V or $\geq (V_{CC} - 0.2\ V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	Commercial	–	1.5	mA
			Industrial	–	2.5	mA
I_{IX}	Input leakage current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		–1	+1	µA
I_{IX}	Input leakage current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		–1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		–-5	+5	µA
V_{IH}	Input HIGH voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –4 mA		2.4		V
V_{OL}	Output LOW voltage	I_{OUT} = 8 mA		–	0.4	V
V_{BL}	Logic ‘0’ voltage on $\overline{HSB}$ output	I_{OUT} = 3 mA		–	0.4	V
V_{CAP}	Storage capacitor	Between V_{CAP} pin and V_{SS}, 6 V rated. 68 µF ±20% nominal		54	260	µF

Notes

4. V_{CC} reference levels throughout this data sheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if VCC is connected to ground.
5. $\overline{CE} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data retention	100	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

In the following table, the capacitance parameters are listed.[6]

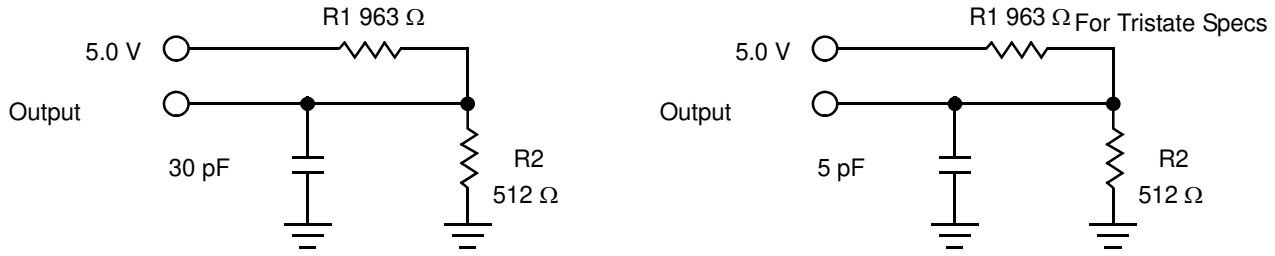
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 0 to 3.0 V	8	pF
C_{OUT}	Output capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[6]

Parameter	Description	Test Conditions	28-SOIC	28-PDIP (300 mil)	28-PDIP (600 mil)	28-CDIP	28-LCC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.55	45.16	55.84	46.1	95.31	°C/W
Θ_{JC}	Thermal resistance (junction to case)		27.95	31.62	25.74	5.01	9.01	°C/W

Figure 6. AC Test Loads



AC Test Conditions

Input pulse levels.....0 V to 3 V
Input rise and fall times (10% to 90%)..... ≤5 ns
Input and output timing reference levels 1.5

Note
6. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip enable access time	–	25	–	35	–	45	ns
t_{RC} [7]	t_{AVAV}, t_{ELEH}	Read cycle time	25	–	35	–	45	–	ns
t_{AA} [8]	t_{AVQV}	Address access time	–	25	–	35	–	45	ns
t_{DOE}	t_{GLQV}	Output enable to data valid	–	10	–	15	–	20	ns
t_{OHA} [8]	t_{AXQX}	Output hold after address change	5	–	5	–	5	–	ns
t_{LZCE} [9]	t_{ELQX}	Chip enable to output active	5	–	5	–	5	–	ns
t_{HZCE} [9]	t_{EHQZ}	Chip disable to output inactive	–	10	–	10	–	12	ns
t_{LZOE} [9]	t_{GLQX}	Output enable to output active	0	–	0	–	0	–	ns
t_{HZOE} [9]	t_{GHQZ}	Output disable to output inactive	–	10	–	10	–	12	ns
t_{PU} [6]	t_{ELICCH}	Chip enable to power active	0	–	0	–	0	–	ns
t_{PD} [6]	t_{EHICCL}	Chip disable to power standby	–	25	–	35	–	45	ns

Switching Waveforms

Figure 7. SRAM Read Cycle 1: Address Controlled [7, 8]

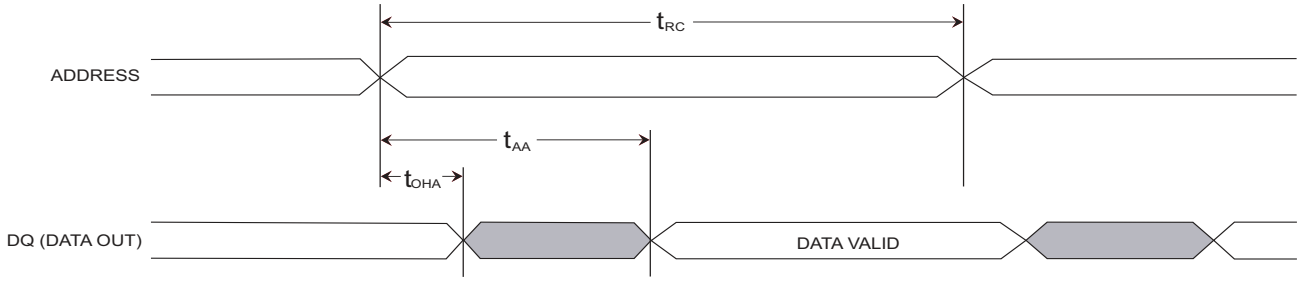
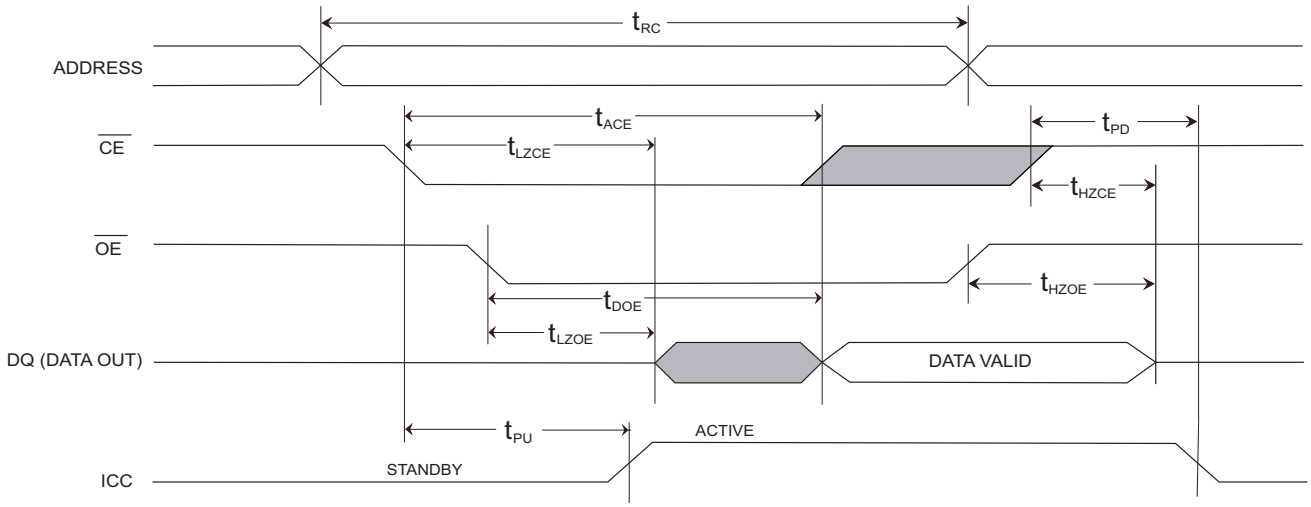


Figure 8. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [7]



Notes
7. $\overline{WE}$ and $\overline{HSB}$ must be High during SRAM Read cycles.
8. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
9. Measured ±200 mV from steady state output voltage.

SRAM Write Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write cycle time	25	–	35	–	45	–	ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write pulse width	20	–	25	–	30	–	ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip enable to end of write	20	–	25	–	30	–	ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data setup to end of write	10	–	12	–	15	–	ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data hold after end of write	0	–	0	–	0	–	ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address setup to end of write	20	–	25	–	30	–	ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address setup to start of write	0	–	0	–	0	–	ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address hold after end of write	0	–	0	–	0	–	ns
t_{HZWE} [9,10]	t_{WLQZ}	Write enable to output disable	–	10	–	13	–	14	ns
t_{LZWE} [9]	t_{WHQX}	Output active after end of write	5	–	5	–	5	–	ns

Switching Waveforms

Figure 9. SRAM Write Cycle 1: $\overline{WE}$ Controlled [11, 12]

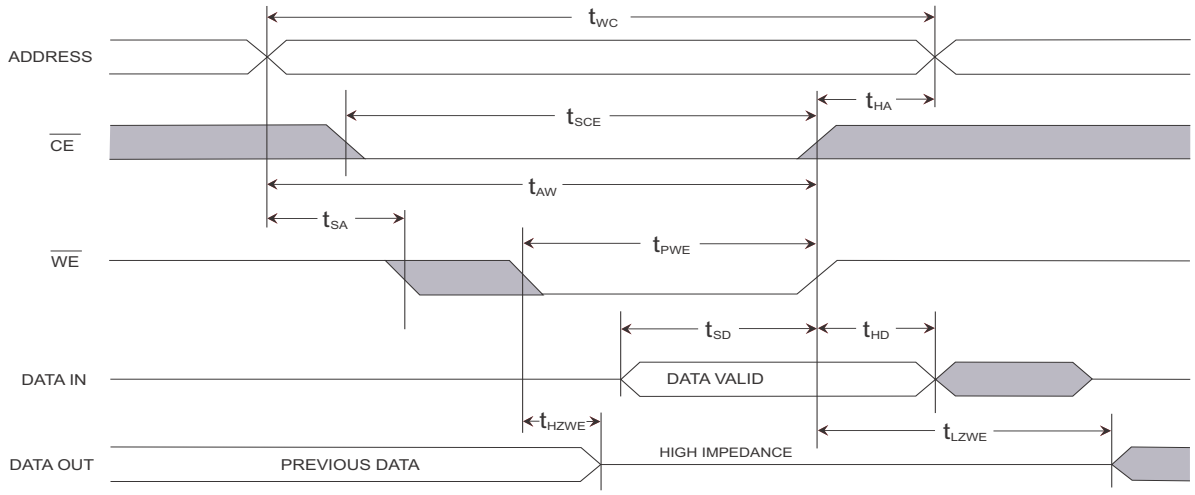
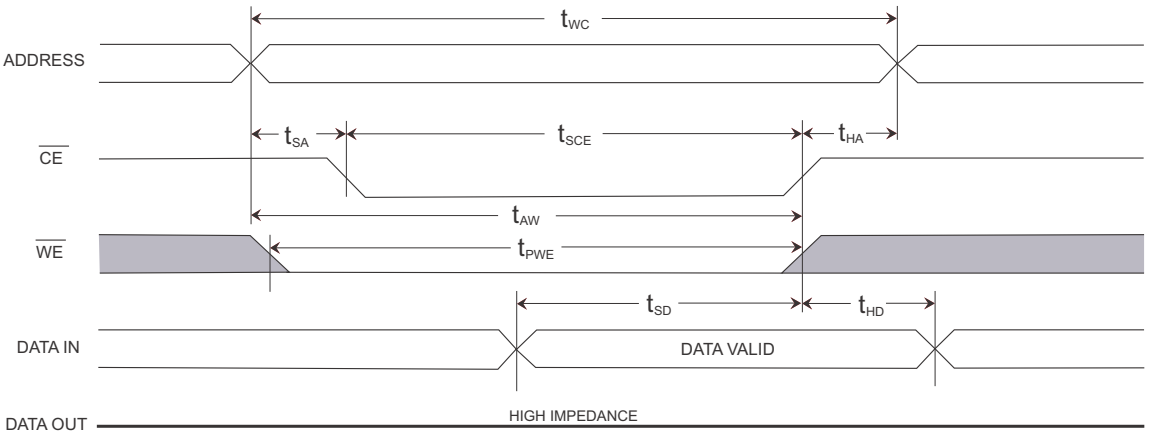


Figure 10. SRAM Write Cycle 2: $\overline{CE}$ Controlled [11, 12]



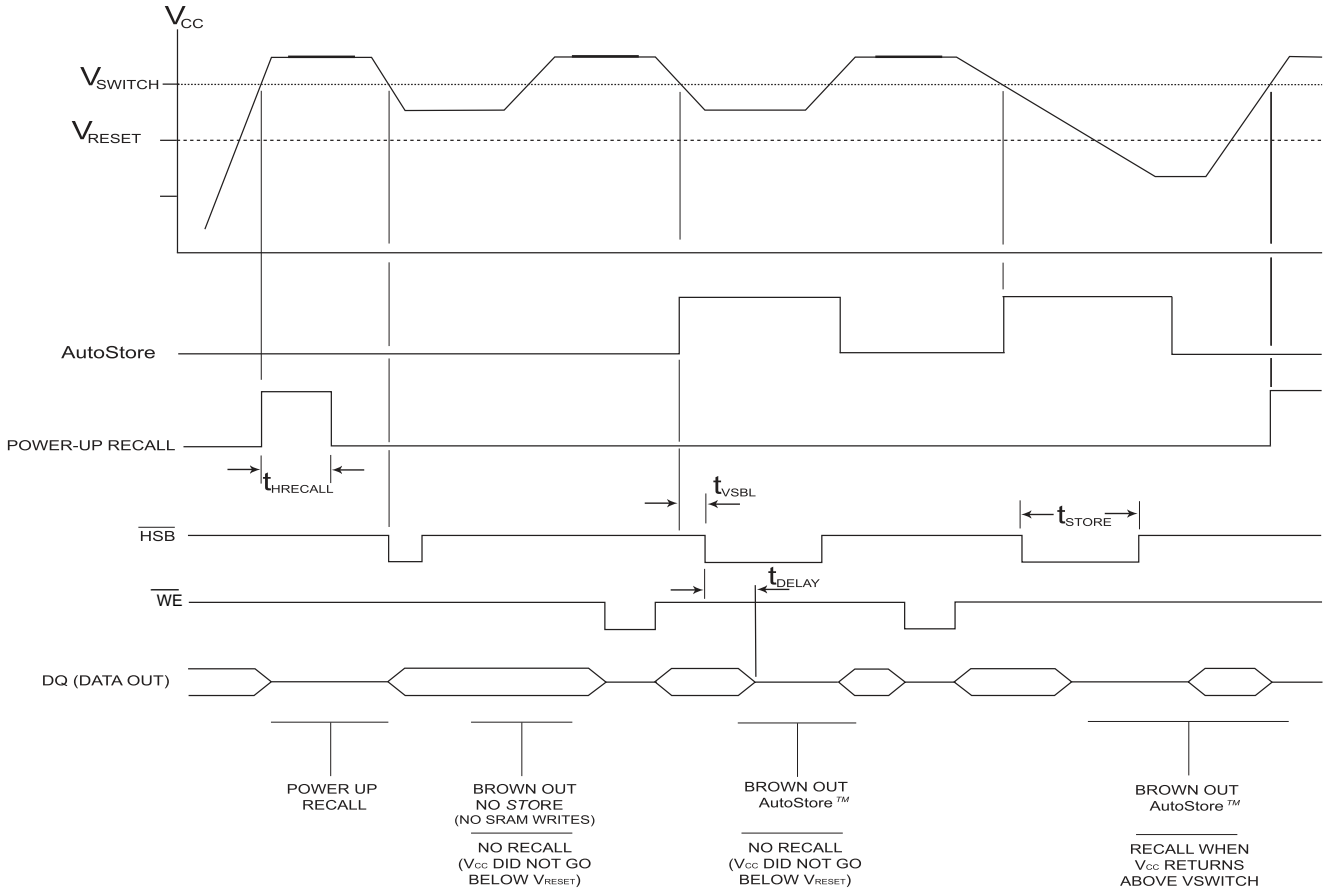
Notes
10. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
11. $\overline{HSB}$ must be high during SRAM Write cycles.
12. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

AutoStore or Power-up RECALL

Parameter	Alt	Description	STK12C68		Unit
			Min	Max	
$t_{HRECALL}$ [13]	$t_{RESTORE}$	Power-up RECALL duration	–	550	µs
t_{STORE} [14, 15, 16]	t_{HLHZ}	STORE cycle duration	–	10	ms
t_{DELAY} [9, 15]	t_{HLQZ} , t_{BLQZ}	Time allowed to complete SRAM cycle	1	–	µs
V_{SWITCH}		Low voltage trigger level	4.0	4.5	V
V_{RESET}		Low voltage reset level	–	3.9	V
$t_{VCCRISE}$		V_{CC} rise time	150	–	µs
t_{VSBL} [11]		Low voltage trigger (V_{SWITCH}) to $\overline{HSB}$ Low	–	300	ns

Switching Waveform

Figure 11. AutoStore/Power-up RECALL



Notes

13. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
14. $\overline{CE}$ and $\overline{OE}$ low for output behavior.
15. $\overline{CE}$ and $\overline{OE}$ low and WE high for output behavior.
16. $\overline{HSB}$ is asserted low for 1us when V_{CAP} drops through V_{SWITCH}. If an SRAM Write has not taken place since the last nonvolatile cycle, $\overline{HSB}$ is released and no store takes place.

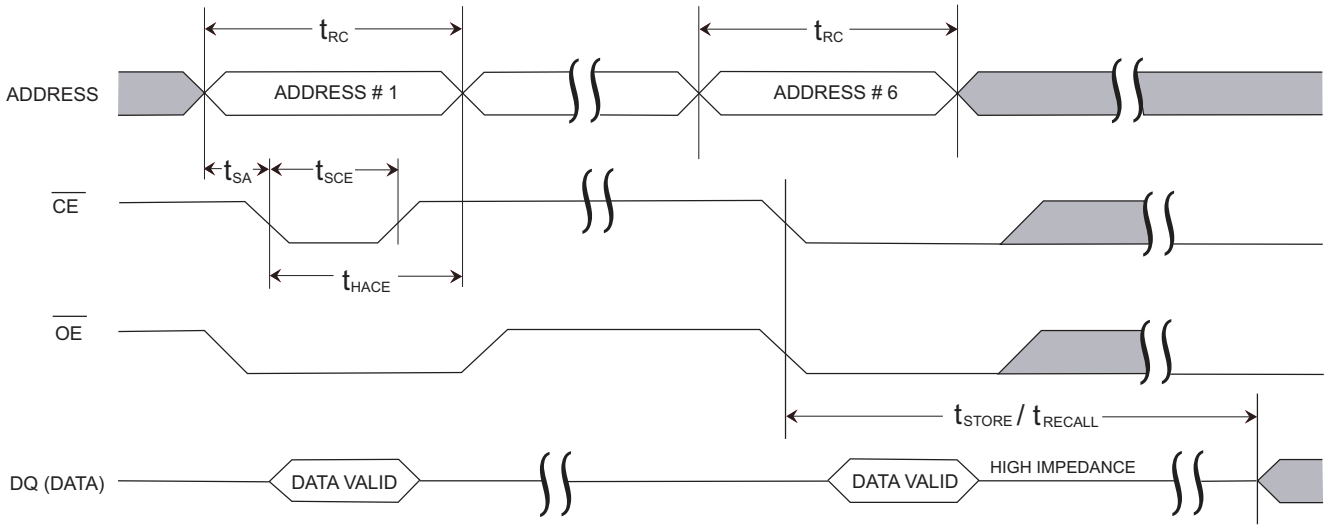
Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [18]

Parameter	Alt	Description	25 ns		35 ns		45 ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}[14]	t_{AVAV}	STORE/RECALL initiation cycle time	25	–	35	–	45	–	ns
t_{SA}[17]	t_{AVEL}	Address setup time	0	–	0	–	0	–	ns
t_{CW}[17]	t_{ELEH}	Clock pulse width	20	–	25	–	30	–	ns
t_{HACE}[17]	t_{ELAX}	Address hold time	20	–	20	–	20	–	ns
t_{RECALL}		RECALL duration	–	20	–	20	–	20	µs

Switching Waveform

Figure 12. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [18]



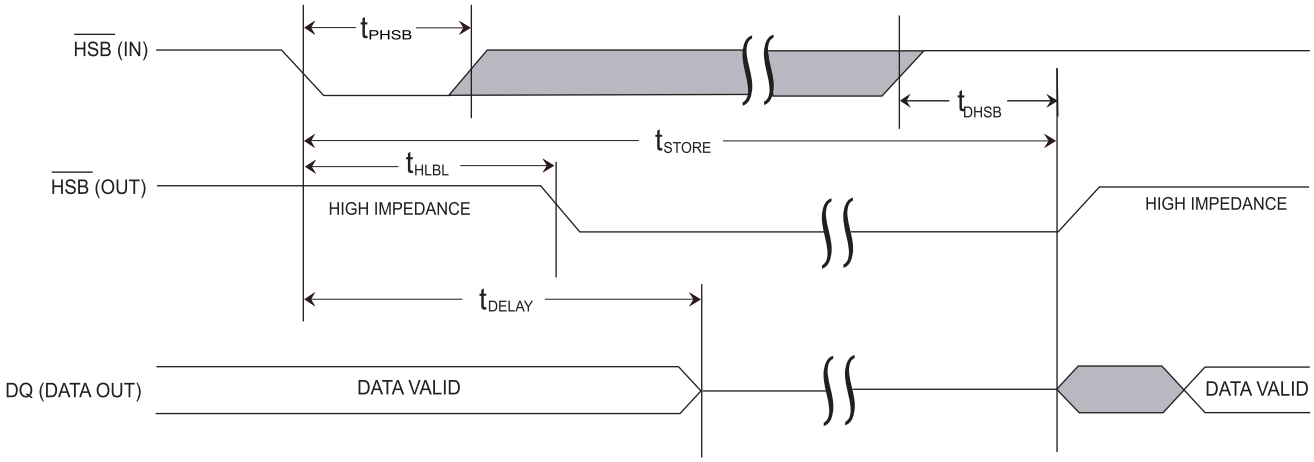
Notes
17. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking aborts the sequence).
18. The six consecutive addresses must be read in the order listed in Table 1 on page 7. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Hardware STORE Cycle

Parameter	Alt	Description	STK12C68		Unit
			Min	Max	
t_{STORE} [9, 14]	t_{HLHZ}	STORE Cycle duration		10	ms
t_{DHSB} [14, 19]	$t_{RECOVER}$, t_{HHQX}	Hardware STORE High to inhibit off		700	ns
t_{PHSB}	t_{HLHX}	Hardware STORE pulse width	15		ns
t_{HLBL}		Hardware STORE Low to STORE busy		300	ns

Switching Waveform

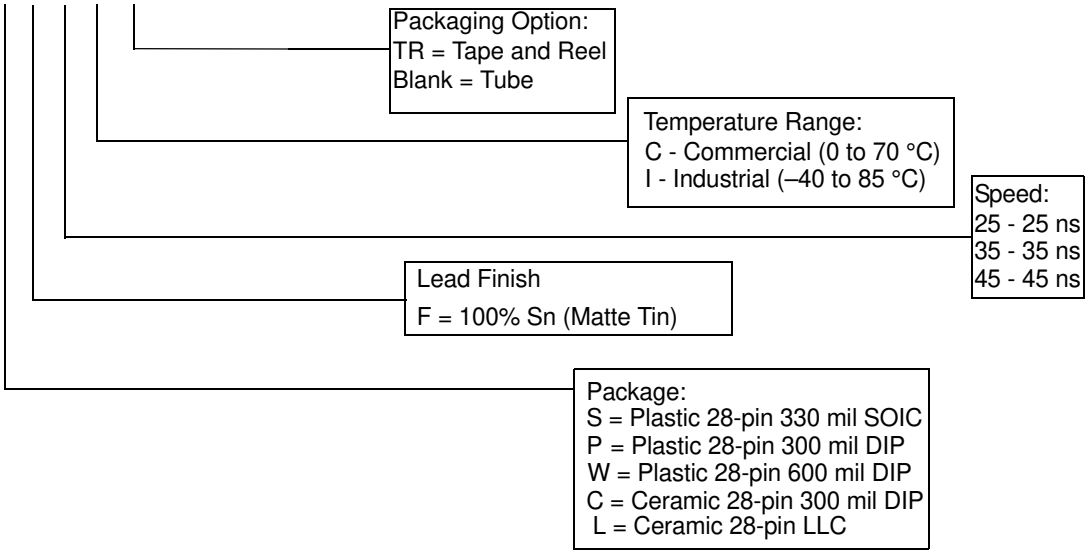
Figure 13. Hardware STORE Cycle



Note
19. t_{DHSB} is only applicable after t_{STORE} is complete.

Part Numbering Nomenclature

STK12C68 - S F 45 I TR



Ordering Information

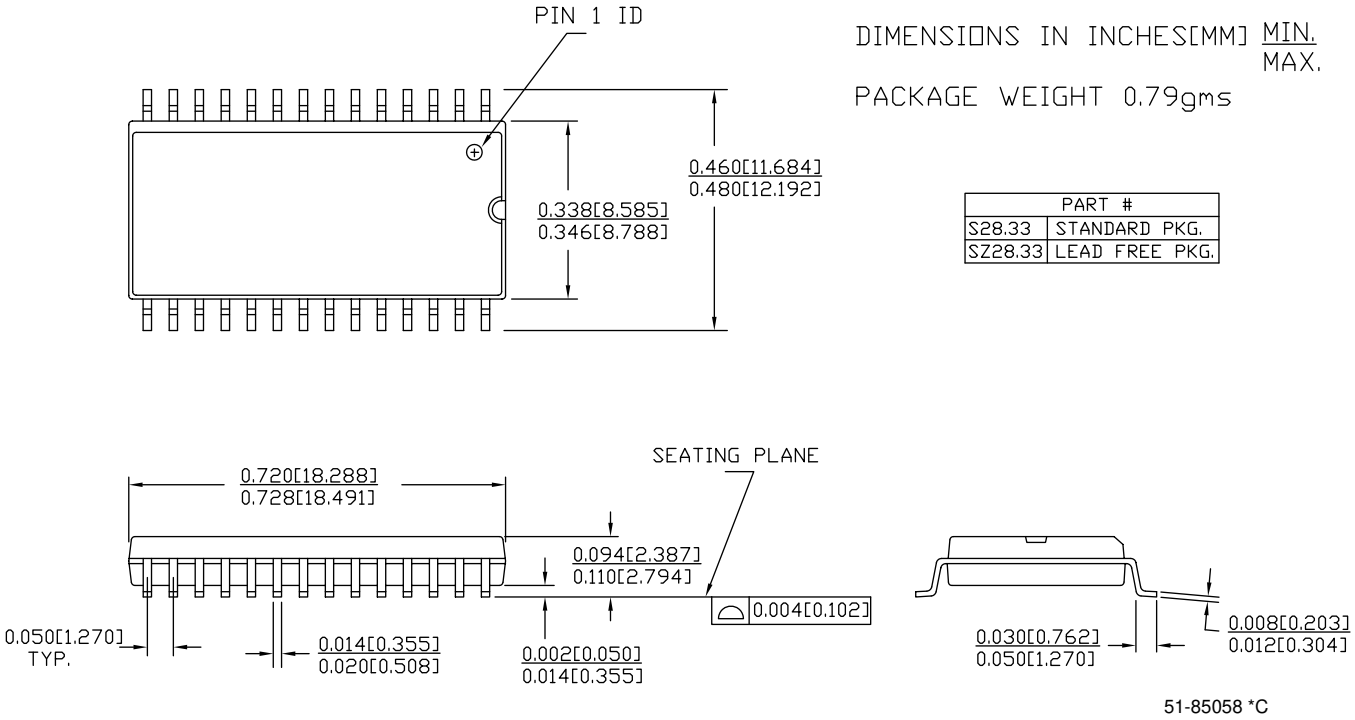
These parts are not recommended for new designs. They are in production to support ongoing production programs only.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	STK12C68-SF25TR	51-85058	28-pin SOIC (330 mil)	Commercial
	STK12C68-SF25	51-85058	28-pin SOIC (330 mil)	
	STK12C68-SF25ITR	51-85058	28-pin SOIC (330 mil)	Industrial
	STK12C68-SF25I	51-85058	28-pin SOIC (330 mil)	
	STK12C68-PF25I	51-85014	28-pin PDIP (300 mil)	
45	STK12C68-SF45TR	51-85058	28-pin SOIC (330 mil)	Commercial
	STK12C68-SF45	51-85058	28-pin SOIC (330 mil)	
	STK12C68-SF45ITR	51-85058	28-pin SOIC (330 mil)	Industrial
	STK12C68-SF45I	51-85058	28-pin SOIC (330 mil)	
	STK12C68-C45I	001-51695	28-pin CDIP (300 mil)	

All parts are Pb-free. The above table contains Final information. Contact your local Cypress sales representative for availability of these parts

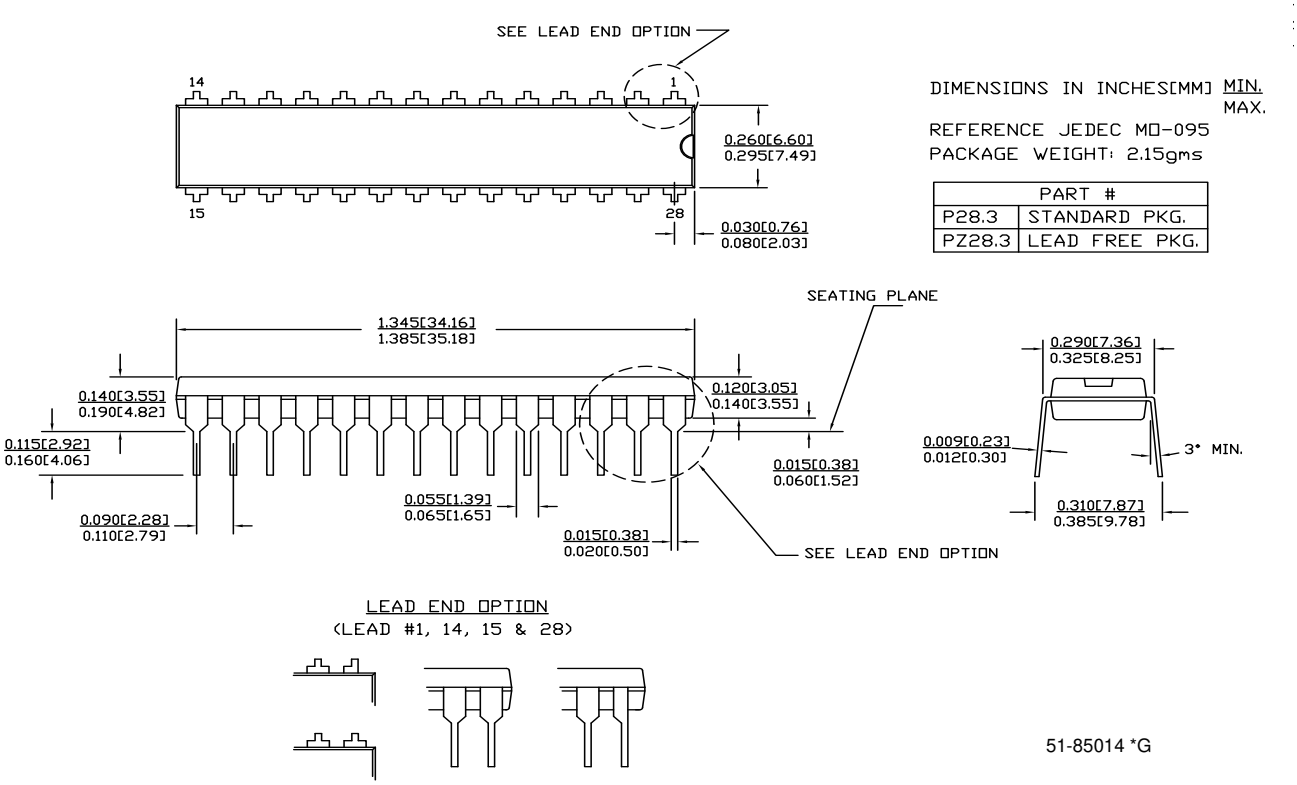
Package Diagrams

Figure 14. 28-Pin (330 Mil) SOIC (51-85058)



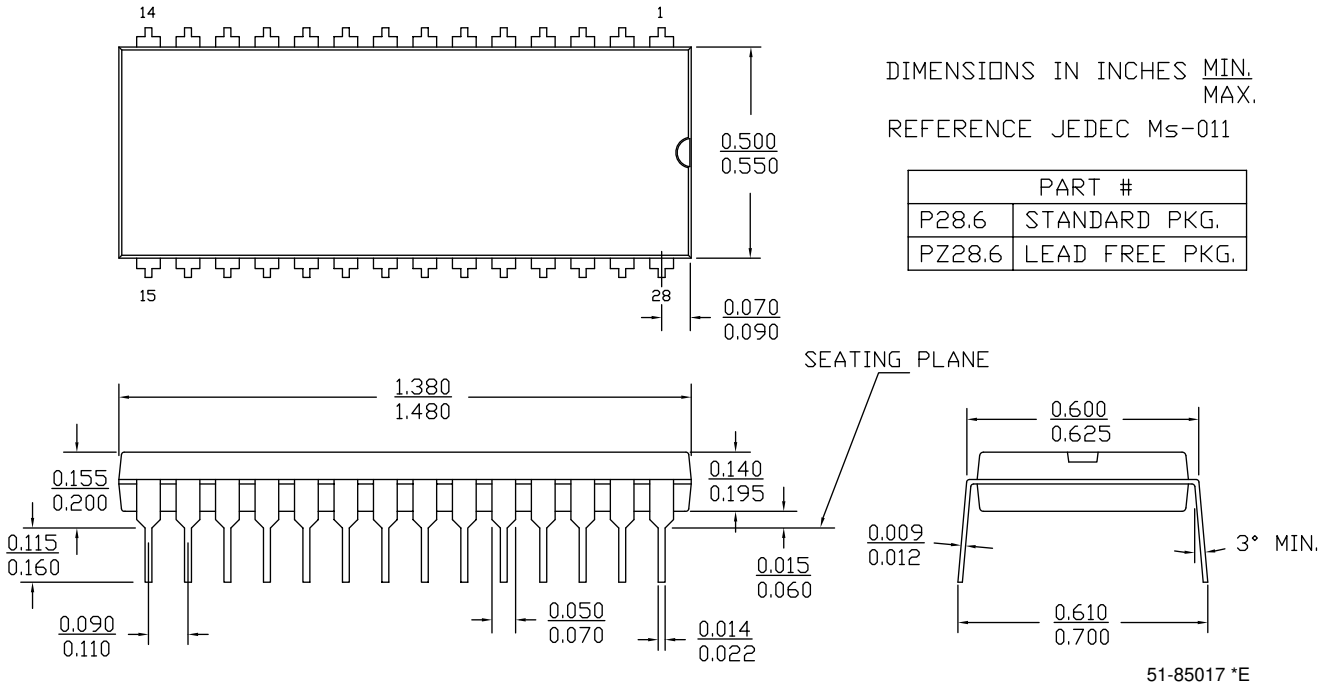
Package Diagrams (continued)

Figure 15. 28-Pin (300 Mil) PDIP (51-85014)



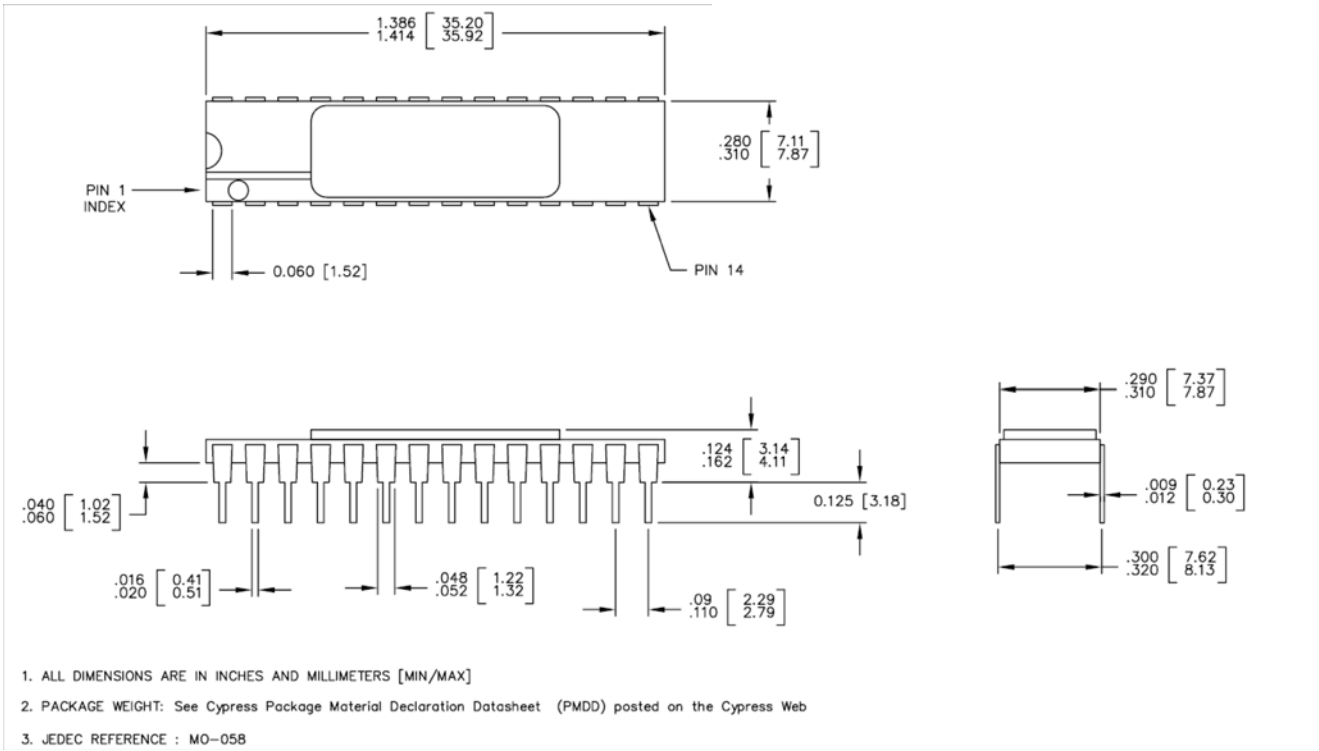
Package Diagrams (continued)

Figure 16. 28-Pin (600 Mil) PDIP (51-85017)



Package Diagrams (continued)

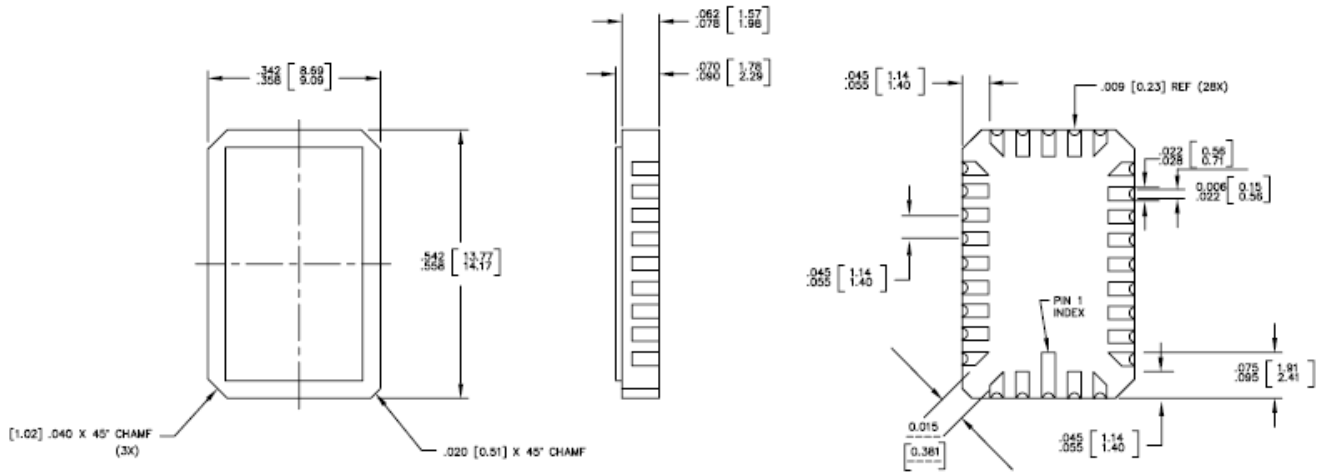
Figure 17. 28-Pin (300 Mil) Side Braze DIL (001-51695)



001-51695 *B

Package Diagrams (continued)

Figure 18. 28-Pad (350 Mil) LCC (001-51696)



1. ALL DIMENSION ARE IN INCHES AND MILLIMETERS [MIN/MAX]
2. JEDEC 95 OUTLINE# MO-041
3. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web

001-51696 *B

Document History Page

Document Title: STK12C68 64 Kbit (8 K x 8) AutoStore nvSRAM Document Number: 001-51027				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2606744	GVCH	01/30/2009	New data sheet
*A	2826441	GVCH	12/11/2009	Added following text in the Ordering Information section: “These parts are not recommended for new designs. In production to support ongoing production programs only.” Added watermark in PDF stating “Not recommended for new designs. In production to support ongoing production programs only.” Added Contents on page 2.
*B	3054694	GVCH	10/12/2010	Removed the following prune parts from the document; STK12C68-C35I STK12C68-C45 STK12C68-L35 STK12C68-L35I STK12C68-L45 STK12C68-L45I STK12C68-PF25 STK12C68-PF45 STK12C68-PF45I STK12C68-WF45 STK12C68-WF45I STK12C68-WF25
*C	3189527	GVCH	03/07/2011	Added watermark in PDF stating “Not recommended for new designs. In production to support ongoing production programs only.”
*D	3208949	GVCH	03/30/11	Removed pruned part “STK12C68-C35” from the ordering code information.
*E	3229103	GVCH	04/15/11	Added missing watermark “Not Recommended for New Designs. In production to support ongoing production programs only.” that was found in *C revision.
*F	3402039	GVCH	10/12/2011	Removed pruned device STK12C68-WF25I from Ordering Information. Updated Package Diagrams and Table of Contents.
*G	4303589	GVCH	03/21/2014	Figure 17: Updated Package diagram from *A to *B revision Figure 18: Updated Package diagram from *A to *B revision Sunset review

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