Peregrine Semiconductor

Product Specification

PE42540

UltraCMOS® SP4T RF Switch
10 Hz – 8 GHz

Product Description

The PE42540 is a HaRP™ technology-enhanced absorptive SP4T RF switch developed on UltraCMOS® process technology. This switch is designed specifically to support the requirements of the test equipment and ATE market. It is comprised of four symmetric RF ports and has very high isolation. An on-chip CMOS decode logic facilitates a two-pin low voltage CMOS control interface and an optional external V_{SS} feature. High ESD tolerance and no blocking capacitor requirements make this the ultimate in integration and ruggedness.

The PE42540 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™ technology enhanced
  - Fast settling time
  - Eliminates gate and phase lag
  - No drift in insertion loss and phase
- High linearity: 58 dBm IIP3
- Low insertion loss: 0.8 dB @ 3 GHz, 1.0 dB @ 6 GHz and 1.2 dB @ 8 GHz
- High isolation: 45 dB @ 3 GHz, 39 dB @ 6 GHz and 31 dB @ 8 GHz
- Maximum power handling: 30 dBm @ 8 GHz
- High ESD tolerance of 2 kV HBM on RFC and 1 kV HBM on all other pins

Figure 1. Functional Diagram

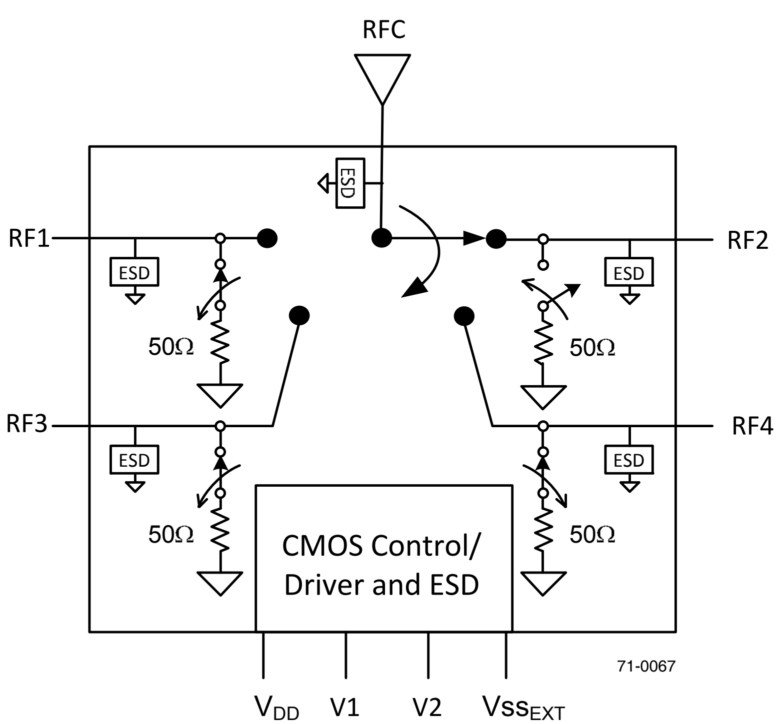


Figure 2. Package Type

32-lead 5x5 mm LGA

Table 1. Electrical Specifications @ 25°C, V_{DD} = 3.3V, Vss_{EXT} = 0V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Unit
Operating Frequency		10 Hz[1]		8 GHz	
RFC–RFX Insertion Loss	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz		0.7 0.8 1.0 1.1 1.2	1.0 1.1 1.3 1.5 1.6	dB dB dB dB dB
RFX–RFX Isolation	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	70 40 34 27 25	80 45 39 32 31		dB dB dB dB dB
RFC–RFX Isolation	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	74 40 28 24 21	84 45 33 29 27		dB dB dB dB dB
Return Loss (RFC to active port)	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz		24 23 18 14 13		dB dB dB dB dB
Return Loss (terminated port)	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz		35 18 13 11 10		dB dB dB dB dB
Settling Time	50% CTRL to 0.05dB final value (–40 to +85°C) *Rising Edge* 50% CTRL to 0.05dB final value (–40 to +85°C) *Falling Edge*		14 15	18 45	µs µs
Switching Time (T_{SW})	50% CTRL to 90% or 10% RF		5	8	µs
P1dB[1] Input 1 dB Compression RFX–RFC	All bands @ 1:1 VSWR, 100% duty cycle	31	33		dBm
Input IP3	8000 MHz		58		dBm
Input IP2	8000 MHz		100		dBm

Note 1: Maximum Operating Pin (50Ω) is shown in *Table 3.* Please refer to *Figures 4, 5,* and *6* when operating the part at low frequency

Figure 3. Pin Configuration (Top View)

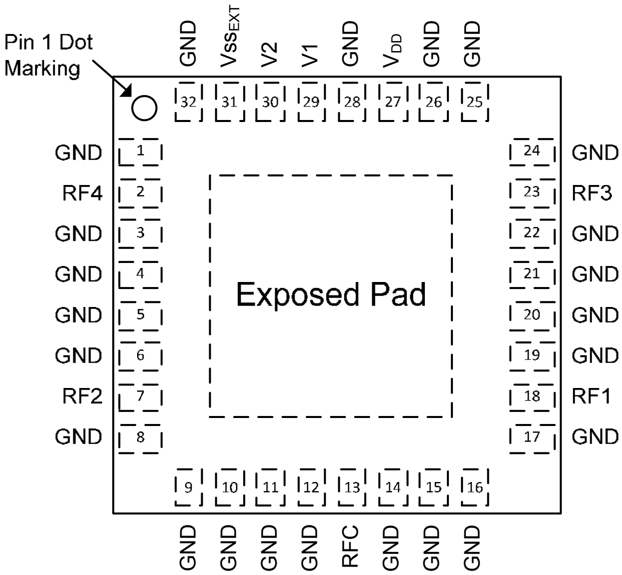


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3-6, 8, 9-12, 14-17, 19-22, 24-26, 28, 32	GND	Ground
2	RF4[2]	RF I/O
7	RF2[2]	RF I/O
13	RFC[2]	RF Common
18	RF1[2]	RF I/O
23	RF3[2]	RF I/O
27	V_{DD}	Supply
29	V1	Switch control input, CMOS logic level
30	V2	Switch control input, CMOS logic level
31	Vss_{EXT}[1]	External V_{SS} Negative Voltage
Paddle	GND	Exposed solder pad: Ground for proper operation

Notes: 1. Use Vss_{EXT} (pin 31, $Vss_{EXT} = -V_{DD}$) to bypass and disable internal negative voltage generator. Connect Vss_{EXT} (pin 31) to GND (Vss_{EXT} = 0V) to enable internal negative voltage generator
2. All RF pins must be DC blocked with an external series capacitor or held at 0 VDC

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Supply Voltage	3.0	3.3	3.55	V
Vss_{EXT} Negative Power Supply Voltage[1]	-3.6	-3.3	-3.0	V
Iss Negative Supply Current		-10	-40	µA
I_{DD} Power Supply Current V_{DD} = 3.3V, Vss_{EXT} = 0V, Temp = +85°C		90	160	µA
I_{DD} Power Supply Current V_{DD} = 3.6V, Vss_{EXT} used			50	µA
V_{CTRL} Control Voltage High	1.2	1.5	V_{DD}	V
V_{CTRL} Control Voltage Low	0	0	0.4	V
I_{CTRL} Control Current			1	µA
P_{IN} Thru Path[2] (50Ω, RF Power in) 9 kHz – 8 GHz			*figs. 4,5,6*	
P_{max} Max power into termination (50Ω) 9 kHz ≤ 6 MHz[2,3] 6 MHz – 8 GHz[2,3]			*figs. 4,5,6* 20	dBm
P_{max} Max power, hot switching (50Ω) 9 kHz ≤ 6 MHz[2,3] 6 MHz – 8 GHz[2,3]			*figs. 4,5,6* 20	dBm
T_{OP} Operating temperature range	–40		+85	°C

Notes: 1. Applies only when external V_{SS} power supply is used. Otherwise, Vss_{EXT} = 0
2. 100% duty cycle (–40 to +85°C, 1:1 VSWR)
3. Do not exceed 20 dBm

Table 4. Absolute Maximum Ratings

Parameter/Condition	Min	Max	Unit
T_{ST} Storage temperature range	–60	+150	°C
V_{DD} Supply Voltage	–0.3	4	V
V_{CTRL} Control Voltage, V1 and V2		4	V
P_{IN} Thru Path (50Ω, RF Power in) 9 kHz – 8 GHz		*figs.* *4,5,6*	
P_{max} Max power into termination (50Ω) 9 kHz ≤ 6 MHz[1] 6 MHz – 8 GHz		*figs.* *4,5,6* 20	 dBm
V_{ESD} ESD Voltage HBM[2] RFC All Pins		 2000 1000	 V V
V_{ESD} ESD Voltage MM, all pins[3]		100	V

Notes: 1. Do not exceed 20 dBm
2. HBM, MIL-STD 883 Method 3015.7
3. MM JEDEC JESD22-A115-A

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42540 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 31 = GND). The rate at which the PE42540 can be switched is only limited to the switching time (*Table 1*) if an external negative supply is provided at (pin 31 = Vss_{EXT}).

Optional External Vss Control (Vss_{EXT})

For proper operation, the Vss_{EXT} control pin must be grounded or tied to the Vss voltage specified in *Table 3*. When the Vss_{EXT} control pin is grounded, FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spur performance, Vss_{EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious Performance

The typical spurious performance of the PE42540 is –144 dBm when Vss_{EXT} = 0V (pin 31 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting $Vss_{EXT} = -V_{DD}$.

Table 5. Truth Table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42540 in the 32-lead 5x5 mm LGA package is MSL3.

Low Frequency Operation

Table 6 shows the minimum and maximum voltage limits when operating the device under various V_{DD} and Vss_{EXT} voltage conditions below 9 kHz. Refer to *Figures 4, 5,* and *6* to determine the maximum operating power over the frequency range of the device.

Table 6. Instantaneous RF Pin Voltage Limits for Operation Below 9 kHz

V_{DD}	Vss_{EXT}	Minimum Peak Voltage at RF Port	Maximum Peak Voltage at RF Port
≥3.0	0.0	–0.2	1.2
3.0	–3.0	–0.6	1.6
3.3	–3.3	–0.3	1.3
3.5	–3.5	–0.1	1.1
3.6	–3.6	0.0	1.0

Maximum Operating Power vs. Frequency

Figures 4, *5*, and *6* show the power limit of the device will increase with frequency. As the frequency increases, the contours and maximum power limit will increase as shown in the curves.

Figure 4. Maximum Operating Power vs. Frequency ($T_{ambient}$ = 25°C)

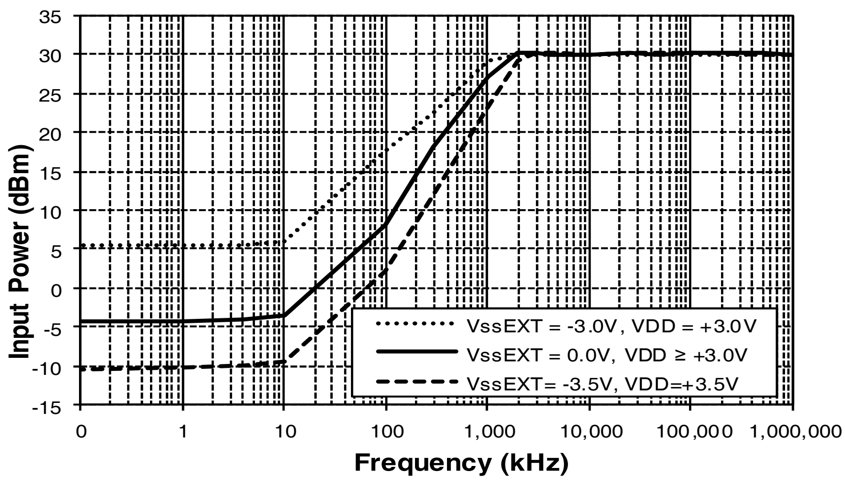


Figure 5. Maximum Operating Power vs. Frequency ($T_{ambient}$ = 50°C)

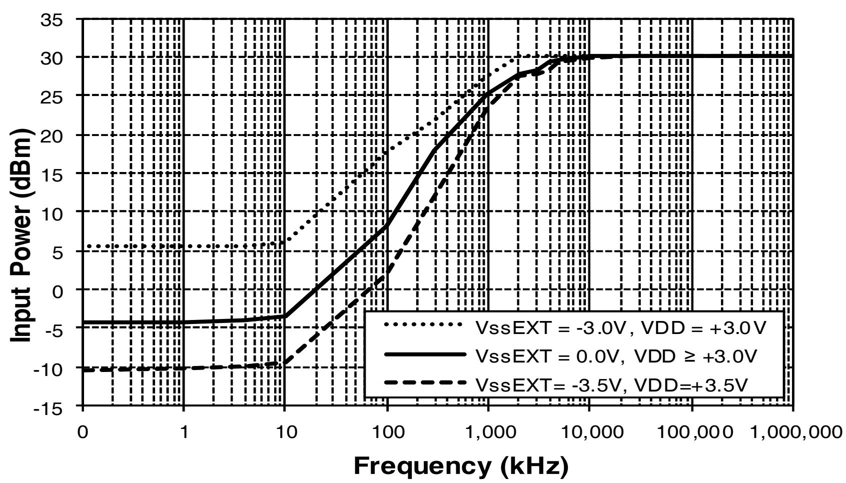


Figure 6. Maximum Operating Power vs. Frequency ($T_{ambient}$ = 85°C)

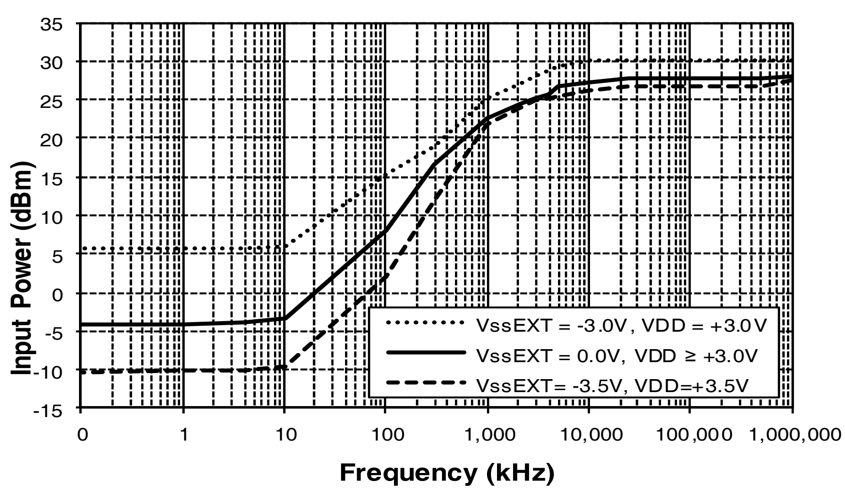


Figure 7. Insertion Loss vs. V_{DD} (Temp = 25°C, Vss = 0)

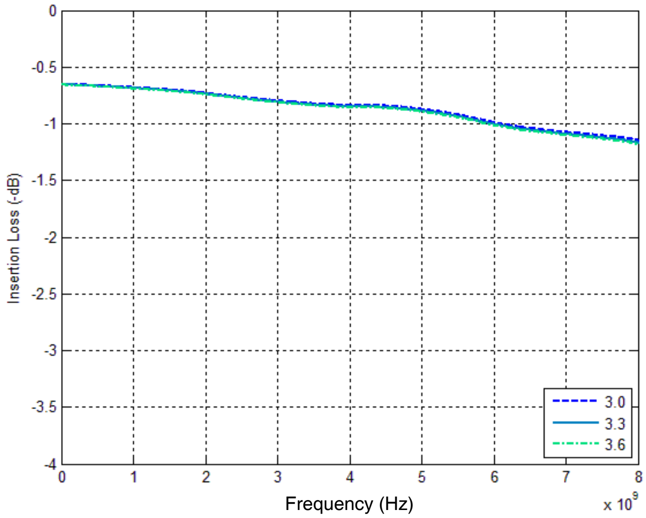


Figure 8. Insertion Loss vs. Temp (V_{DD} = 3.3V, Vss = 0)

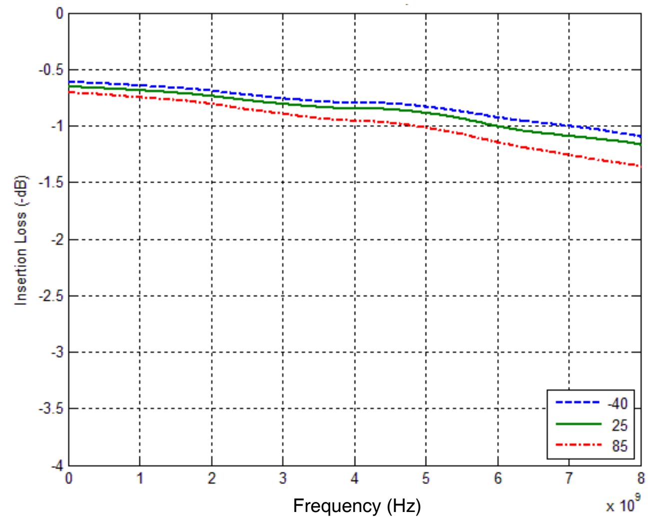


Figure 9. Insertion Loss (Temp = 25°C, V_{DD} = 3.3V, Vss = 0)

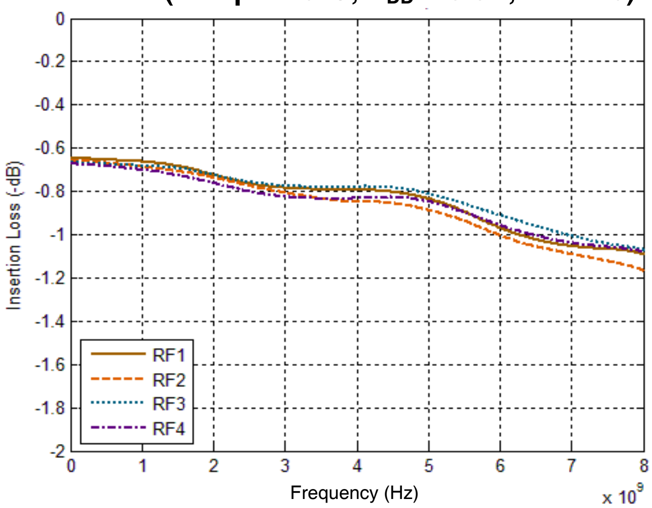


Figure 10. Isolation: RFX-RFX vs. V_{DD} (Temp = 25°C, Vss = 0)

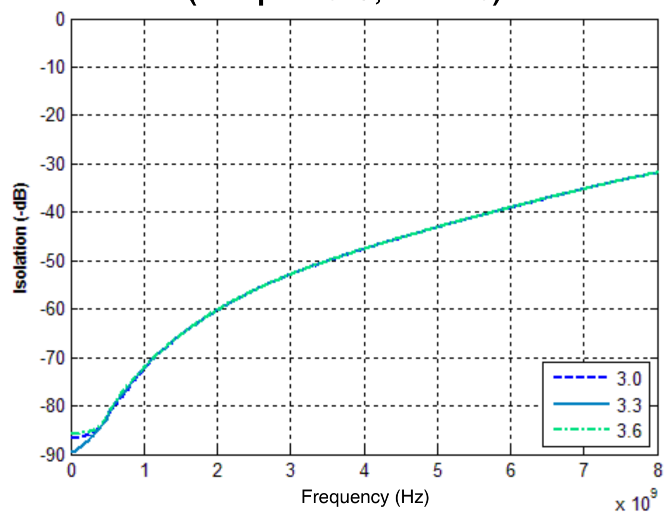


Figure 11. Isolation: RFX-RFX vs. Temp (V_{DD} = 3.3V, Vss = 0)

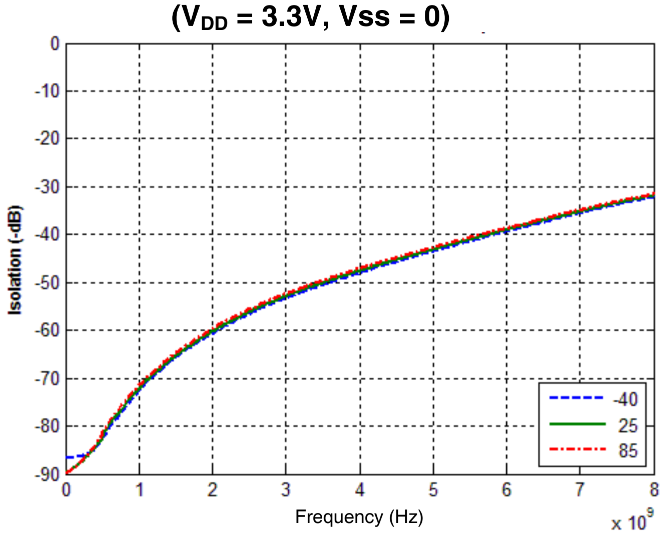


Figure 12. Isolation: RFX-RFC vs. V_{DD} (Temp = 25°C, Vss = 0)

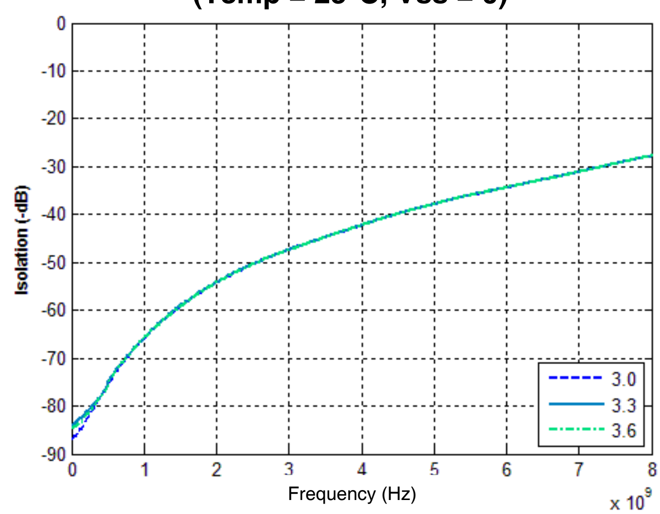


Figure 13. Isolation: RFX-RFC vs. Temp (V_{DD} = 3.3V, Vss = 0)

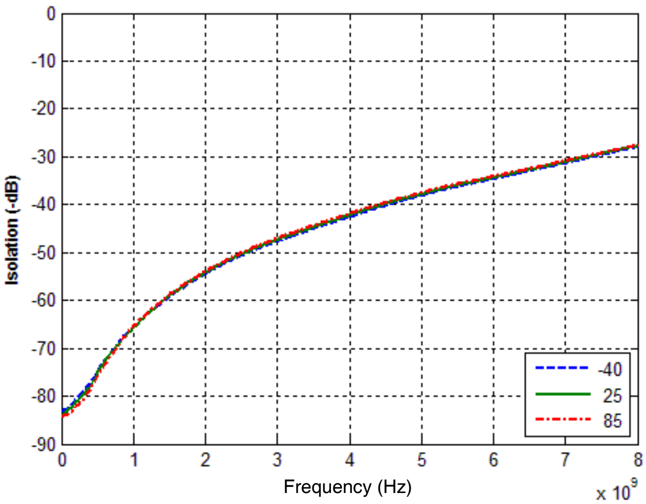


Figure 14. Active Port Return Loss vs. V_{DD} (Temp = 25°C, Vss = 0)

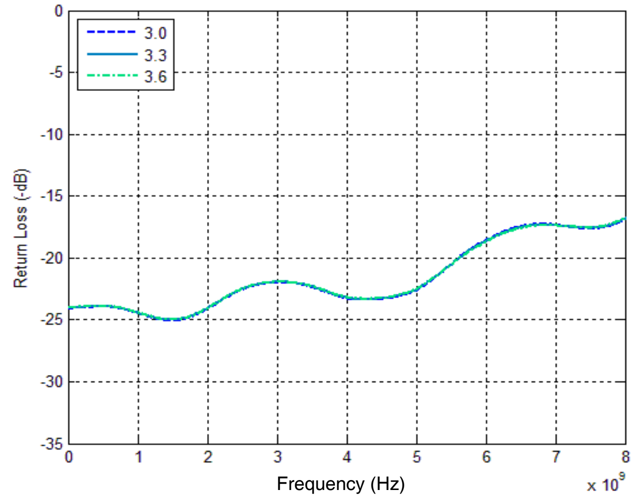


Figure 15. Active Port Return Loss vs. Temp (V_{DD} = 3.3V, Vss = 0)

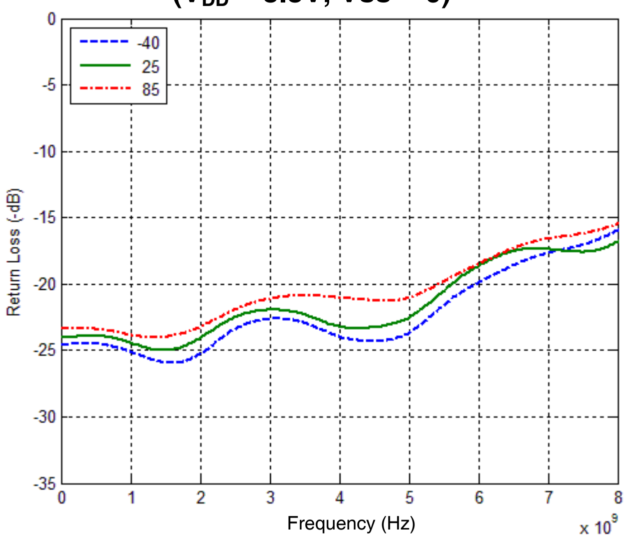


Figure 16. Terminated Port Return Loss vs. V_{DD} (Temp = 25°C, Vss = 0)

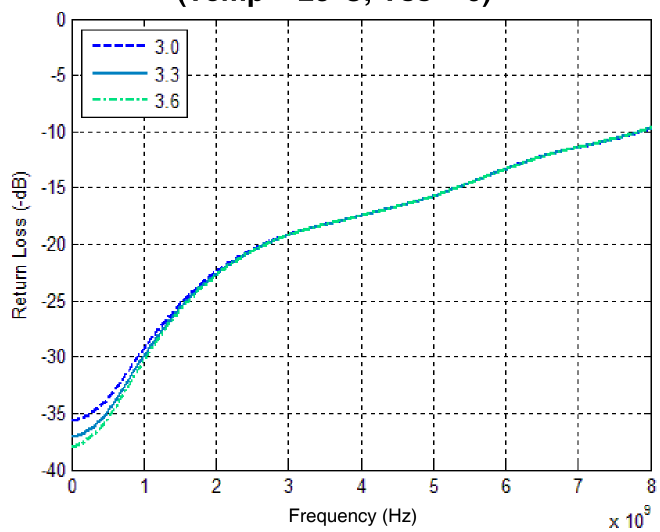


Figure 17. Terminated Port Return Loss vs. Temp (V_{DD} = 3.3V, Vss = 0)

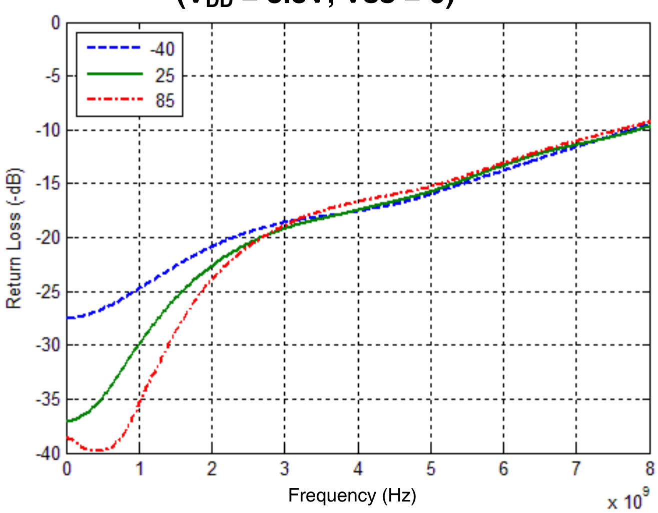


Figure 18. RFC Port Return Loss vs. V_{DD} (Temp = 25°C, Vss = 0)

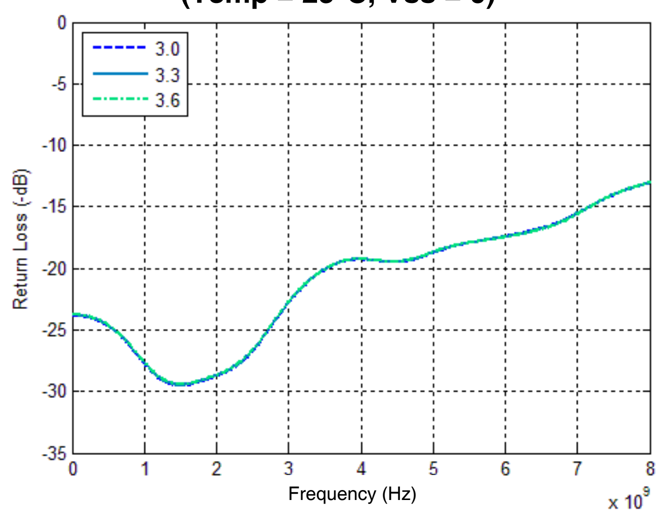


Figure 19. RFC Port Return Loss vs. Temp (V_{DD} = 3.3V, Vss = 0)

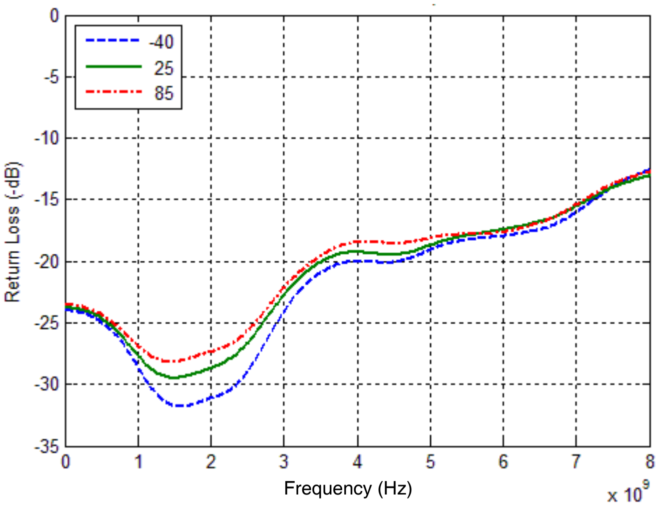
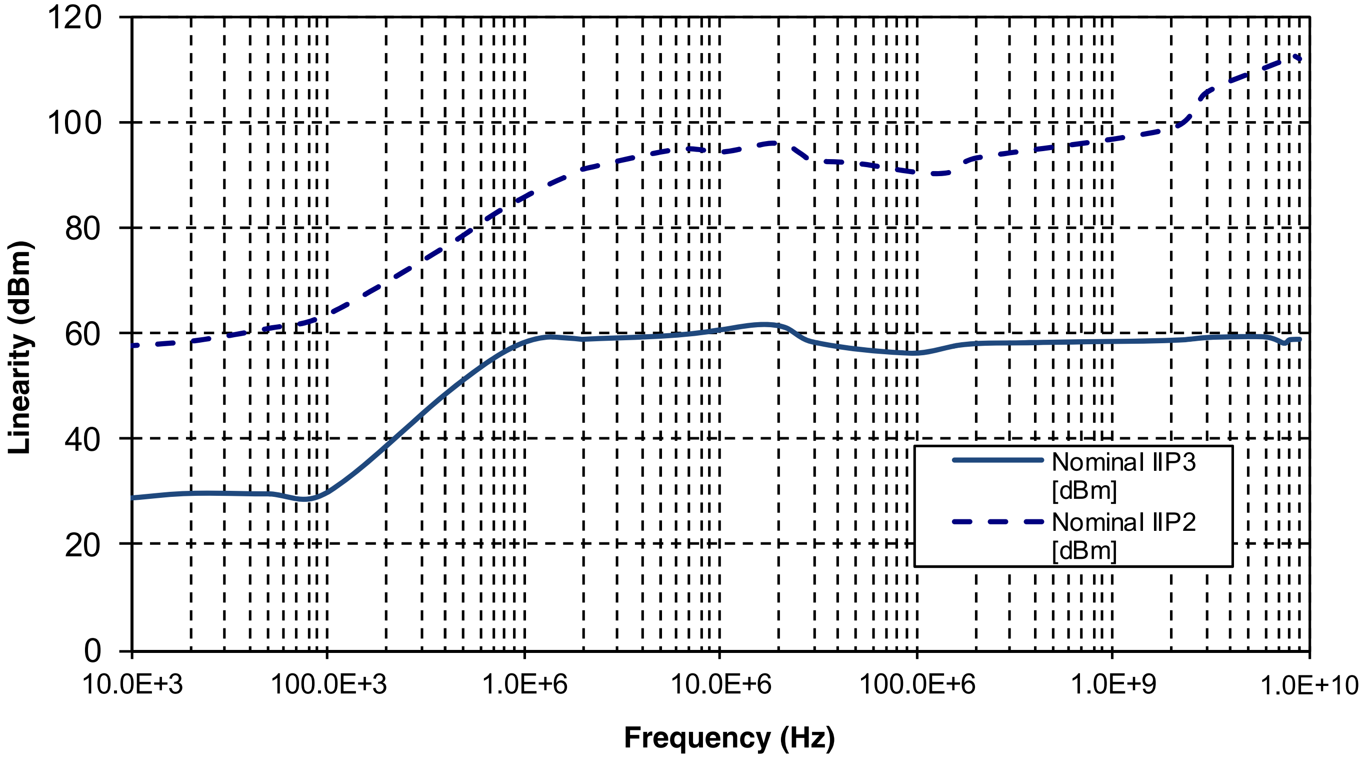


Figure 20. Linearity Performance (Temp = 25°C, V_{DD} = 3.3V, Vss = 0)

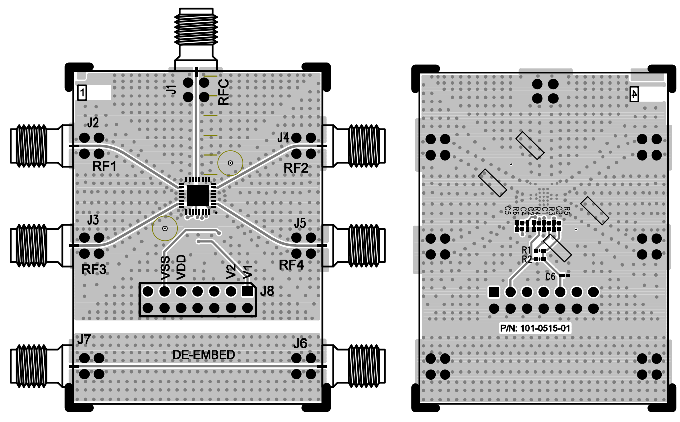


Evaluation Kit

The SP4T switch EK Board was designed to ease customer evaluation of Peregrine's PE42540. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via SMA connectors J2, J4, J3 and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

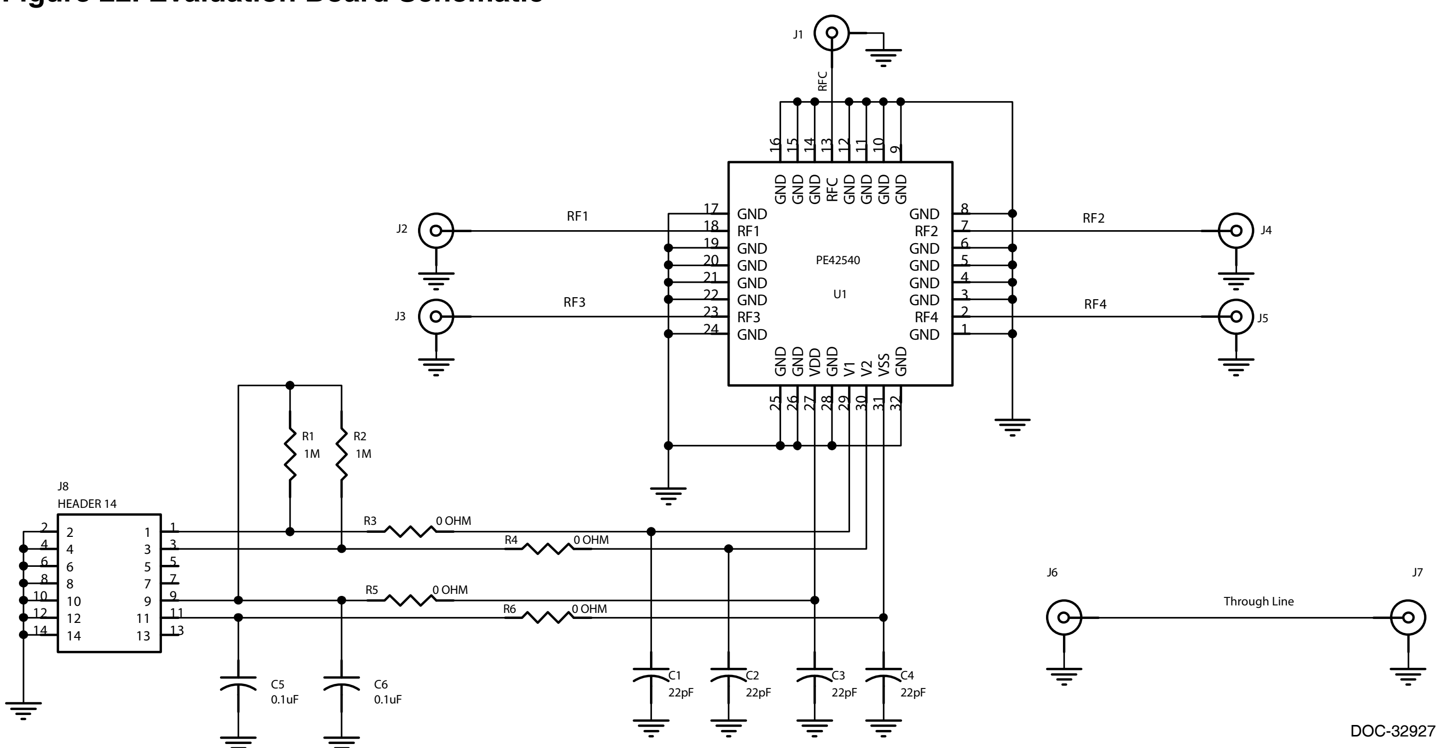
The board is constructed of a four metal layer material with a total thickness of 62 mils. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 15 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

Figure 21. Evaluation Board Layouts



PRT-28605

Figure 22. Evaluation Board Schematic



DOC-32927

Figure 23. Package Drawing

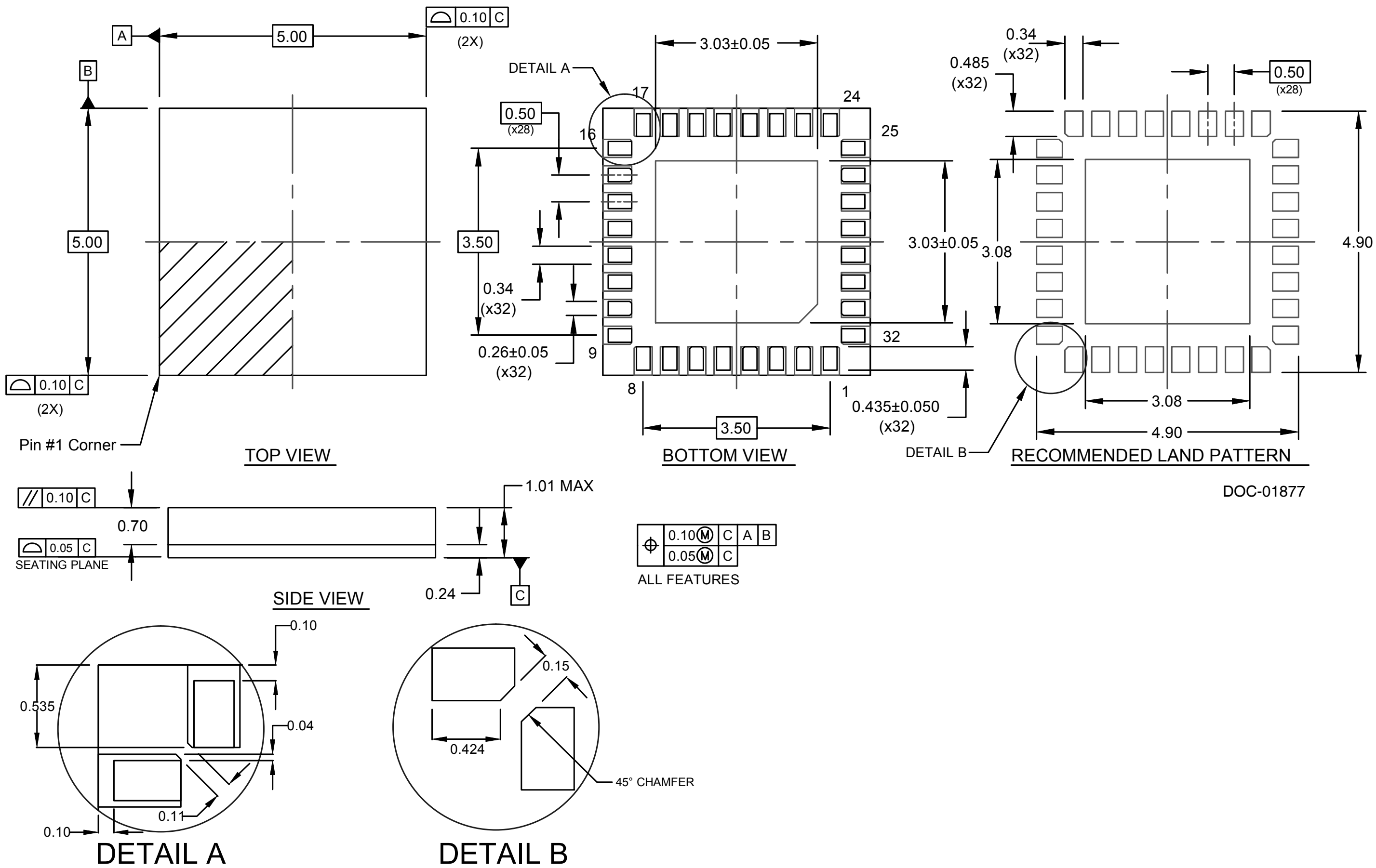
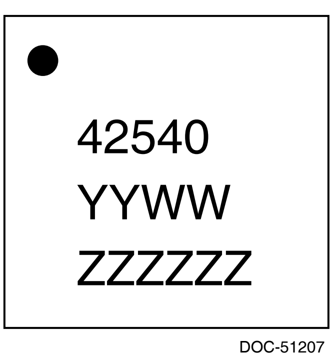


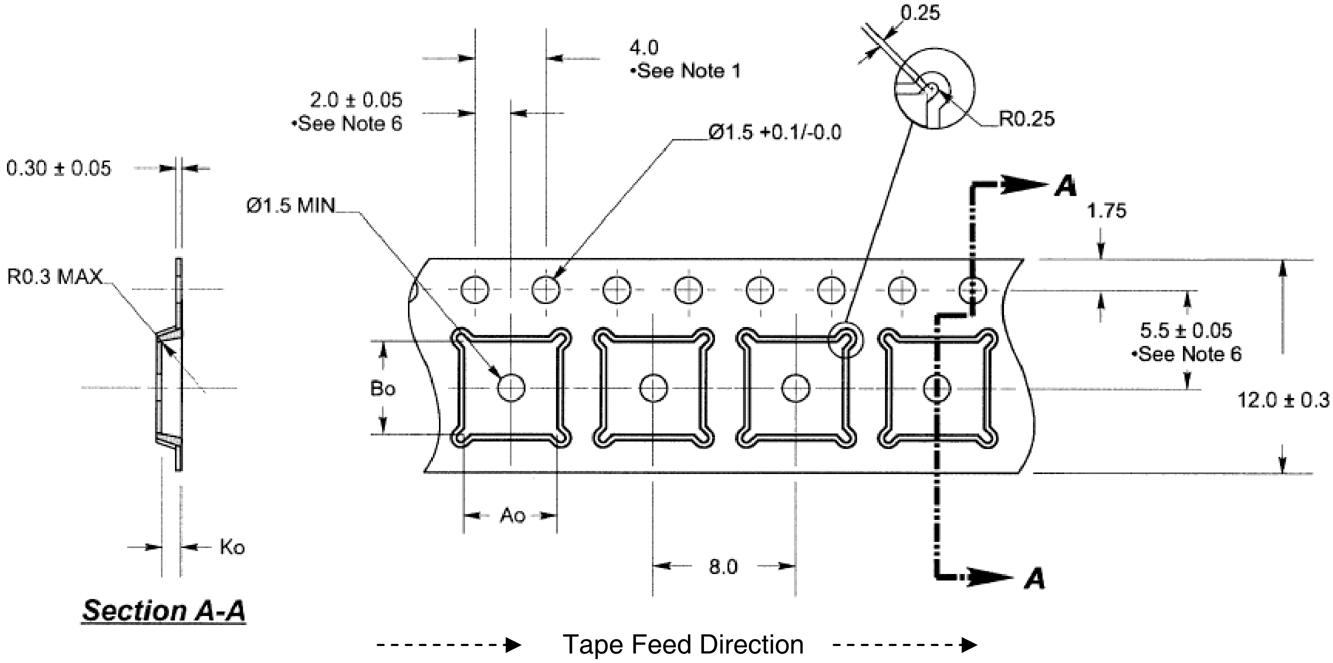
Figure 24. Marking Specifications



YYWW = Date Code

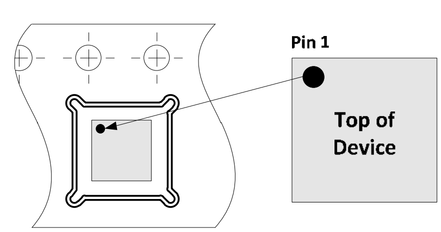
ZZZZZ = Last six digits of Lot Number

Figure 25. Tape and Reel Drawing



Notes: 1. 10 sprocket hole pitch cumulative tolerance ±0.02
2. Camber not to exceed 1 mm in 100 mm
3. Material: PS + C
4. Ao and Bo measured as indicated
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 5.25 ± 0.05 mm
Bo = 5.25 ± 0.05 mm
Ko = 1.1 ± 0.05 mm



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE42540LGBD-Z	PE42540 SP4T RF switch	Green 32-lead 5x5 mm LGA	3000 units / T&R
EK42540-04	PE42540 Evaluation kit	Evaluation kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.