High Speed CMOS 8-Bit Transceivers

QS54/74FCT245T
QS54/74FCT640T

QS54/74FCT2245T
QS54/74FCT2640T

FEATURES/BENEFITS

- Pin and function compatible to the 74F245/640 74FCT245/640 and 74FCT245T/640T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 245T, 640T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, C, and D speed grades; 3.8 ns tPD for D
- Iol = 64 mA Com., 48 mA Mil.

FCT-T 2245T, 2640T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades; 4.1 ns tPD for C
- Iol = 12mA Com.

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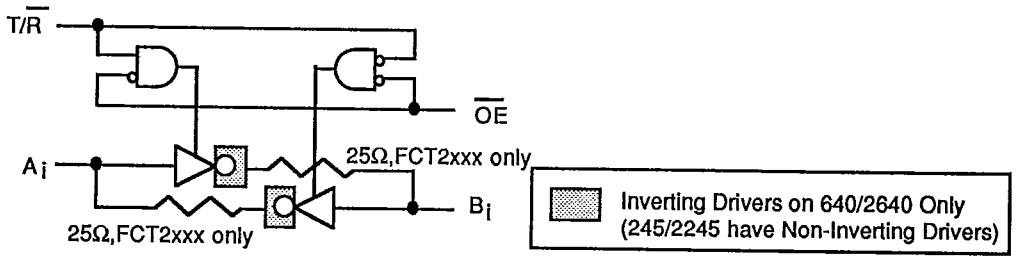
DESCRIPTION

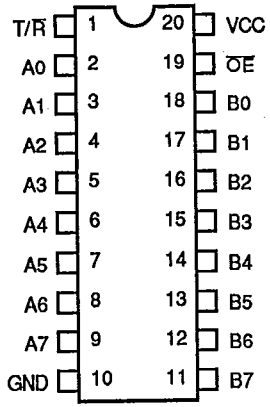
The QSFCT245AT/CT and QSFCT2245AT/CT are 8-bit non-inverting transceivers that have three-state outputs which are useful for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow, either from A to B or B to A, and the Output Enable ($\overline{OE}$) input enables the selected port for output. The FCT2245AT/CT and FCT2640AT/CT are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2245 parts can replace the 245 series to reduce noise in an existing design. All inputs have clamp diode for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

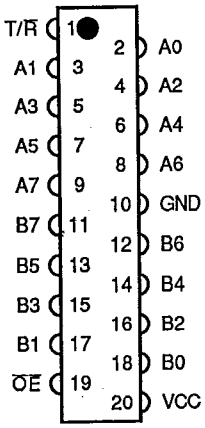


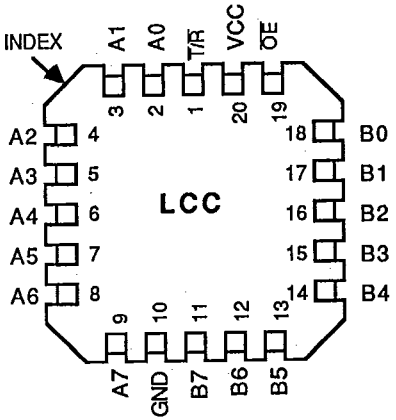
PINOUTS

PDIP, SOIC, QSOP



ZIP





ALL PINS TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
Ai	I/O	Data Bus A
Bi	I/O	Data Bus B
T/$\overline{R}$	I	Direction
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

$\overline{OE}$	T/$\overline{R}$	A	B	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	Output	Input	Bus B to Bus A
L	H	Input	Output	Bus A to Bus B

H=High, L=Low, Hi-Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,19	4	4	5	7	pF
-------	6	6	7	9	pF
2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX (25Ω)	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: Ta = 0 °C to 70 °C, Vcc = 5.0V ±5% Military: Ta = -55 °C to +125 °C, Vcc = 5.0V ±10%
Cload = 50 pF, Rload = 500Ω unlesss otherwise noted.

Symbol	Description		Notes (1)	245, 640, 2245, 2640		245A, 640A, 2245A, 2640A		245C, 2245C		245D		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
tPHL tPLH	Propagation Delay Ai to/from Bi, 245,640	COM		1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	ns
		MIL		1.5	7.5	1.5	4.9					
	Propagation Delay Ai to/from Bi, 2245,2640	COM		1.5	7	1.5	4.6	1.5	4.1			
		MIL		1.5	7.5	1.5	4.9					
tPZH tPZL	Output Enable Time $\overline{OE}$, T/$\overline{R}$ to A/B, 245,640	COM		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.6	
		MIL		1.5	10	1.5	6.5					
	Output Enable Time $\overline{OE}$, T/$\overline{R}$ to A/B, 2245,2640	COM		1.5	9.5	1.5	6.2	1.5	5.8			
		MIL		1.5	10	1.5	6.5					
tPHZ tPLZ	Output Disable Time $\overline{OE}$, T/$\overline{R}$ to A/B	COM	2	1.5	7.5	1.5	5	1.5	4.5	1.5	4.5	
		MIL	2	1.5	10	1.5	6					

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.