

MOSFET – N-Channel, POWERTRENCH®

150 V, 169 A, 6.3 mΩ

FDBL86210-F085

Features

- Typical $r_{DS(on)} = 5\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Typical $Q_{g(tot)} = 70\text{ nC}$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous ($V_{GS} = 10$), $T_C = 25^\circ\text{C}$ (Note 1)	169	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	502	mJ
P_D	Power Dissipation	500	W
	Derate Above 25°C	3.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

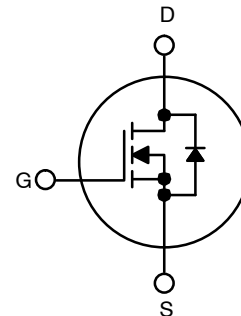
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.24\text{ mH}$, $I_{AS} = 64\text{ A}$, $V_{DD} = 100\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

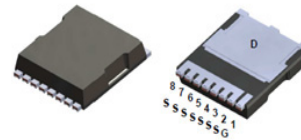


ON Semiconductor®

www.onsemi.com

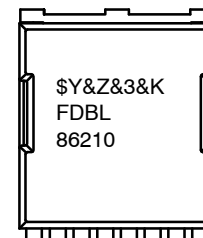


N-Channel



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



$\$Y$ = ON Semiconductor Logo
 $\&Z$ = Assembly Plant Code
 $\&3$ = Numeric Date Code
 $\&K$ = Lot Code
 FDBL86210 = Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping†
FDBL86210-F085	FDBL86210	H-PSOF8L	2000 Units/ Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDBL86210-F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	150	–	–	V	
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 150 V, V _{GS} = 0 V	T _J = 25°C	–	–	1	μA
			T _J = 175°C (Note 4)	–	–	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA	

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.8	4.0	V	
r _{DS(on)}	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 10 V	T _J = 25°C	–	5	6.3	mΩ
			T _J = 175°C (Note 4)	–	14	17.5	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	–	5805	–	pF
C _{oss}	Output Capacitance		–	536	–	pF
C _{rss}	Reverse Transfer Capacitance		–	16	–	pF
R _g	Gate Resistance	f = 1 MHz	–	2.2	–	Ω
Q _{g(toT)}	Total Gate Charge at 10 V	V _{GS} = 0 to 10 V V _{DD} = 75 V, I _D = 80 A	–	70	90	nC
Q _{g(th)}	Threshold Gate Charge		V _{GS} = 0 to 2 V	–	10.5	13
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 75 V, I _D = 80 A	–	32.5	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	10	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 75 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	–	80	ns
t _{d(on)}	Turn-On Delay Time		–	39	–	ns
t _r	Rise Time		–	30	–	ns
t _{d(off)}	Turn-Off Delay Time		–	70	–	ns
t _f	Fall Time		–	23	–	ns
t _{off}	Turn-Off Time		–	–	130	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V	–	–	1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V	–	–	1.2	V
T _{rr}	Reverse Recovery Time	I _F = 80 A, dI _{SD} /dt = 100 A/μs, V _{DD} = 120 V	–	108	125	ns
Q _{rr}	Reverse Recovery Charge		–	323	467	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

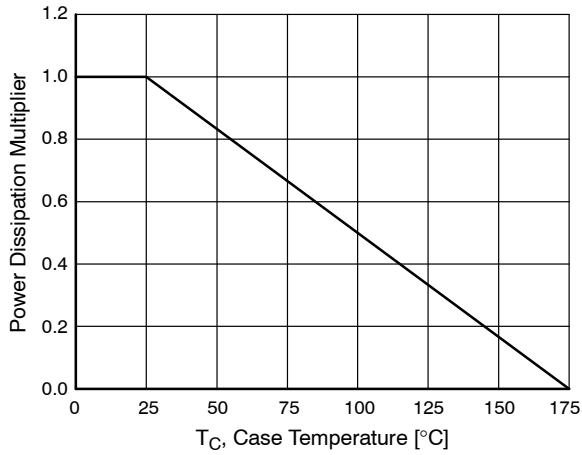


Figure 1. Normalized Power Dissipation vs. Case Temperature

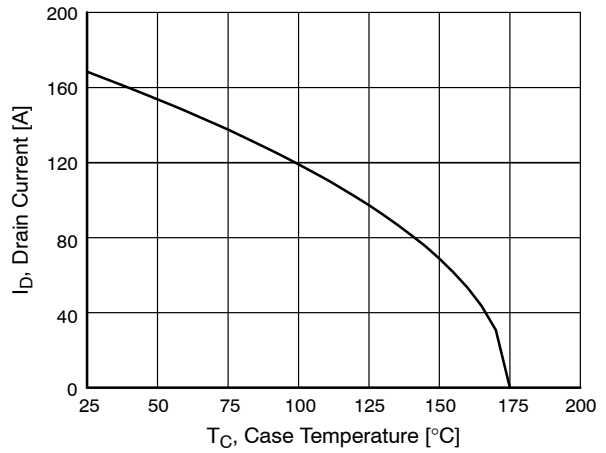


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

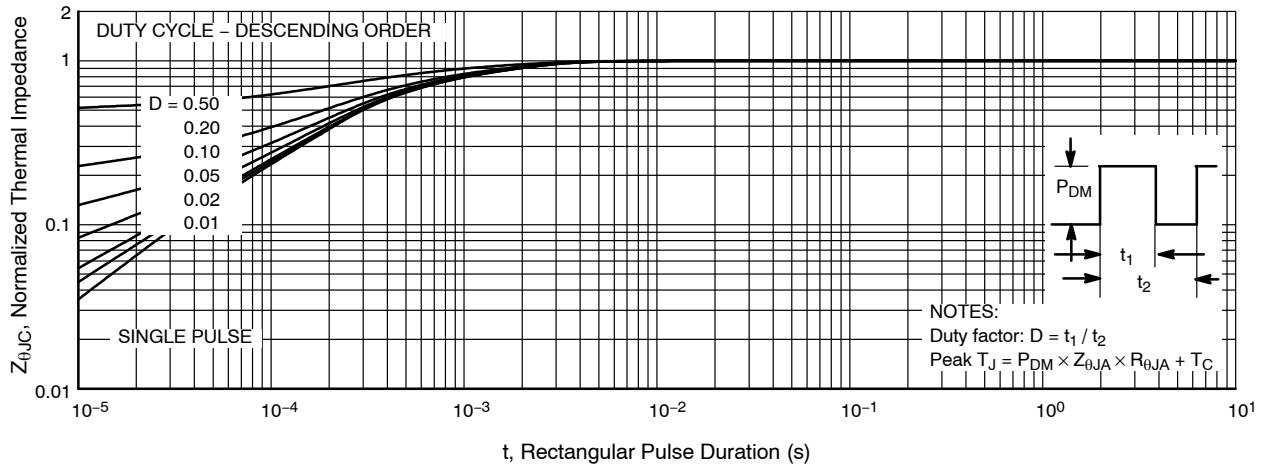


Figure 3. Normalized Maximum Transient Thermal Impedance

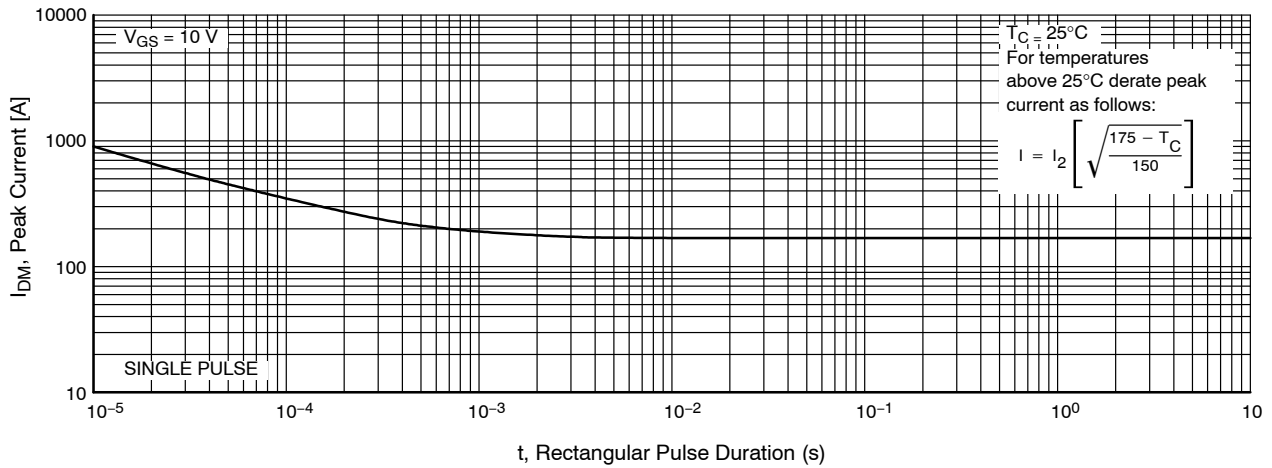


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

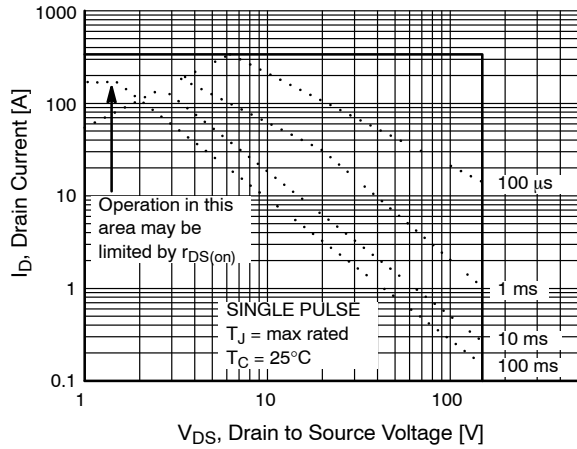
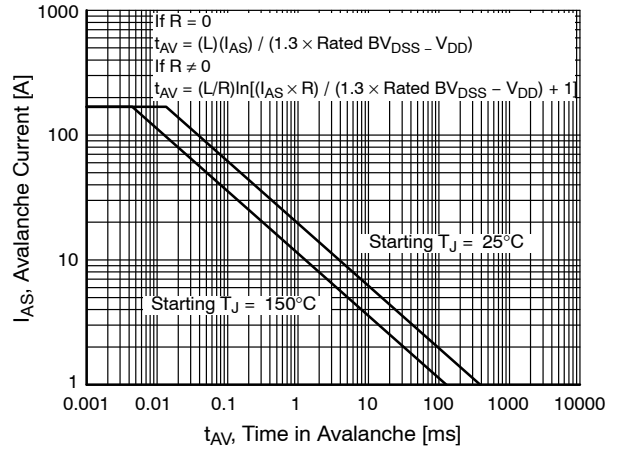


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes [AN7514](#) and [AN7515](#).

Figure 6. Unclamped Inductive Switching Capability

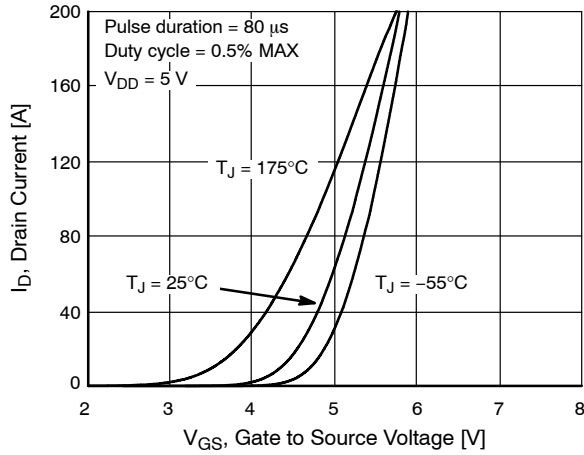


Figure 7. Transfer Characteristics

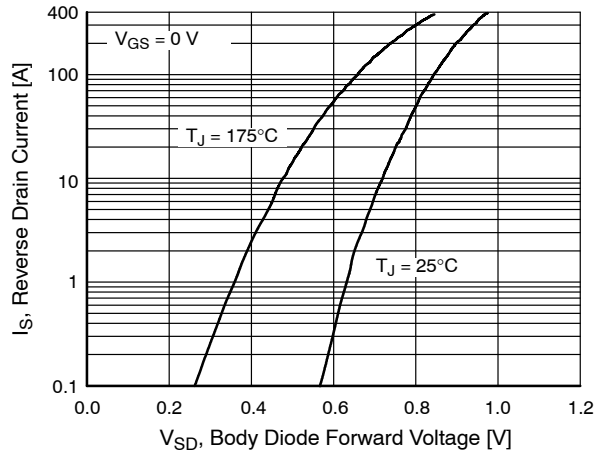


Figure 8. Forward Diode Characteristics

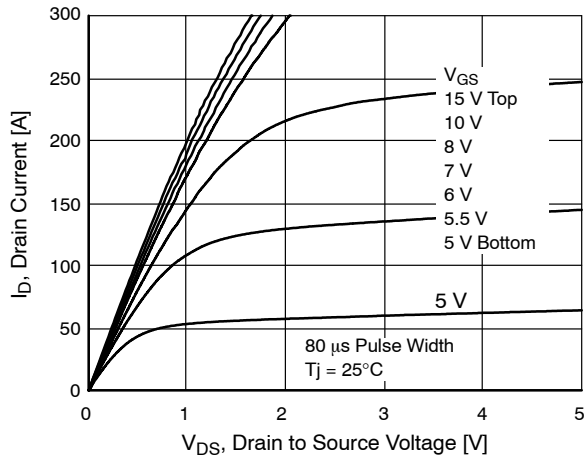


Figure 9. Saturation Characteristics

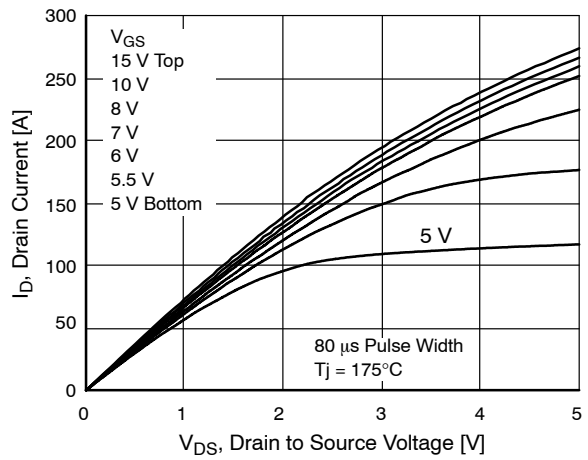


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

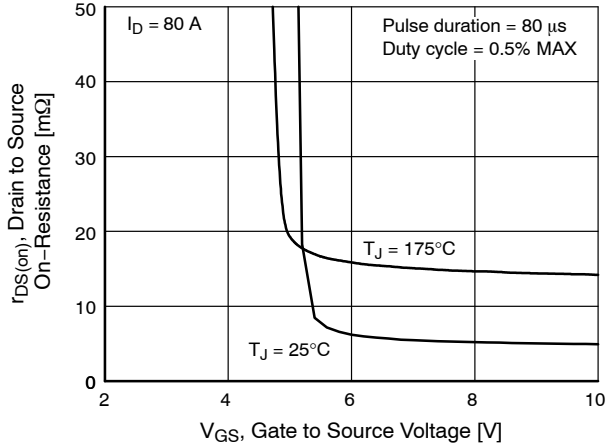


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

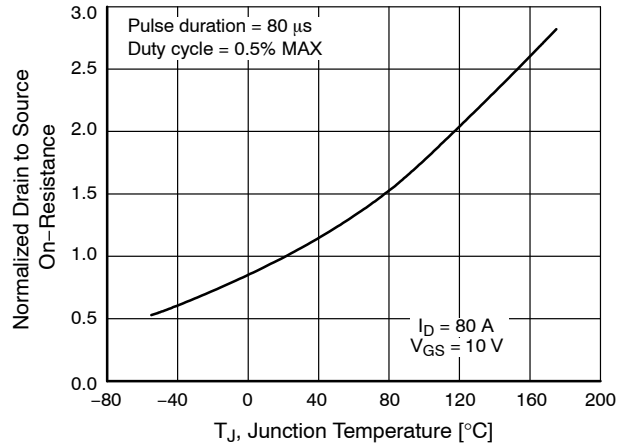


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

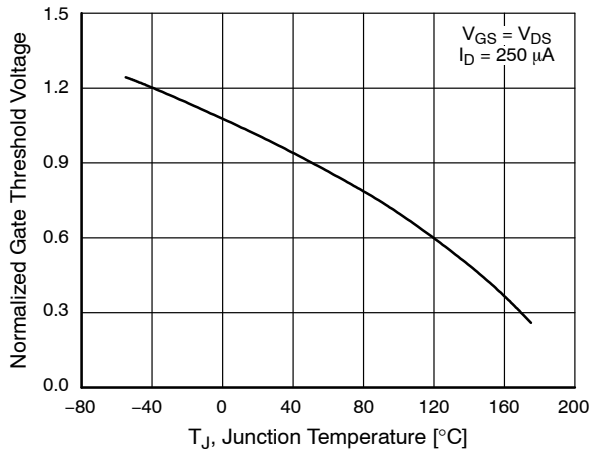


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

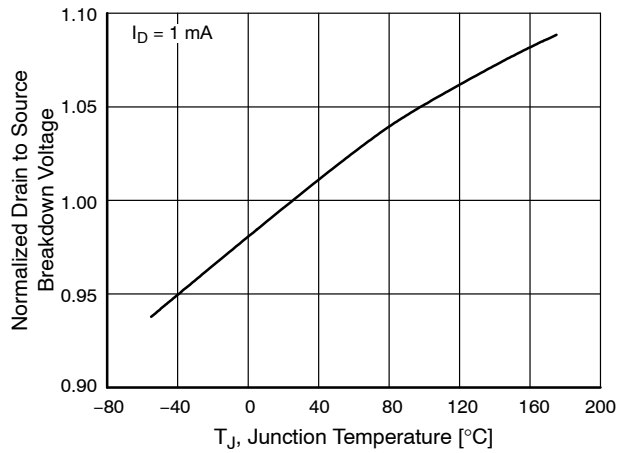


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

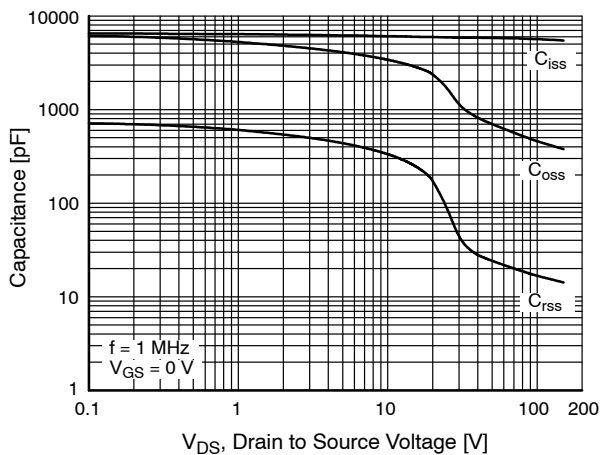


Figure 15. Capacitance vs. Drain to Source Voltage

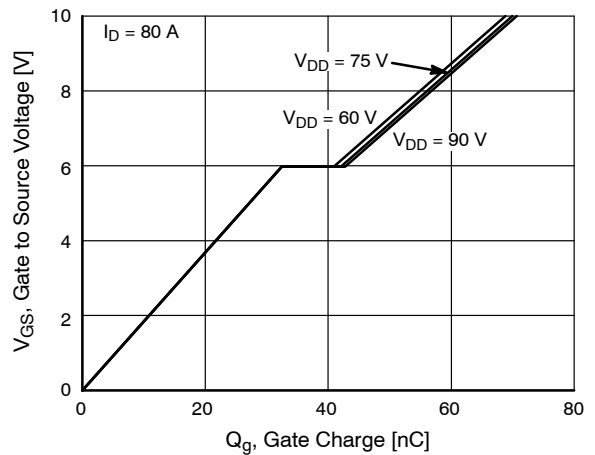


Figure 16. Gate Charge vs. Gate to Source Voltage

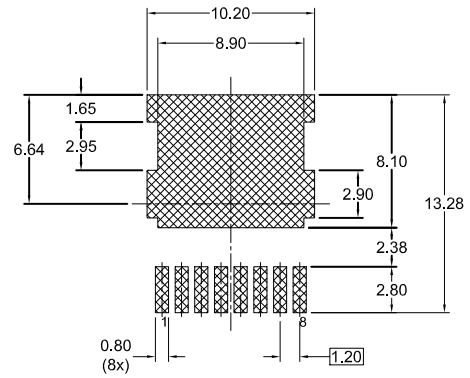
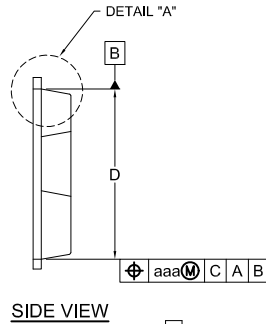
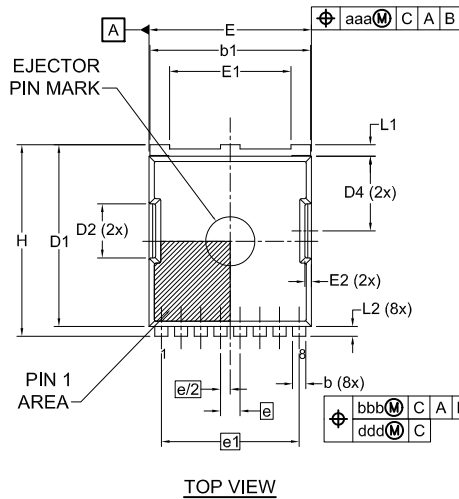
POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



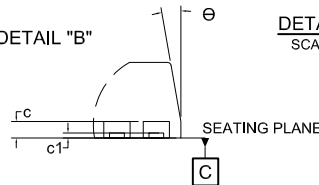
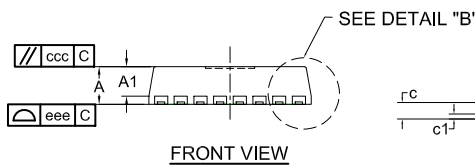
H-PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

DATE 22 MAY 2023



LAND PATTERN RECOMMENDATION

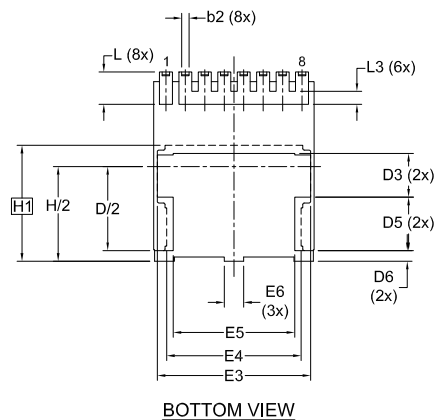
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL "A"
SCALE: 2X

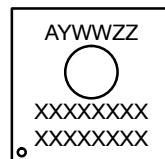
NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL "B"
SCALE: 2X

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13813G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	H-PSOF8L 11.68x9.80	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales