ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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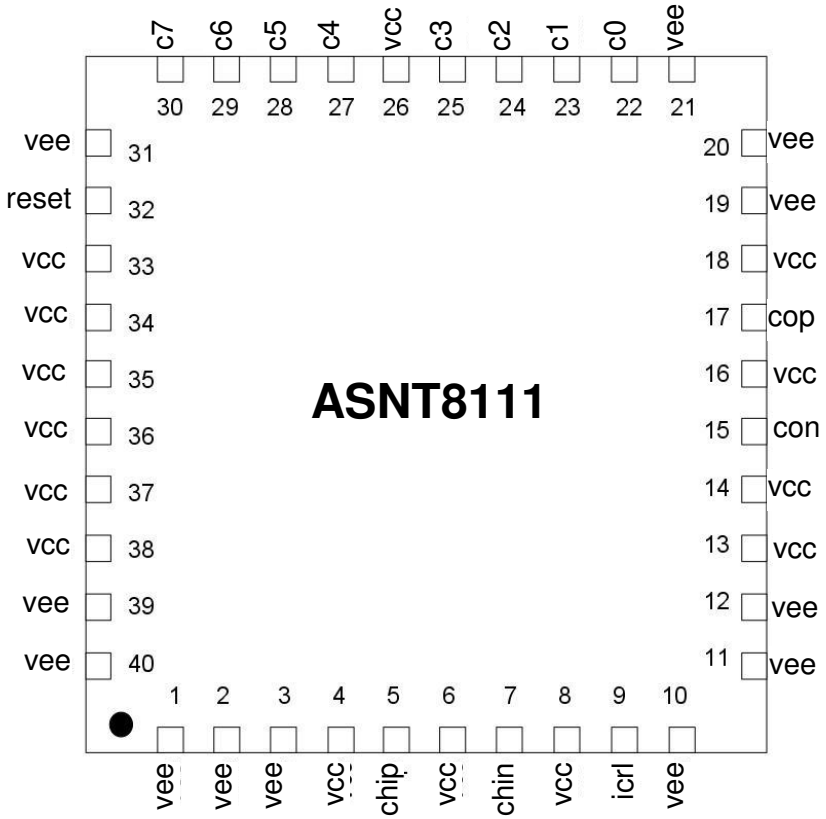
ASNT8111-PQB
DC-to-24*GHz* Programmable Integer Divider

- Wide frequency range from DC to 24*GHz*
- Continuous division ratios from 1 to 256
- 50% duty cycle of the output divided clock signal
- Fully differential CML input and output interfaces
- Adjustable power consumption
- Easy 8-bit parallel programming interface compatible with CMOS/LVTTL standards
- Optional external reset function
- Dynamic division ratio adjustment with a short set-up time (about 20*ns* after the pulse edge on any control input)
- Single +2.8*V* or -2.8*V* power supply
- Industrial temperature range
- Standard 40-pin QFN package with a thermal pad



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DESCRIPTION

ASNT8111-PQB is a high-speed programmable integer clock divider with dynamic adjustment of the division ratio through a standard 8-bit parallel LVTTL/CMOS interface and optional external active-high CMOS/LVTTL reset signal. The functional block diagram of the device is shown in Fig. 1.

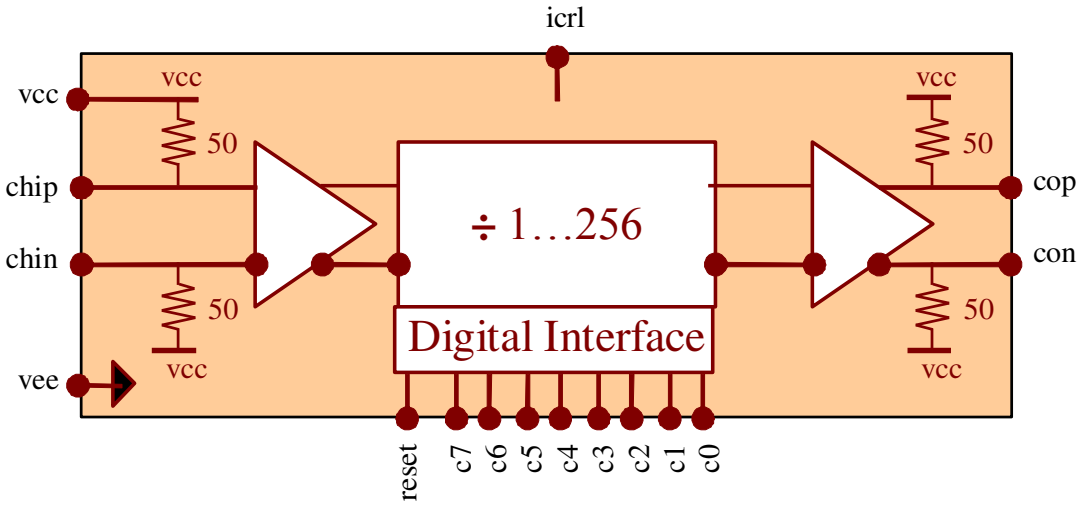

Fig. 1. Functional Block Diagram

The divider accepts an input clock signal chip/chin with a speed from DC to the maximum specified frequency and provides a clean 50% duty cycle output divided clock signal cop/con in any operational mode. The divider allows for dynamic adjustment of the division ratio from 1 to 256 with a step of 1. A binary code on the control inputs c0-c7 defines the value of the ratio from 1 to 255, where c7 is the most significant bit. All "0"s ("low" state) define the division by 256. Following any change of any control signal, the divider switches to idle after (64...128) periods of the high-speed system clock plus an additional 1.6*ns* delay, and returns back to normal operation with the new division ratio after an additional delay equal to 192 periods of the high-speed system clock.

The device automatically resets itself after the initial power-up and any change of the division control signals. When the optional external reset signal reset is set to "high", the divider switches to idle (static "0" output) after a 0.7*ns* delay as shown in the timing diagram in Fig. 2. When reset returns to "low", the divider switches back to normal operation after (64...128) periods of the high-speed system clock plus an additional 1.6*ns* of delay. The minimum allowed reset pulse must be longer than 64 periods of the high-speed system clock.

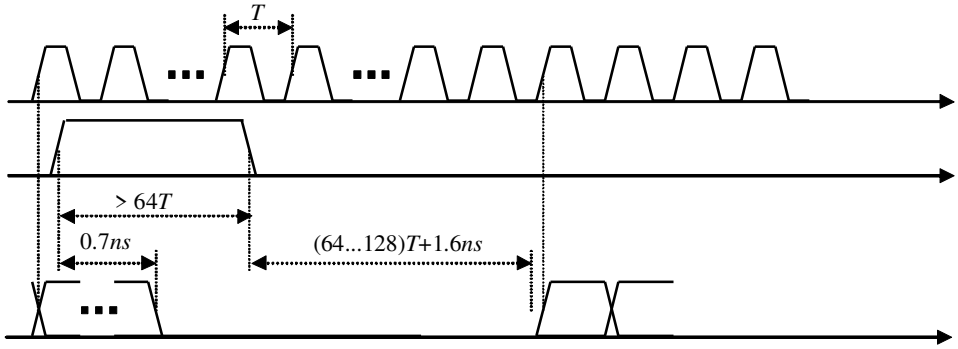

Fig. 2. Timing Diagram

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc=0.0*V*=ground), or a positive supply (vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

The parts power consumption may be reduce by up to 25% using an external resistor to connect the control port icrl to vee. Please be aware that reduced current may result in lower maximum frequency!

All the characteristics detailed below assume vcc = +2.8*V* and vee = 0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.3	*V*
Power Consumption		3.2	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
chip	5	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc
chin	7		
cop	17	CML output	Differential divided clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
con	15		
Low-Speed I/Os			
reset	32	CMOS input	External reset signal
Digital Controls			
c0	22	CMOS input	Digital division control signals
c1	23		
c2	24		
c3	25		
c4	27		
c5	28		
c6	29		
c7	30		
Analog Controls			
icrl	9	Input	Power control port; requires external resistor connected to vee or external power supply with current sinking capability

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply or ground	4, 6, 8, 13, 14, 16, 18, 26, 33, 34, 35, 36, 37, 38
vee	Negative power supply or ground	1, 2, 3, 10, 11, 12, 19, 20, 21, 31, 39, 40

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	2.5	2.8	3.0	*V*	
*I*vee	810			*mA*	icrl shorted to vee
			1050	*mA*	R>6*KOhm* between icrl and vee
Power consumption	2.03			*W*	icrl shorted to vee
			3.15	*W*	R>6*KOhm* between icrl and vee
Junction temperature	-25	50	125	*°C*	
Input (chip/chin)					
Frequency	0.0		24	*GHz*	
Swing	60	400	1000	*mV*	Differential or SE, p-p; at 6*GHz*
CM Level	vcc- (SE swing)/2				
Rise/Fall Times			3	*ns*	20%-80%
Output (cop/con)					
Frequency	0.0		24	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall Times	15	17	19	*ps*	20%-80%
Additive Jitter		TBD		*ps*	Peak-to-Peak
Duty Cycle	47%	50%	53%		For clock signal
Select (c0-c7) & Reset (reset)					
Logic "1" level	V_{CC}-0.4			*V*	
Logic "0" level			V_{EE}+0.4	*V*	

PACKAGE INFORMATION

The chip is packaged in a standard 40-pin QFN package shown Fig. 3. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part's identification label is ASNT8111-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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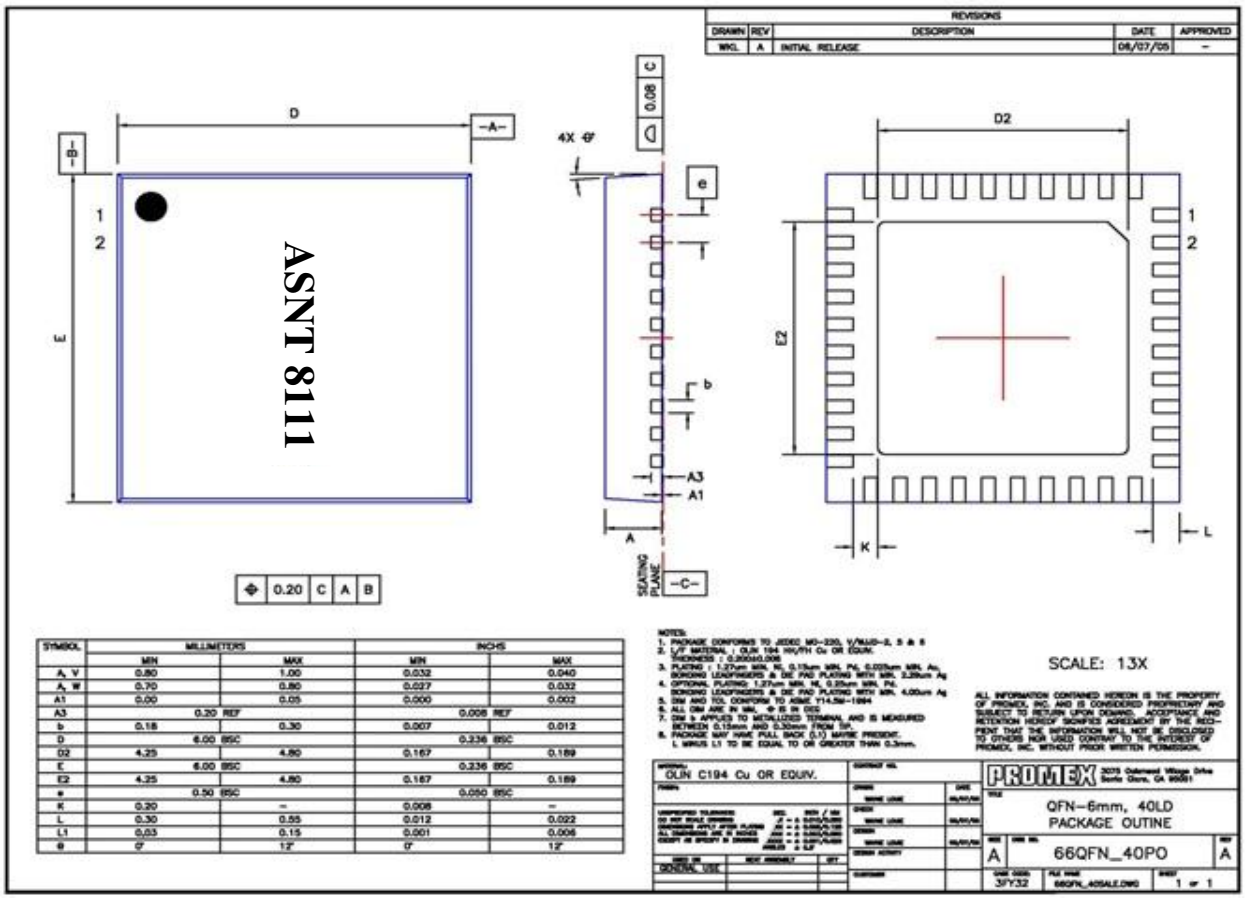

Fig. 3. QFN 40-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.1.2	02-2020	Updated Package Information
1.0.2	10-2019	First release