CUI INC®

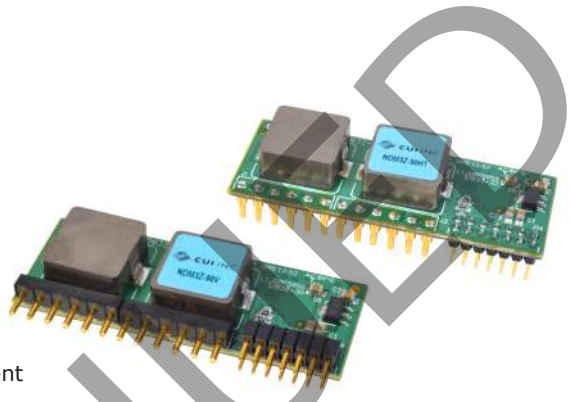
MODEL: NDM3Z-90 | **DESCRIPTION**: AUTO COMPENSATED, DIGITAL DC-DC POL CONVERTER

GENERAL CHARACTERISTICS

- 7.5~14 V input range
- 0.6~1.8 V programmable output
- high efficiency
- voltage tracking
- voltage margining
- active current sharing
- *Snapshot*™ parametric capture
- voltage/current/temperature monitoring
- synchronization and phase spreading
- remote differential voltage sense
- programmable soft start and soft stop
- fault management

FEATURES

- compact package
  vertical:
  50.8 x 9.51 x 19.05 mm
  (2.0 x 0.37 x 0.75 in)
  horizontal:
  50.8 x 19.05 x 10.0 mm
  (2.0 x 0.75 x 0.39 in)
- 90 A output
- adaptive algorithms
- cycle-by-cycle charge management
- dual phase architecture
- SMBus interface
- PMBus™ compatible



RoHS PMBus AMP Architects of Modern Power

MODEL

MODEL	input voltage (Vdc)	output voltage (Vdc)	output current max (A)	output wattage max (W)
NDM3Z-90	7.5~14	0.6~1.8	90	162

PART NUMBER KEY

NDM3Z-90 X - X - XXX

Base Number

Module Orientation and Pin Style:
HT = horizontal, through hole mount
HS = horizontal, surface mount
V = vertical

Pin Configuration:
A = HT 3.56 mm pin length (HT)
V 4 mm pin length (V)
B = V 5.5 mm pin length (V)
S = surface mount pins

Firmware Configuration:
000~ZZZ

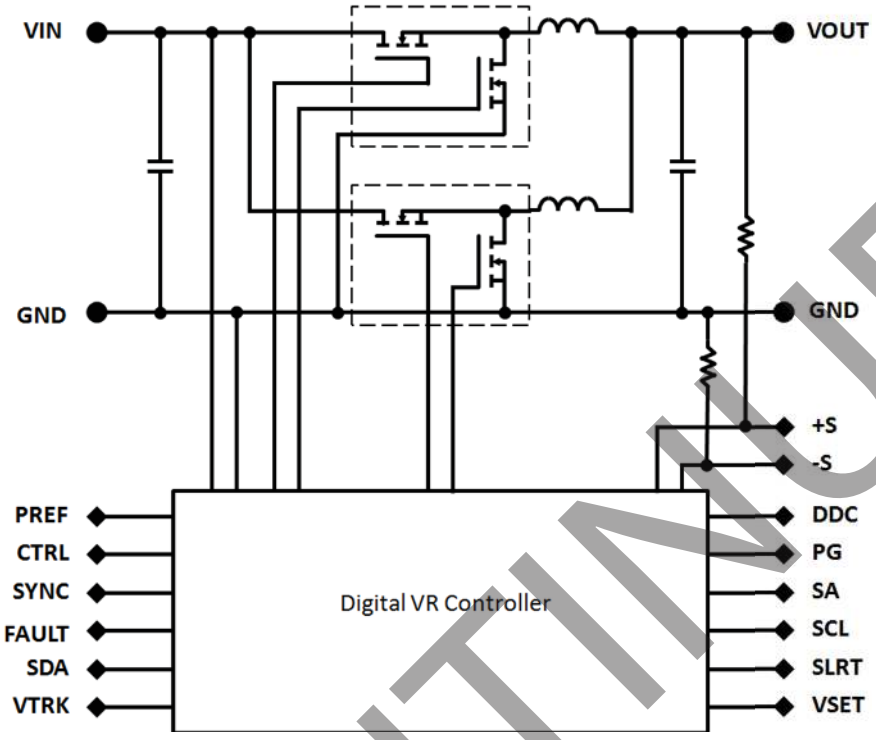
Example part number: **NDM3Z-90V-A-002**

vertical module
4.0 mm pin length
firmware configuration 002

* HS and HT modules are delivered on tape and reel
* V modules are delivered in trays

CONTENTS

INTERNAL CIRCUIT DIAGRAM



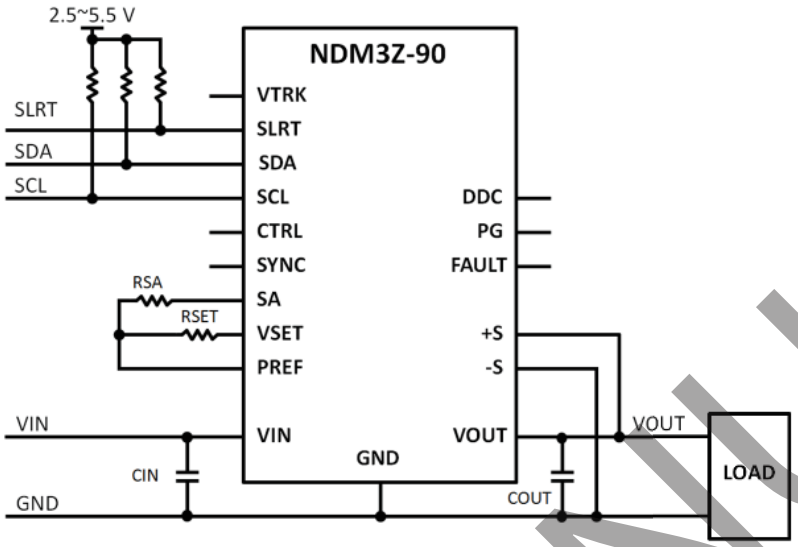
POWER CONNECTIONS

symbol	pin	IO type	description
VIN	1A, 1B, 1C, 1D	Power	Input voltage
GND	2A, 2B, 2C, 2D	Ground	Power ground
VOUT	3A, 3B, 3C, 3D	Power	Output voltage
N/C	11, 12	N/A	No connect on module

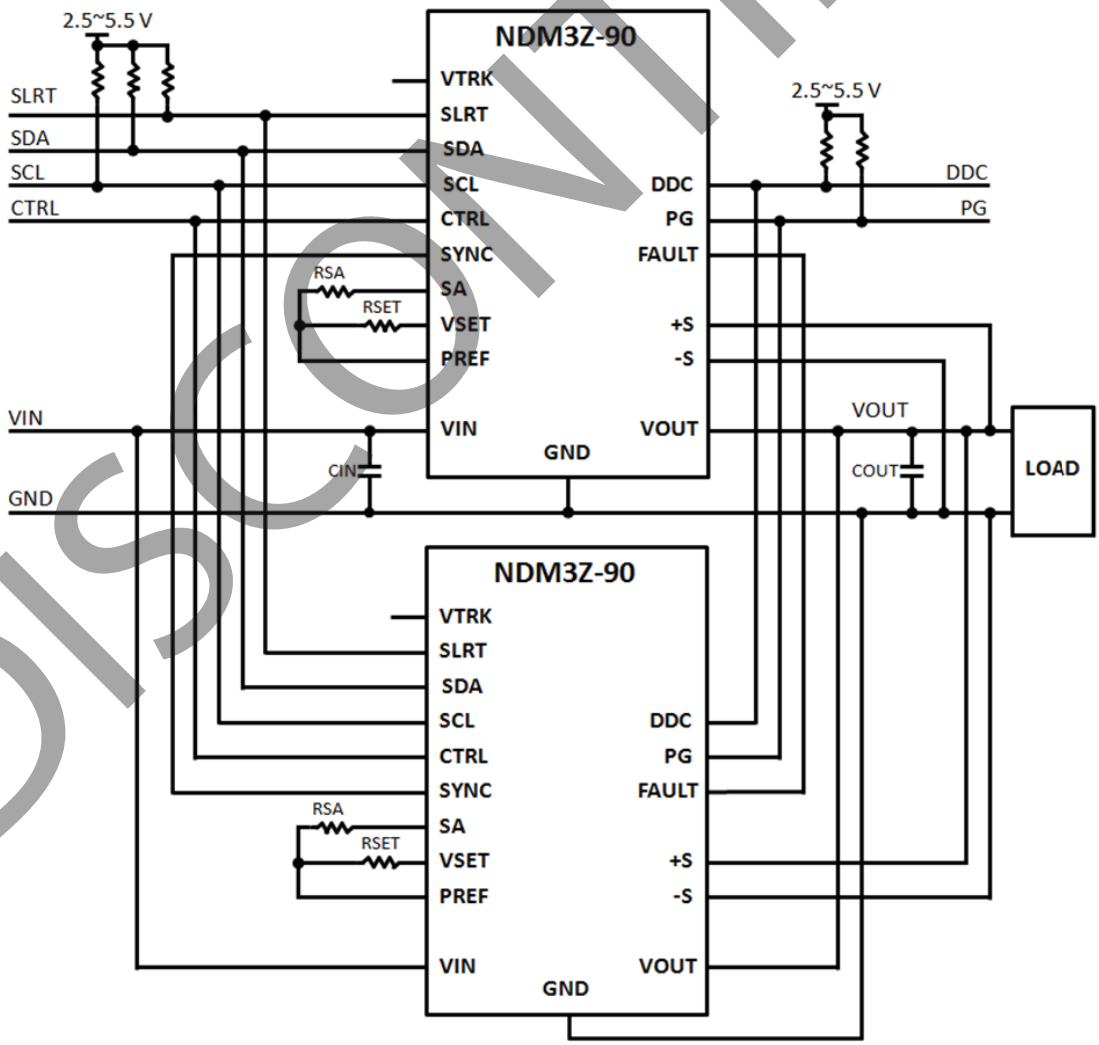
COMMUNICATION CONNECTIONS

symbol	pin	IO type	description
+S	4A	Analog	Output voltage positive sense input, N/C if not used
-S	4B	Analog	Output voltage negative sense input, N/C if not used
VSET	5A	Digital	Output voltage pin-strap
VTRK	5B	Analog	Voltage tracking input, N/C if not used
SLRT	6A	Digital	SMBus alert, N/C if not used
SDA	6B	Digital	SMBus data, pull-up resistor required even if not used
SCL	7A	Digital	SMBus clock, pull-up resistor required even if not used
FAULT	7B	Digital	Module fault indicator, N/C if module is stand-alone, tied together if modules are current share configured
SA	8A	Digital	SMBus address pinstrap
SYNC	8B	Digital	Synchronization I/O, N/C if not used
PG	9A	Digital	Power good, pull-up resistor or configured as push-pull
CTRL	9B	Digital	Remote control or enable, N/C if not used, internal pull-up resistor
DDC	10A	Digital	Digital-DC Communications bus, pull-up resistor or configured as push-pull (stand-alone only) required
PREF	10B	Ground	Pin-strap ground

TYPICAL APPLICATION CIRCUIT



TYPICAL APPLICATION CIRCUIT - PARALLEL OPERATION



ABSOLUTE MAXIMUM RATINGS

parameter	conditions/description	min	typ	max	units
V_{in}	input voltage	-0.3		16	V
digital pin voltage	CTRL, DDC, SA, SLRT, SDA, SCL, SYNC, VSET, PG, FAULT	-0.3		6.0	V
analog pin voltage	+S, V_O, VTRK	-0.3		6.5	V
ground voltage differential	GND, PREF, -S	-0.3		0.3	V
operating temperature	T_{P1}	-40		150	°C
storage temperature		-40		150	°C

Notes: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied.

Configuration File

The digital control circuit in this module uses a configuration file which determines the functionality and performance of the product. The Standard configuration is designed to fit most application needs and the Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. Changes in Standard configuration might be required to optimize performance in specific applications. Changes to the Standard configuration are required for current sharing operation.

PRODUCT ELECTRICAL SPECIFICATION

T_{P1} = -30 to +95 °C, V_I = 7.5 to 14 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin strap. Standard configuration.
External C_{IN} = 1000 µF/12 mΩ + 24 x 10 µF, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF. See Operating Information section for selection of capacitor types.
Sense pins are connected to load.

parameter	conditions/description		min	typ	max	units
input voltage (V_I)			7.5		14	V
input voltage rise time (V_I)	monotonic				6	V/ms
output voltage without pin-strap (V_O)				1.2		V
output voltage adjustment range (V_O)			0.60		1.8	V
output voltage adjustment including PMBus margining (V_O)			0.54		1.98	V
output voltage set-point resolution (V_O)				0.025		$\%V_O$
output voltage accuracy[2] (V_O)	including line, load, temp		-1		1	$\%V_O$
internal resistance +S/-S to VOUT/GND (V_O)				47		Ω
+S bias current (V_O)			-100	20	100	µA
-S bias current (V_O)				20		µA
line regulation (V_O)	I_O = max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		2 2 2		mV mV mV
load regulation (V_O)	I_O = 0~100%	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		2 2 2		mV mV mV
output ripple & noise (V_O)	(up to 20 MHz)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		2.5 3.5 5.0		mVp-p mVp-p mVp-p
output current (I_O)			0		90	A
current limit threshold (I_{lim})			100	114	125	A

Notes: 2. For V_o < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus

PRODUCT ELECTRICAL SPECIFICATION (CONTINUED)

parameter	conditions/description		min	typ	max	units
short circuit current (I_{SC})	RMS, hiccup mode, V_O = 1.0 V, 1.5 mΩ short			12		A
efficiency (η)	50% of max I_O	V_O = 0.6 V		87.6		%
		V_O = 1.0 V		91.4		%
		V_O = 1.8 V		94.3		%
	I_O = max I_O	V_O = 0.6 V		83.7		%
		V_O = 1.0 V		88.7		%
		V_O = 1.8 V		92.5		%
power dissipation at max I_O (d)		V_O = 0.6 V		10.5		W
		V_O = 1.0 V		11.5		W
		V_O = 1.8 V		13.1		W
input idling power (P_{Ii})	I_O = 0	V_O = 0.6 V		1.29		W
		V_O = 1.0 V		1.35		W
		V_O = 1.8 V		1.82		W
input standby power (P_{CTRL})	turned off with CTRL-pin			0.44		W
switching frequency (f_{SW} = 1/T_{SW})				320		kHz
switching frequency range[2] (f_{SW} = 1/T_{SW})	PMBus configurable FREQUENCY_SWITCH		200		640	kHz
switching frequency set-point accuracy (f_{SW} = 1/T_{SW})			-5		5	%
external sync pulse width (f_{SW} = 1/T_{SW})			150			ns
input clock frequency drift tolerance (f_{SW} = 1/T_{SW})	external sync		-10		10	%
initialization time (T_{INIT})	From VI > ~2.7 V to ready to be enabled			67		ms
output voltage total on delay time (T_{ONdel_tot})	enabled by input voltage			T_{INIT} + T_{ONdel}		
	enabled by CTRL pin			T_{ONdel}		
output voltage on delay time (T_{ONdel})	turn on delay duration			5		ms
	range PMBus configurable TON_DELAY		3		250	ms
	accuracy (actual delay vs set value)			-0/+2		ms
output voltage off delay time[3] (T_{OFFdel})	turn off delay duration			0		ms
	range PMBus configurable TOFF_DELAY		4		250	ms
	accuracy (actual delay vs set value)			-0/+2		ms
output voltage on/off ramp up time (0→100%,100→0% of V_O) (T_{ONrise}/$T_{OFFfall}$)	turn on ramp duration			5		ms
	turn off ramp duration			Disabled in standard configuration. Turn off immediately upon expiration of turn off delay.		
	ramp duration range PMBus configurable TON_RISE/TOFF_FALL		0		100	ms
	ramp time accuracy for standalone operation (actual ramp time vs set value)			250		µs
power good threshold (PG)	rising			90		%V_O
	falling			85		%V_O
power good threshold range (PG)	PMBus configurable POWER_GOOD_ON VOUT_UV_FAULT_LIMIT		0		100	%V_O

Notes:
1. Value refers to total (internal + external) effective output capacitance. Capacitance derating with VO typical for ceramic capacitors (bias characteristics) and temperature variations must be considered for the external capacitor(s). See section External Output Capacitors.
2. There are configuration changes to consider when changing the switching frequency, see section Switching Frequency.
3. The specified accuracy applies for off delay times larger than 4 ms. A value of 0 ms can be set to guarantee a fast shut-off, but this will force the device to Immediate Off behavior, even if soft-off, i.e. ramp-down, is configured. When setting 0 ms the actual delay will be 0 ms.

PRODUCT ELECTRICAL SPECIFICATION (CONTINUED)

parameter	conditions/description	min	typ	max	units
power good delay (PG)	From VO reaching target to PG assertion		2		ms
power good delay range (PG)	PMBus configurable POWER_GOOD_DELAY	0		5000	ms
input under voltage protection threshold (IUVP)			6.4		V
input under voltage protection threshold range (IUVP)	PMBus configurable VIN_UV_FAULT_LIMIT		6.4~14		V
input under voltage protection hysteresis (IUVP)			0.5		V
input under voltage protection hysteresis range (IUVP)	PMBus configurable VIN_UV_WARN_LIMIT		0~7.6		V
input under voltage protection set point accuracy (IUVP)			280		mV
input under voltage protection response delay (IUVP)			100		µs
input under voltage protection fault response[1] (IUVP)	shutdown, automatic restart VIN_UV_FAULT_RESPONSE		280		ms
input over voltage protection threshold (IOVP)			16		V
input over voltage protection threshold range (IOVP)	PMBus configurable VIN_OV_FAULT_LIMIT		6.9~16		V
input over voltage protection hysteresis (IOVP)			1		V
input over voltage protection hysteresis range (IOVP)	PMBus configurable VIN_OV_WARN_LIMIT		0~9.1		V
input over voltage protection set point accuracy (IOVP)			280		mV
input over voltage protection response delay (IOVP)			100		µs
input over voltage protection fault response[1] (IOVP)	shutdown, automatic restart VIN_OV_FAULT_RESPONSE		280		ms
output under voltage protection threshold (UVP)			85		$\%V_O$
output under voltage protection threshold range (UVP)	PMBus configurable VOUT_UV_FAULT_LIMIT		0~100		$\%V_O$
output over voltage protection threshold (OVP)			115		$\%V_O$
output over voltage protection threshold range (OVP)	PMBus configurable VOUT_OV_FAULT_LIMIT		100~115		$\%V_O$
output over/under voltage protection response time (UVP/OVP)			10		µs
output over/under voltage protection fault response[1] (UVP/OVP)	shutdown, automatic restart VOUT_UV_FAULT_RESPONSE VOUT_OV_FAULT_RESPONSE		280		ms

Notes: 1. Automatic restart ~280 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information for other fault response options.

PRODUCT ELECTRICAL SPECIFICATION (CONTINUED)

parameter	conditions/description	min	typ	max	units
over current protection threshold[1] (OCP)	set value per phase		57		A
over current protection threshold range[1] (OCP)	PMBus configurable IOUT_AVG_OC_FAULT_LIMIT		0~57		A
over current protection protection delay[1] (OCP)			5		T_{SW}
over current protection fault response[1] (OCP)	shutdown, automatic restart[2] MFR_IOUT_OC_FAULT_RESPONSE		280		ms
over temperature protection threshold[3] (OTP)	position P3		125		°C
over temperature protection threshold range[3] (OTP)	position P3 PMBus configurable OT_FAULT_LIMIT		-40~125		°C
over temperature protection hysteresis[3] (OTP)	position P3 PMBus configurable		15		°C
over temperature protection fault response[3] (OTP)	position P3 shutdown, automatic restart[2] OT_FAULT_RESPONSE		280		ms
over temperature protection threshold[3] (OTP)	position P1		150		°C
over temperature protection threshold range[3] (OTP)	position P1 PMBus configurable MFR_VMON_OV_FAULT_LIMIT		-40~150		°C
over temperature protection hysteresis[3] (OTP)	position P1 PMBus configurable		25		°C
over temperature protection fault response[3] (OTP)	position P1 shutdown, automatic restart[2] VMON_OV_FAULT_RESPONSE		280		ms
monitoring accuracy	input voltage READ_VIN		280		mV
	output voltage READ_VOUT		1		$\%V_O$
	output current READ_IOUT	T_{P1} = 25 °C, V_O = 1.0 V T_{P1} = 0-95 °C, V_O = 1.0 V	1 3.5		A A
	duty cycle READ_DUTY_CYCLE	No tolerance, value is that applied to PWM controller			
	temperature READ_TEMPERATURE_1	position P3	-10		5	%
tracking input bias current[4]	VTRK = 5 V		70	200	µA
tracking input voltage range	VTRK pin		0~1.8		V
tracking accuracy	regulation 100% tracking ramp accuracy, V_O = 1.0 V, 5 ms ramp	-2		2	mV
current difference between products in a current sharing group	steady state operation		Max 2 x READ_IOUT monitoring accuracy		
number of products in a current sharing group				4	

Notes:
1. The set OCP limit applies per phase. The total OCP limit will be twice the set value.
2. Automatic restart ~280 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information for other fault response options.
3. See section Over Temperature Protection (OTP).
4. The maximum tracking rise-time is 1 V/ms, see section Voltage Tracking.

PRODUCT ELECTRICAL SPECIFICATION (CONTINUED)

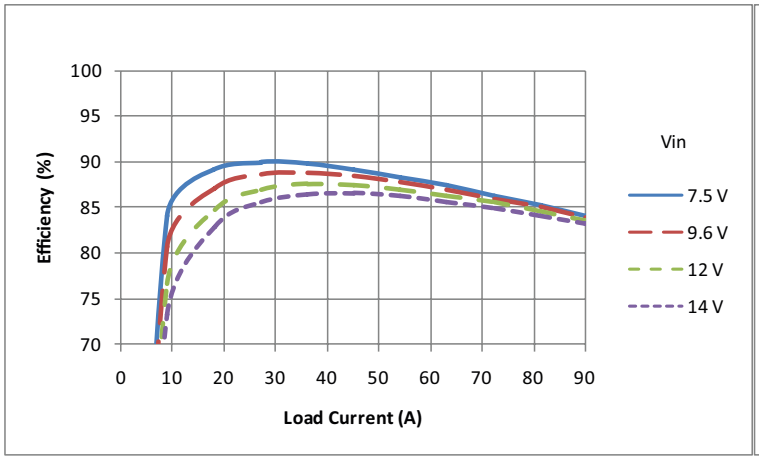
parameter	conditions/description	min	typ	max	units
logical output low signal level (V_{OL})	SCL, SDA, SYNC, DDC, SLRT, PG sink/source current = 2 mA			0.5	V
logical output high signal level (V_{OH})	SCL, SDA, SYNC, DDC, SLRT, PG sink/source current = 2 mA	2.25			V
logic output low sink current (I_{OL})		-2			mA
logic output high source current (I_{OH})				2	mA
logic input low threshold (V_{IL})	SCL, SDA, CTRL, SYNC, DDC			0.8	V
logic input high threshold (V_{IH})	SCL, SDA, CTRL, SYNC, DDC	2			V
logic leakage current (I_{I_LEAK})	SCL, SDA, SYNC, SLRT, PG	-100		100	µA
logic pin input capacitance (C_{I_PIN})	SCL, SDA, CTRL, SYNC, DDC		12		pF
logic pin internal pull-up resistance (R_{I_PU})	SCL, SDA, SLRT CTRL to +5V DDC to +5V		no internal pull-up 10 47		 kΩ kΩ
SMBus operating frequency (f_{SMB})		100		400	kHz
SMBus bus free time[1] (T_{BUF})	STOP bit to START bit	1.3			µs
SMBus SDA setup time from SCL[1] (t_{set})		100			ns
SMBus SDA hold time from SCL[1] (t_{hold})		300			ns
SMBus START/STOP condition setup/hold time from SCL		600			ns
SCL low period (T_{low})		1.3			µs
SCL high period (T_{high})		0.6			µs

Notes: 1. See SMBus - Timing section.

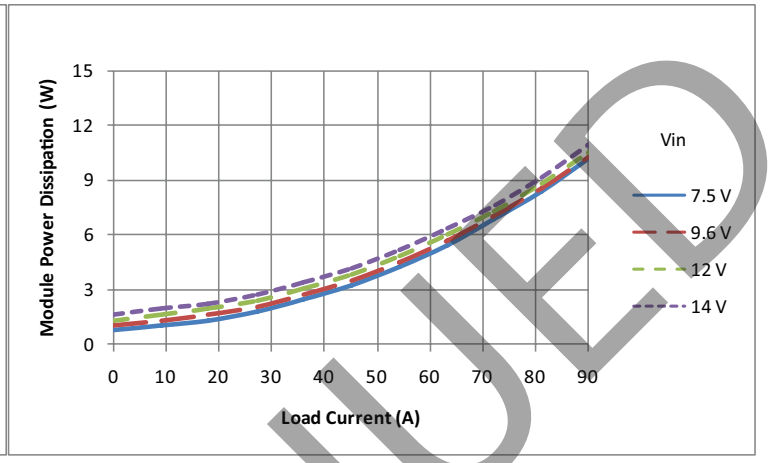
TYPICAL OUTPUT CHARACTERISTICS, V_0 = 0.6 V

Conditions [Standard configuration unless otherwise stated]: T_{P1} = 25°C

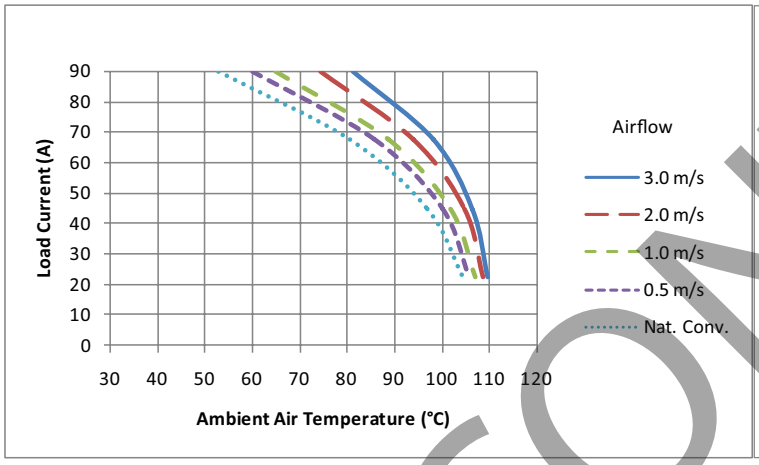
Efficiency



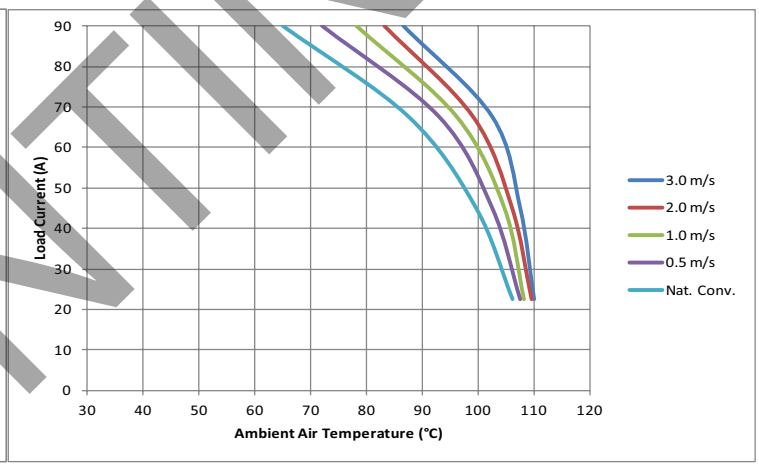
Power Dissipation



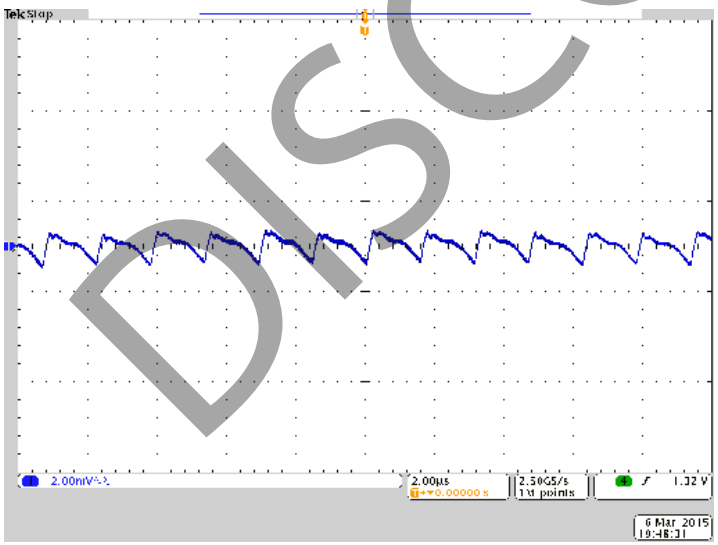
Output Current Derating for Vertical Version



Output Current Derating for Lay Down Version

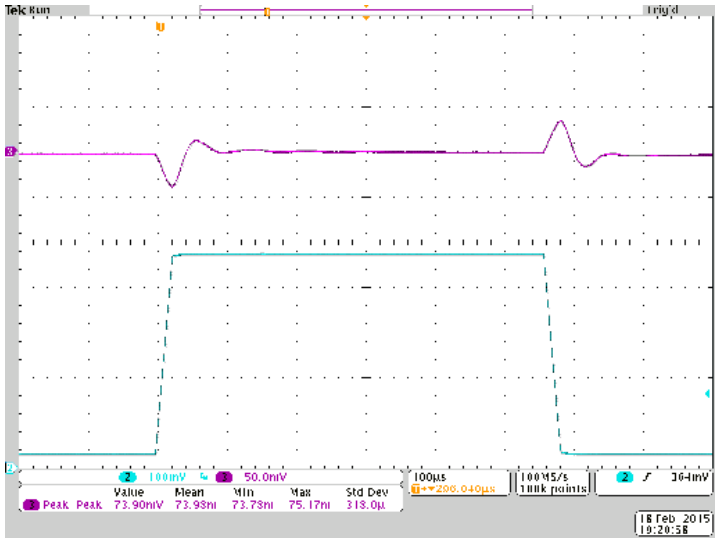


Output Ripple and Noise



Vin = 12 V, Iout = Imax

Transient Response

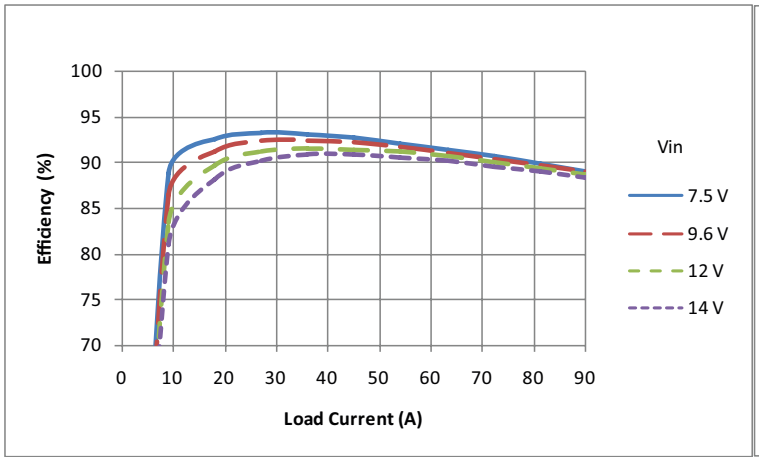


Vin = 12 V, Iout = 25% Imax ➞ 75% Imax ➞ 25% Imax

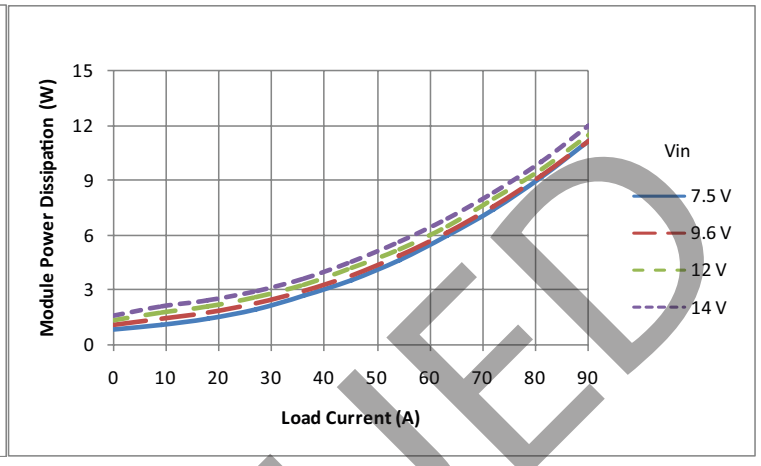
TYPICAL OUTPUT CHARACTERISTICS, V_0 = 1.0 V

Conditions [Standard configuration unless otherwise stated]: T_{P1} = 25°C

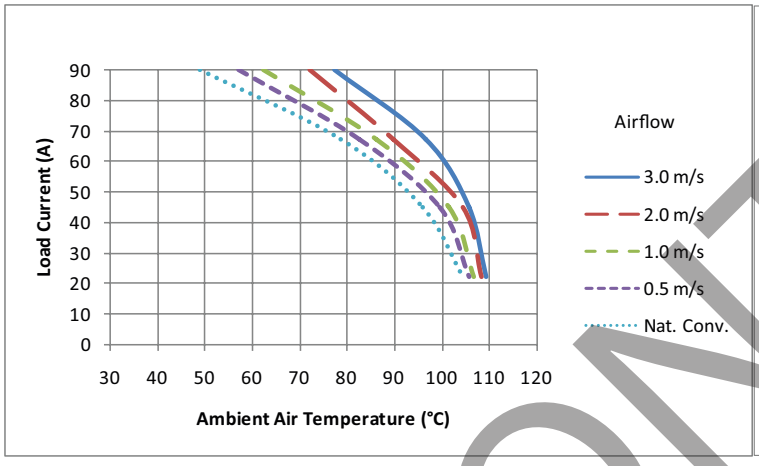
Efficiency



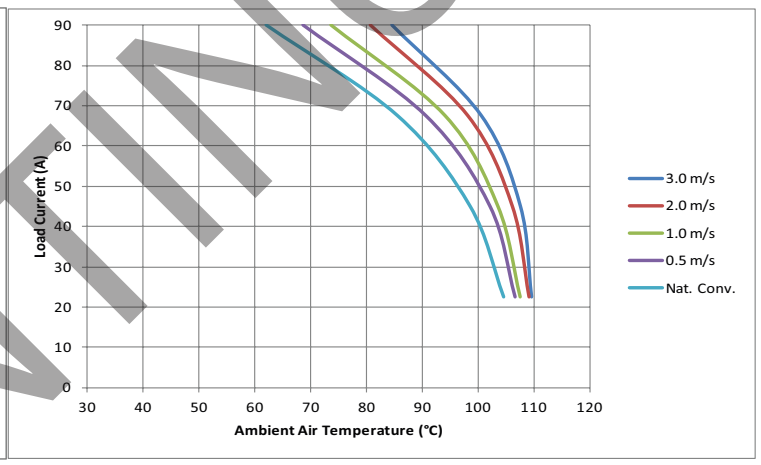
Power Dissipation



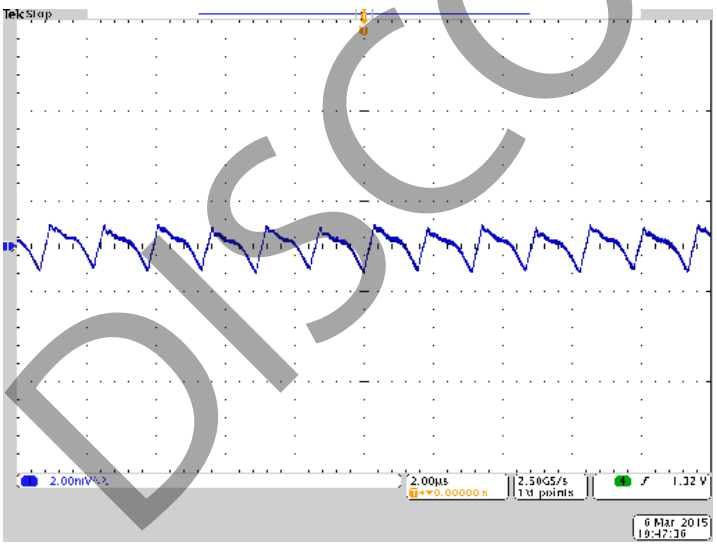
Output Current Derating for Vertical Version



Output Current Derating for Lay Down Version

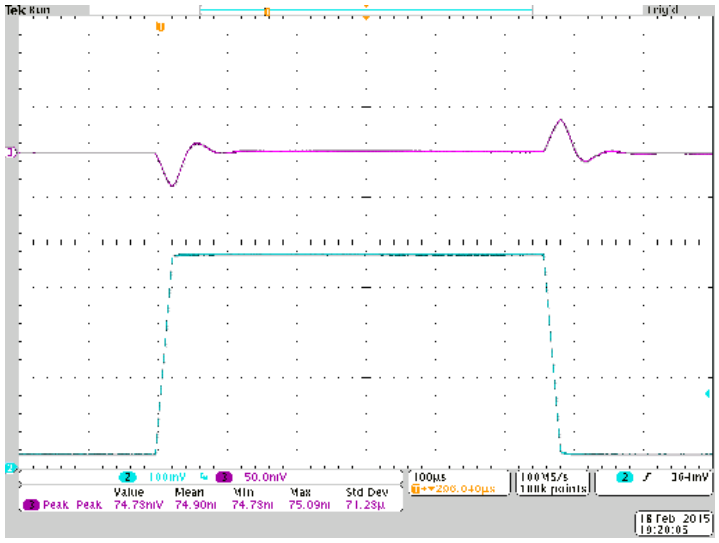


Output Ripple and Noise



Vin = 12 V, Iout = Imax

Transient Response

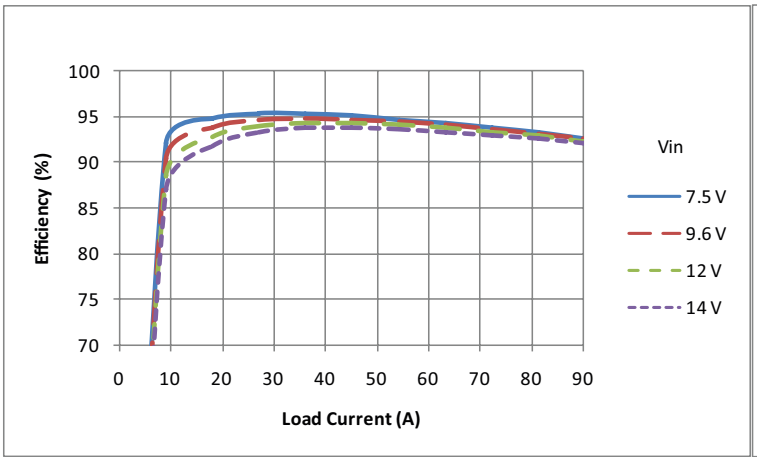


Vin = 12 V, Iout = 25% Imax ➞ 75% Imax ➞ 25% Imax

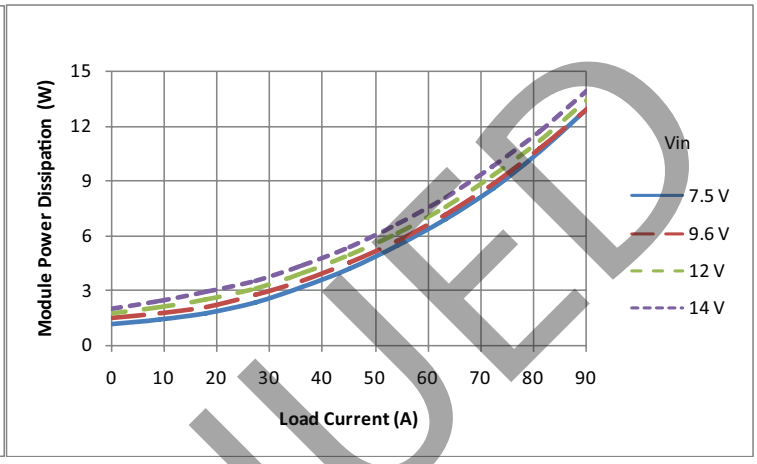
TYPICAL OUTPUT CHARACTERISTICS, V_0 = 1.8 V

Conditions [Standard configuration unless otherwise stated]: T_{P1} = 25°C

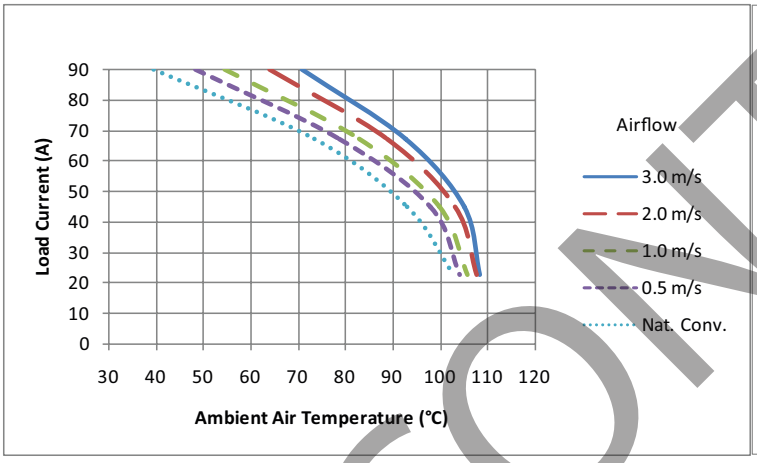
Efficiency



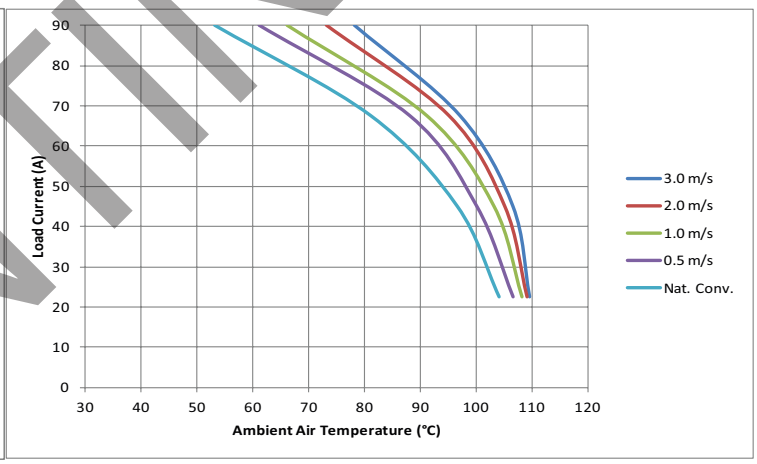
Power Dissipation



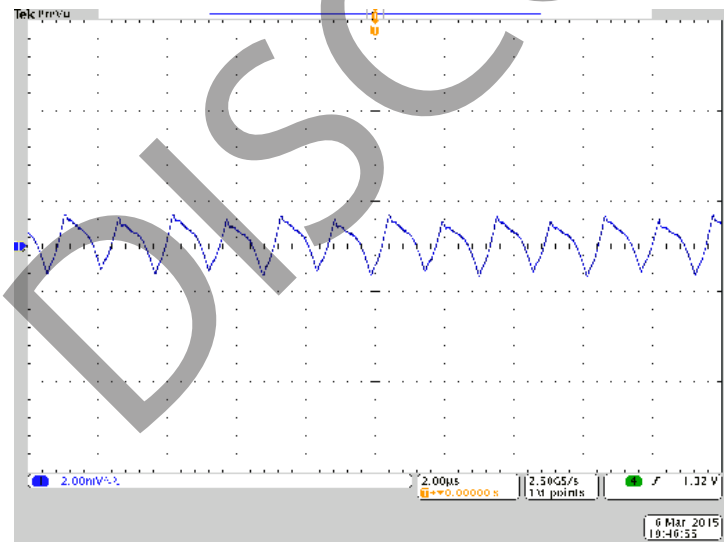
Output Current Derating for Vertical Version



Output Current Derating for Lay Down Version

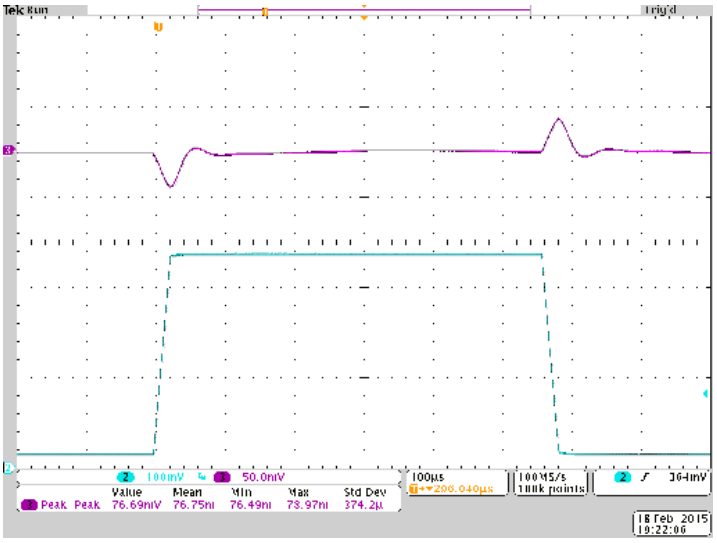


Output Ripple and Noise



Vin = 12 V, Iout = Imax

Transient Response

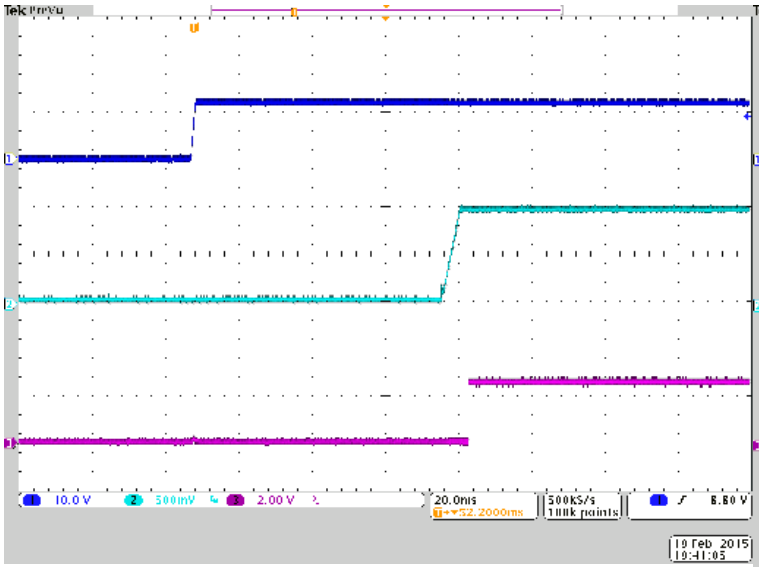


Vin = 12 V, Iout = 25% Imax ➞ 75% Imax ➞ 25% Imax

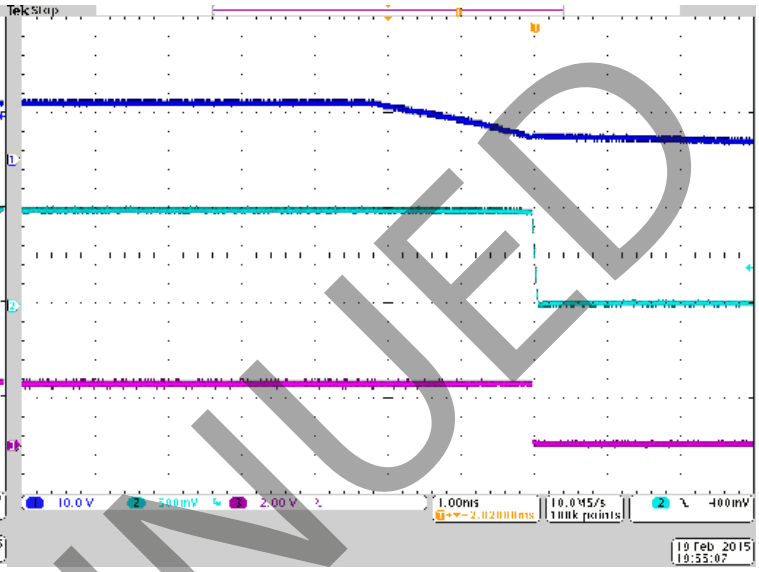
TYPICAL ON/OFF CHARACTERISTICS

Conditions [Standard configuration unless otherwise stated]: T_{P1} = 25°C, V_0 = 1.0 V

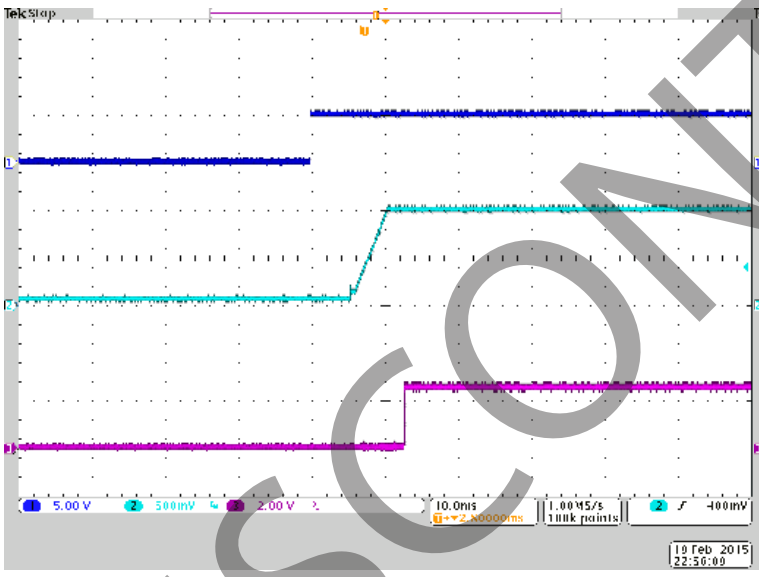
Enable by input voltage



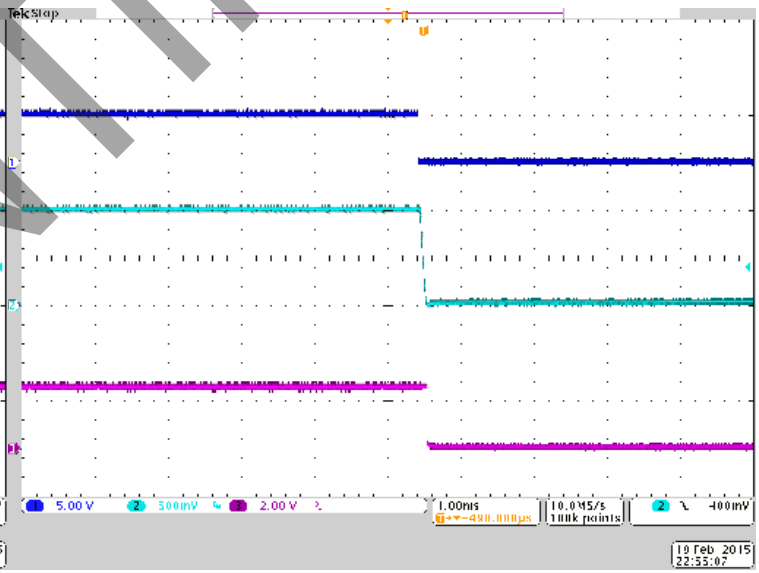
Disable by input voltage



Enable by CTRL pin



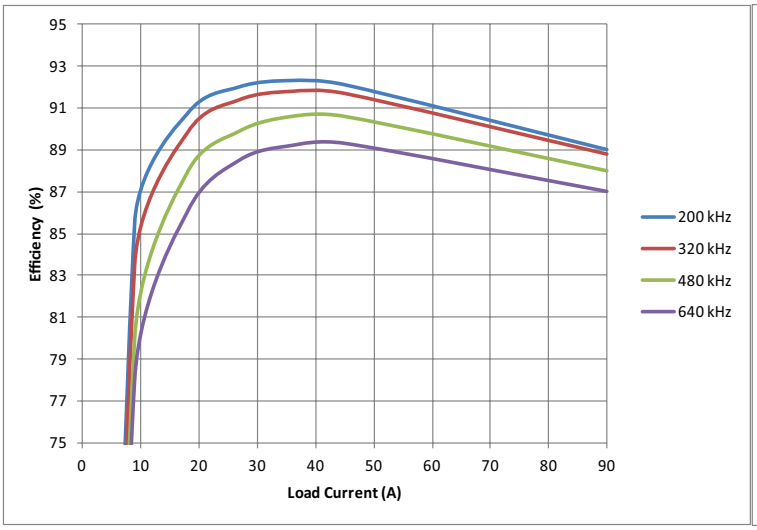
Disable by CTRL pin



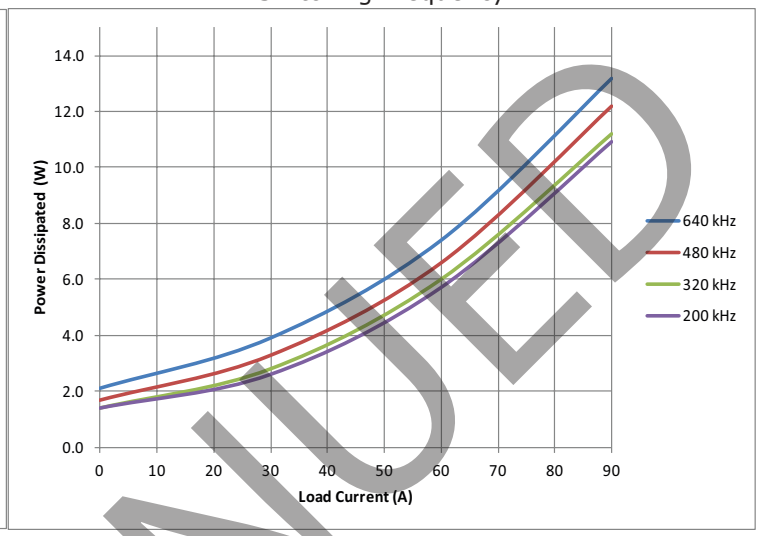
TYPICAL CHARACTERISTICS

Conditions [Standard configuration unless otherwise stated]: T_{P1} = 25°C

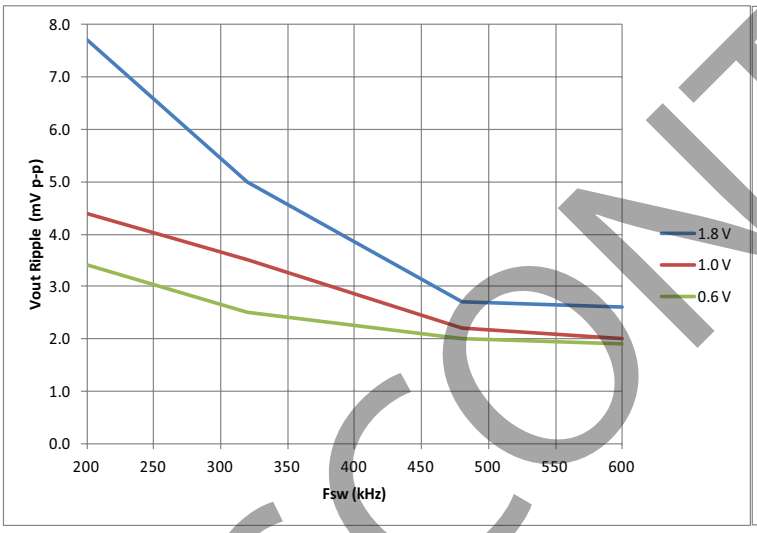
Efficiency vs. Output Current and Switching Frequency



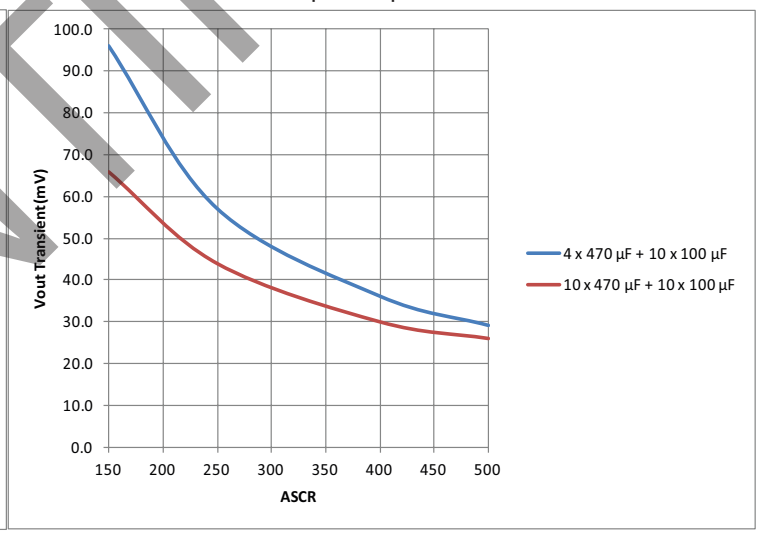
Power Dissipation vs. Output Current and Switching Frequency



Output Ripple vs. Switching Frequency

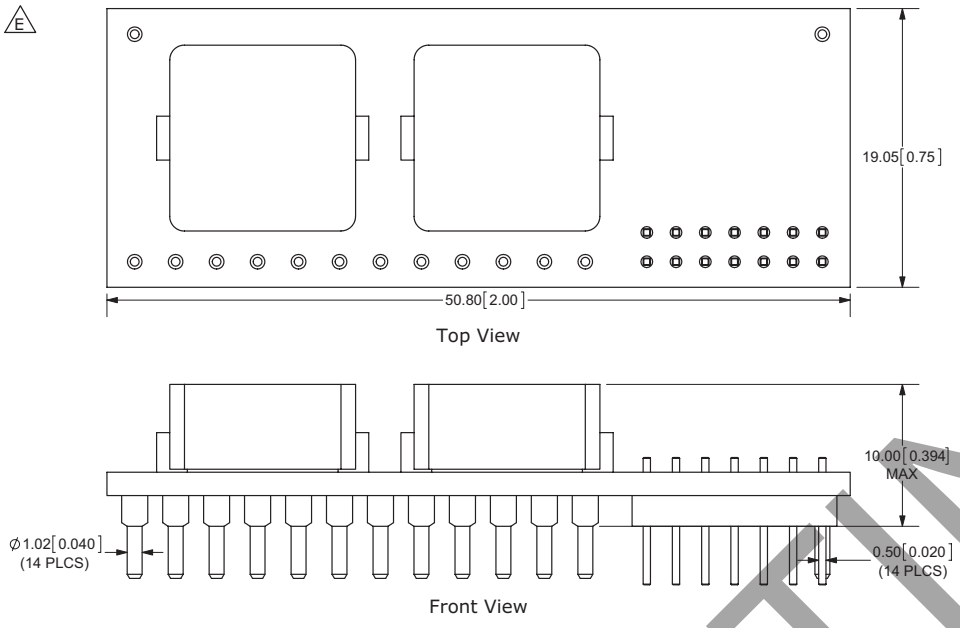


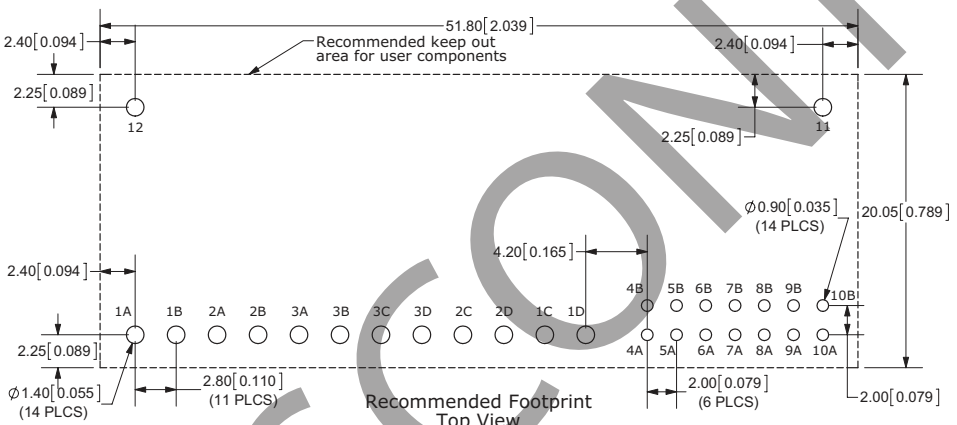
Load Transient vs. ASCR Gain and External Output Capacitance



MECHANICAL DRAWING (HORIZONTAL, THROUGH-HOLE MOUNT)

units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)



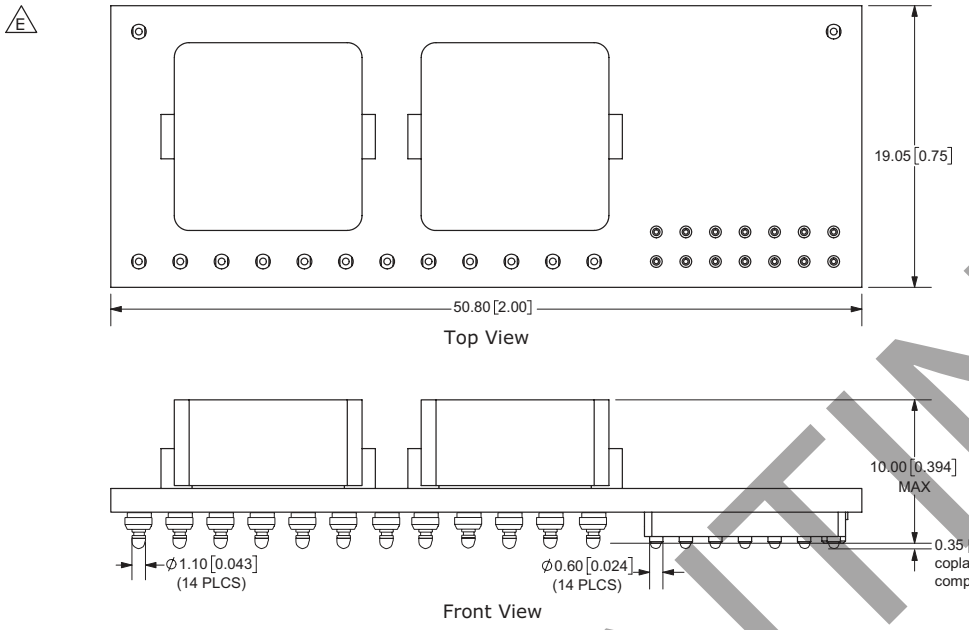


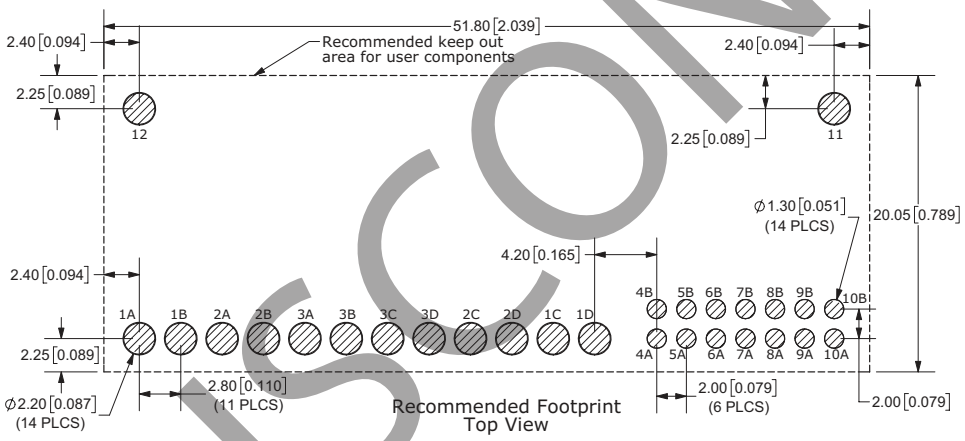
PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A, 1B, 1C, 1D	VIN	Copper Alloy	Min 0.1 µm Au over 1~3 µm Ni
2A, 2B, 2C, 2D	GND		
3A, 3B, 3C, 3D	VOUT		
4A	+S		
4B	-S		
5A	VSET		
5B	VTRK		
6A	SLRT		
6B	SDA		
7A	SCL		
7B	FAULT		
8A	SA		
8B	SYNC		
9A	PG		
9B	CTRL		
10A	DDC		
10B	PREF		
11	N/C		
12	N/C		

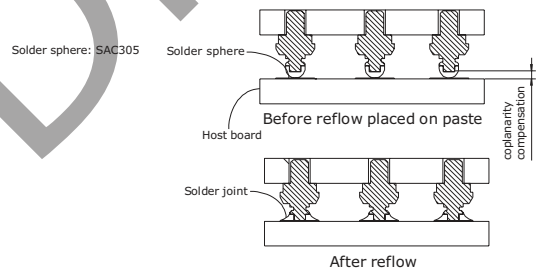
Note: 1. 0.19 mm [0.008 inches] minimum clearance components under POL module to host PCB.

MECHANICAL DRAWING (HORIZONTAL, SURFACE MOUNT)

units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)



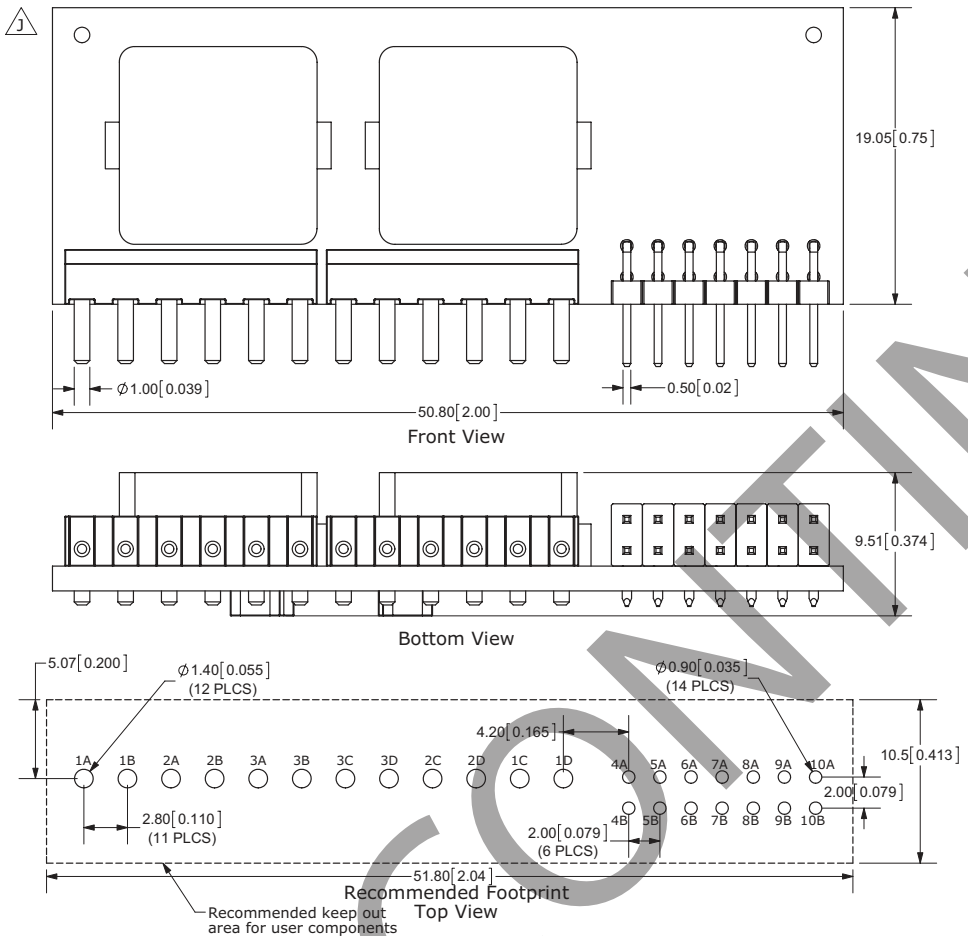




PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A, 1B, 1C, 1D	VIN	Copper Alloy	Min 0.1 µm Au over 2 µm Ni
2A, 2B, 2C, 2D	GND		
3A, 3B, 3C, 3D	VOUT		
4A	+S		
4B	-S		
5A	VSET		
5B	VTRK		
6A	SLRT		
6B	SDA		
7A	SCL		
7B	FAULT		
8A	SA		
8B	SYNC		
9A	PG		
9B	CTRL		
10A	DDC		
10B	PREF		
11	N/C		
12	N/C		

MECHANICAL DRAWING (VERTICAL)

units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)



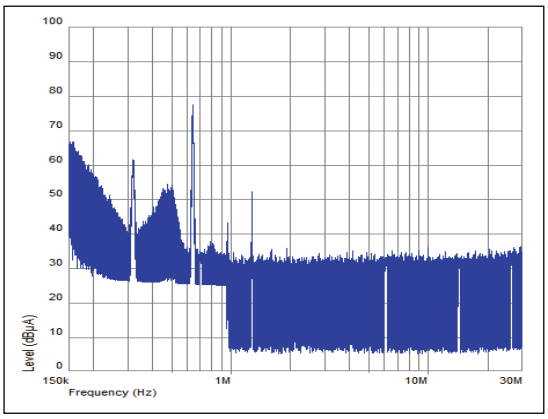
PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A, 1B, 1C, 1D	VIN	Copper Alloy	Min 0.1 µm Au over 1~3 µm Ni
2A, 2B, 2C, 2D	GND		
3A, 3B, 3C, 3D	VOUT		
4A	+S		
4B	-S		
5A	VSET		
5B	VTRK		
6A	SLRT		
6B	SDA		
7A	SCL		
7B	FAULT		
8A	SA		
8B	SYNC		
9A	PG		
9B	CTRL		
10A	DDC		
10B	PREF		

EMC SPECIFICATION

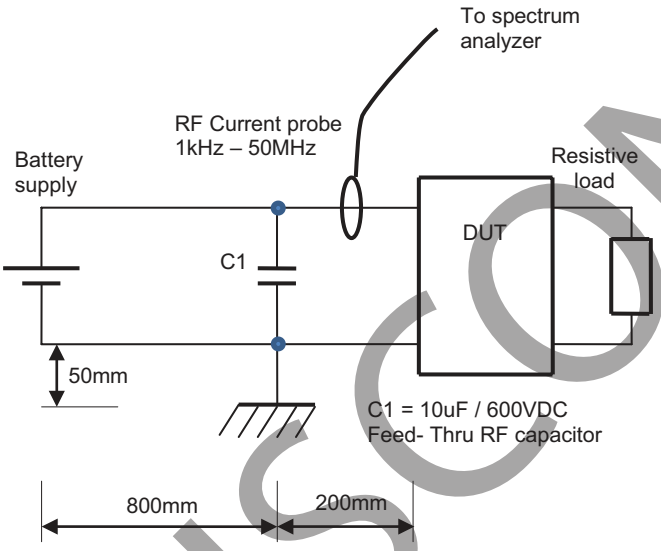
Conducted EMI is measured according to the test set-up below. The typical fundamental switching frequency is 320 kHz.

Conducted EMI

Input terminal value (typical for standard configuration).
V_I = 12 V, V_O = 1.0 V, I_O = I_{MAX}



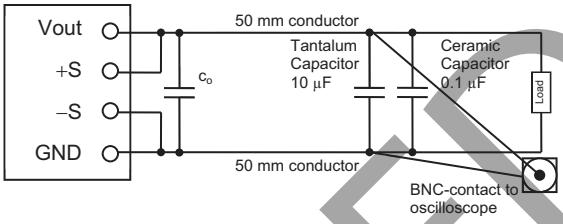
EMI without filter.



Test set-up conducted emission, power lead.

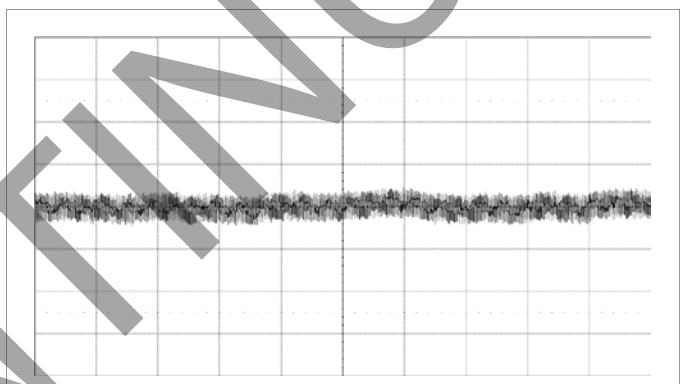
Output Ripple and Noise

The circuit shown below is used to measure output ripple and noise. A damped filter is created by the 50 mm conductor and the two capacitors.



Output ripple and noise test set-up.

The following is an example of the low frequency output ripple and noise as measured with the above circuit.



V_I=12 V, V_O=1.0 V, I_O=90 A, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF, 5 mV/div, 50 µs/div

Example of low frequency ripple at the output.

PMBUS INTERFACE

Power Conversion Overview

The NDM3Z-90 module has several features to enable high power conversion efficiency. Adaptive algorithms and cycle-by-cycle charge management improves the response time and reduces the output deviation as a result of load transients. The incorporation of DFM enhances the CUI modules for improved performance.

Power Management Overview

This product incorporates a wide range of configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults.

The product's standard configuration is suitable for a wide range of operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix at the end of this specification. The ability of CUI modules to digitally control, configure and monitor OS features provides significant benefits during development, production and the product life.

SMBus Interface

The product can be used with any standard two-wire I2C or SMBus host device. See Electrical Specification for allowed clock frequency range. In addition, the product is compatible with PMBus version 1.2 and includes an SLRT line to help mitigate limitations related to continuous fault monitoring. The PMBus signals SCL, SDA and SLRT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$T = R_P C_P \leq 1\mu s$

Where R_P is the pull-up resistor value and C_P is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

PMBus Addressing

The PMBus address is configured with a resistor connected between the SA pin and the PREF pin, as shown in the Typical Application Circuit. Recommended resistor values are shown in the table below. 1% tolerance resistors are required.

R_{SA} (kΩ)	Address	R_{SA} (kΩ)	Address
0 (short)	0x26	42.2	0x28
10	0x19	46.4	0x29
11	0x1A	51.1	0x2A
12.1	0x1B	56.2	0x2B
13.3	0x1C	61.9	0x2C
14.7	0x1D	68.1	0x2D
16.2	0x1E	75	0x2E
17.8	0x1F	82.5	0x2F
19.6	0x20	90.9	0x30
21.5	0x21	100	0x31
23.7	0x22	110	0x32
26.1	0x23	121	0x33
28.7	0x24	133	0x34
31.6	0x25	147	0x35
34.8	0x26	162	0x36
38.3	0x27	178	0x37
		infinite (open)	0x28

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	general call address / START byte
0x01	CBUS address
0x02	address reserved for different bus format
0x03 ~ 0x07	reserved for future use
0x08	SMBus host
0x09 ~0x0B	assigned for smart battery
0x0C	SMBus alert response address
0x28	reserved for ACCESS.bus host
0x2C ~ 0x2D	reserved for previous versions of the SMBus specification
0x37	reserved for ACCESS.bus default address
0x40 ~ 0x44	reserved by previous versions of the SMBus specification
0x48 ~ 0x4B	unrestricted addresses
0x61	SMBus device default address
0x78 ~ 0x7B	10-bit slave addressing
0x7C ~ 0x7F	reserved for future use

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus Command
input voltage	READ_VIN
output voltage	READ_VOUT
total output current	READ_IOUT
output current of each phase	READ_IOUT0 READ_IOUT1
controller temperature	READ_TEMPERATURE_1
switching frequency	READ_FREQUENCY
duty cycle	READ_DUTY_CYCLE
highest temperature of power switches*	READ_VMON

* Reports a voltage level corresponding to the temperature. See command details in the end of this specification.

Monitoring Faults

Fault conditions can be monitored using the SLRT pin, which will be asserted low when any number of pre-configured fault or warning conditions occur. The SLRT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled. It is possible to mask which fault conditions should not assert the SLRT pin by the command MFR_SMBALERT_MASK.

In response to the SLRT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
overview, power good	STATUS_WORD STATUS_BYTE
output voltage level	STATUS_VOUT
output current level	STATUS_IOUT
input voltage level	STATUS_INPUT
temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
miscellaneous	STATUS_MFR_SPECIFIC

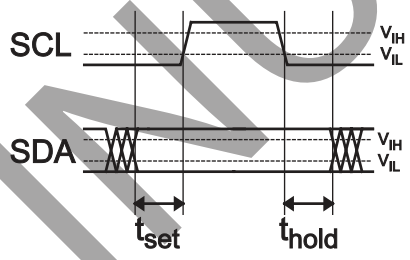
Snapshot Parameter Capture

This product offers a special feature that enables the user to capture parametric data during normal operation by a single PMBus command SNAPSHOT. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Controller temperature
- Switching frequency
- Duty cycle
- Status and fault information

When a fault occurs the Snapshot functionality will automatically store this parametric data to NVM. The data can then later be read back to provide valueable information for analysis. It is possible to select which faults will trigger a store to NVM by the PMBus command SNAPSHOT_FAULT_MASK.

PMBus/I²C Timing



Setup and hold times timing diagram.

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification for SMBus electrical and timing requirements.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A busfree time delay according to this specification must occur between every SMBus transmission (between every stop & start condition). The product supports PEC (Packet Error Checking) according to the SMBus specification.

When sending subsequent commands to the same unit it is recommended to insert additional delays after write transactions according to the table below. After read transactions a delay of 2 ms should be inserted before accessing the unit again.

PMBus Command	Delay after *write* before additional command
STORE_USER_ALL	100 ms
STORE_DEFAULT_ALL	100 ms
RESTORE_USER_ALL	100 ms
RESTORE_DEFAULT_ALL	100 ms
any other command	10 ms

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the PMBus command values; the Default NVM and the User NVM. The Default NVM is pre-loaded with CUI factory default values. The Default NVM is write-protected and can be used to restore the CUI factory default values through the command RESTORE_DEFAULT_ALL. The User NVM is pre-loaded with CUI factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, whereafter commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.

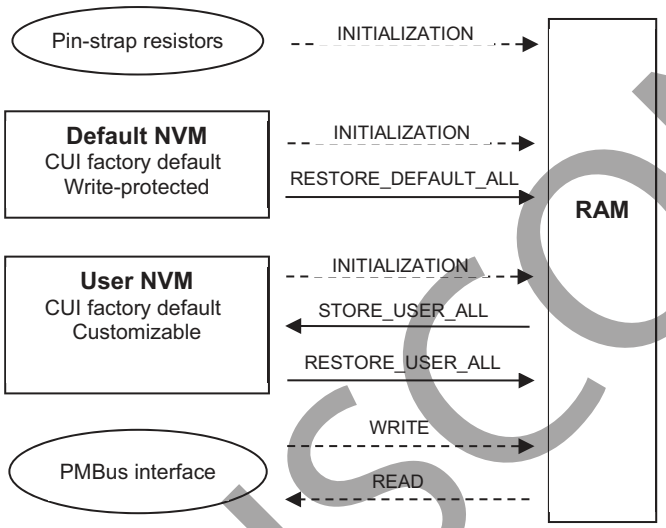


Illustration of memory areas of the product.

Command Protection

The user may write-protect specific PMBus commands in the User NVM by using the command UNPROTECT.

Initialization Procedure

The product follows an internal initialization procedure after power is applied to the VIN pin:

1. Self test and memory check.
2. The address pin-strap resistors are measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured and the associated output voltage level will be loaded to operational RAM of PMBus command VOUT_COMMAND.
4. CUI factory default values stored in default NVM memory are loaded to operational RAM. This overwrites any previously loaded values.
5. Values stored in the User NVM are loaded into operational RAM memory. This overwrites any previously loaded values (e.g. VOUT_COMMAND by pin-strap).
6. Check for external clock signal at the SYNC pin and lock internal clock to the external clock if used.

Once this procedure is completed and the Initialization Time has passed (see Electrical Specification), the output voltage is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

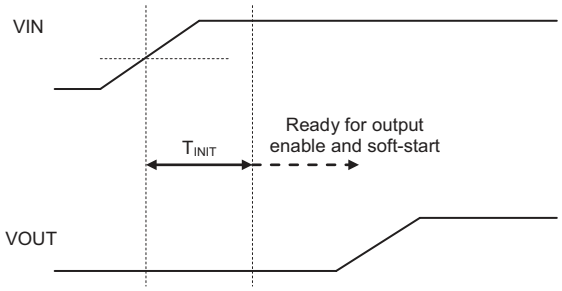


Illustration Initialization time.

OPERATING INFORMATION

Input Voltage
The input voltage range 7.5-14V makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter.

Input Under Voltage Protection (IUVP)
The product monitors the input voltage and will turn-on and turn-off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels. Once the input voltage falls below the turn-off threshold, the device can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the input voltage is below the turn-on threshold. Operation resumes automatically and the output is enabled when the input voltage has risen above the turn-on threshold.

The default response is option 2. The IUVP function can be reconfigured using the PMBus commands VIN_UV_FAULT_LIMIT (turn-off threshold), VIN_UV_WARN_LIMIT (turn-on threshold) and VIN_UV_FAULT_RESPONSE.

Input Over Voltage Protection (IOVP)
The product monitors the input voltage continously and will respond as configured when the input voltage rises above the configured threshold level (see Electrical Specification). Refer to section "Input Under Voltage Protection" for functionality, response configuration options and default setting. The IOVP function can be reconfigured using the PMBus commands VIN_OV_FAULT_LIMIT (turn-off threshold), VIN_OV_WARN_LIMIT (turn-on threshold) and VIN_OV_FAULT_RESPONSE.

Input and Output Impedence
The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors
The product is a two-phase converter which gives lower input ripple than a single phase design. Thus, ripple-current-rating requirements for the input capacitors are lower.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

If several products are connected in a phase spreading setup the amount of input ripple current, and capacitance per product, can be reduced.

Input capacitors must be placed closely and with low impedance connections to the VIN and GND pins in order to be effective.

External Output Capacitors
The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to achieve a small output deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

It is recommended to locate low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts and cabling in order for capacitance to be effective.

Dynamic Loop Compensation (DLC)
The typical design of regulated power converters includes a control function with a feedback loop that can be closed using either analog or digital circuits. The feedback loop

is required to provide a stable output voltage, but should be optimized for the output filter to maintain output voltage regulation during transient conditions such as sudden changes in output current and/or input voltage. Digitally controlled converters allow one to optimize loop parameters without the need to change components on the board, however, optimization can still be challenging because the key parameters of the output filter include parasitic impedances in the PCB and the often distributed filter components themselves.

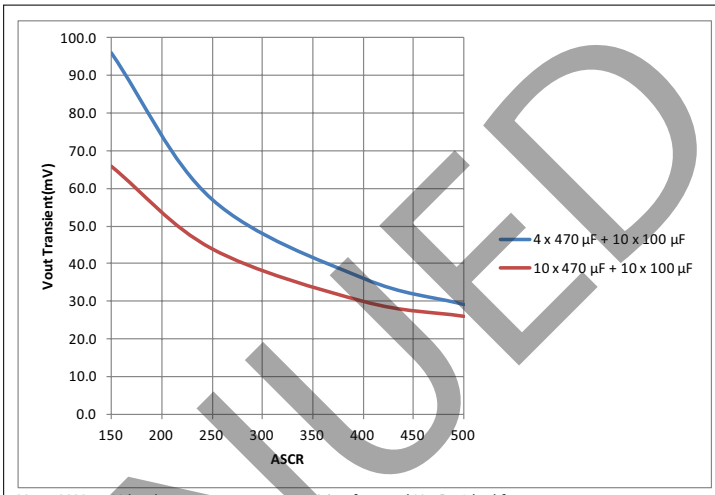
Dynamic Loop Compensation has been developed to solve the problem of compensation for a converter with a difficult to define output filter. This task is achieved by utilization of algorithms that can identify an arbitrary output filter based on accurate measurements of the output voltage in response to a very small excitation signal initiated by the algorithm, or occurring due to the changes in operating conditions, and automatically adjust feedback loop parameters to match the output filter.

Details of the algorithm that is used to characterize an output filter and the different operational modes can be found in the following sections.

Control Loop

The products use a fully digital control loop that achieves precise control of the entire power conversion process, resulting in a very flexible device that is also very easy to use. A non-linear charge-mode control algorithm is implemented that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers, thus saving cost and board space. The algorithm is inherently stable at all conditions due to a residual scheme.

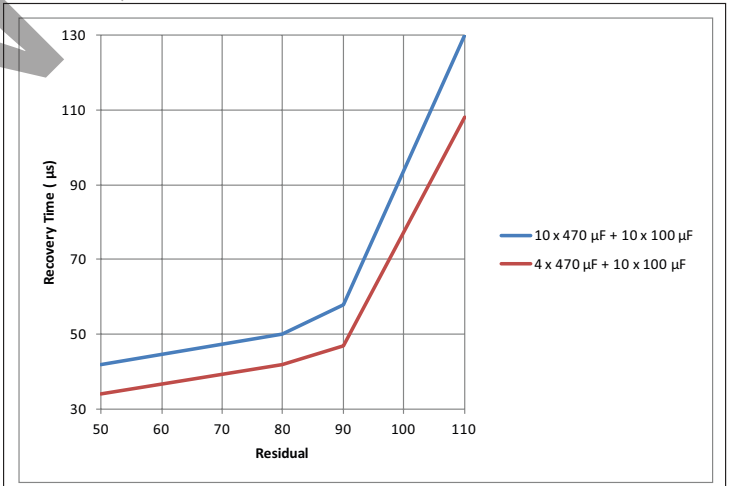
Control may be set more or less aggressive by adjusting a gain factor, set by the PMBus command ASCR_CONFIG. Increasing the gain, i.e the control effort, will reduce the voltage deviation at load transients, at the expense of somewhat increased ripple on the output. Below graph exemplifies the impact on load transient performance when adjusting the gain factor.



V_I=12 V, V_O=1 V, load step 25%-75%-25% , 2A/µs, f_{sw}=320 kHz, Residual factor=90

Voltage deviation vs. control loop gain setting and output capacitance

The user may also adjust the residual factor, set by the ASCR_CONFIG command, to improve the recovery time after a load transient.



V_I=12 V, V_O=1 V, load step 25%-75%-25% , 2A/µs, f_{sw}=320 kHz, gain factor=300

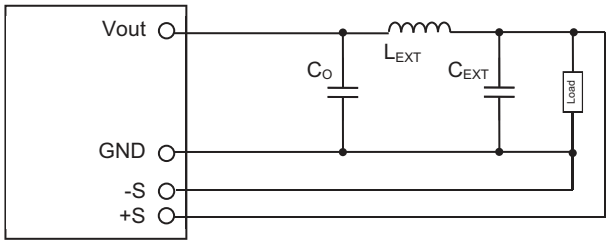
Recovery time vs. control loop residual setting and output capacitance.

By default the product is configured with a moderate gain setting to provide a trade-off between load transient performance and output ripple for a wide range of operating conditions. For a specific application the gain factor can be increased with an improved load transient response.

Remote Sense

The product has remote sense to compensate the voltage drops between the output and the point of load. The sense traces should be located close to each other and to the PCB ground layer to reduce noise susceptibility.

In cases where the external output filter includes an inductor (forming a pi filter) according to the picture below, the L_{EXT}/C_{EXT} resonant frequency places an upper limit on the controller loop bandwidth. If the resonant frequency is high the sense lines can be connected after the filter (as shown in the picture) – if the resonant frequency is low and the DC drop from L_{EXT} is acceptable, sensing before the filter may be better.



External output filter with inductor (pi filter).

Output Voltage Control

To control the output voltage the following options are available:

1. Output voltage is controlled through the CTRL pin.
2. Output voltage is controlled using the PMBus command OPERATION.

The CTRL pin has an internal 10 kΩ pull-up resistor to 5 V. The external device must provide a minimum required sink current to guarantee a voltage not higher than the logic low threshold level (see Electrical Characteristics). When the CTRL pin is left open, the voltage generated on the CTRL pin is 5 V.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to enabling the output voltage.

Output Voltage Adjust using Pin-Strap Resistor

Using an external Pin-strap resistor, R_{SET}, the output voltage can be set to several predefined levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin as shown in the Typical Application Circuit. Maximum 1% tolerance resistors are required.

R_{SET} (kΩ)	Vout [V]	R_{SET} (kΩ)	Vout [V]
0 (short)	1.00	26.1	1.10
10	0.60	28.7	1.15
11	0.65	31.6	1.20
12.1	0.70	34.8	1.25
13.3	0.75	38.3	1.30
14.7	0.80	42.2	1.40
16.2	0.85	46.4	1.50
17.8	0.90	51.1	1.60
19.6	0.95	56.2	1.70
21.5	1.00	61.9	1.80
23.7	1.05	infinite (open)	1.20

RSET also sets the maximum output voltage; see section Output Voltage Range Limitation. The resistor is sensed only during the initialization procedure after application of input voltage. Changing the resistor value during normal operation will not change the output voltage.

Output Voltage Adjust using PMBus

The output voltage set by pin-strap can be overridden up to a certain level (see section Output Voltage Range Limitation) by using the PMBus command VOUT_COMMAND. See Electrical Specification for adjustment range.

Voltage Margining Up/Down

Using the PMBus interface it is possible to adjust the output voltage to one of two predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the CTRL pin or by the PMBus.

Output Voltage Trim
The actual output voltage can be trimmed to optimize performance of a specific load by setting a non-zero value for PMBus command VOUT_TRIM. The value of VOUT_TRIM is summed with the nominal output voltage set by VOUT_COMMAND, allowing for multiple products to be commanded to a common nominal value, but with slight adjustments per load.

Output Voltage Range Limitation
The output voltage range that is possible to set by configuration or by the PMBus interface is hardware limited by the pin-strap resistor R_{SET}. The maximum output voltage is set to 115% of the output value defined by R_{SET}. This protects the application circuit from an over voltage due to an accidental PMBus command.

The limitation applies to the actual regulated output voltage rather than to the configured value. Thus, it is possible to write and read back a VOUT_COMMAND value higher than the limit, but the actual output voltage will be limited. The output voltage limit can be reconfigured to a lower value by writing the PMBus command VOUT_MAX.

Output Over Voltage Protection (OVP)
The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. The product can be configured to respond in different ways to the output voltage exceeding the OVP limit:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response is option 2. The OVP limit and fault response can be reconfigured using the PMBus commands VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE and OVUV_CONFIG.

Output Under Voltage Protection (UVP)
The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. Refer to section Output Over Voltage Protection for response configuration options and default setting. The UVP limit and fault response can be reconfigured using the PMBus commands VOUT_UV_FAULT_LIMIT and VOUT_UV_FAULT_RESPONSE.

Power Good
The power good pin (PG) indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition, PG is held low. By default, PG is asserted high after the output has ramped to a voltage above 90% of the nominal voltage, and deasserted if the output voltage falls below 85% of the nominal voltage. These thresholds may be changed using the PMBus commands POWER_GOOD_ON and VOUT_UV_FAULT_LIMIT.

The time between when the POWER_GOOD_ON threshold is reached and when the PG pin is actually asserted is set by the PMBus command POWER_GOOD_DELAY. See Electrical Specification for default value and range.

By default the PG pin is configured as an open drain output but it is also possible to set the output in push-pull mode by the command USER_CONFIG. The PG output is not defined during ramp up of the input voltage due to the initialization of the product.

Over Current Protection (OCP)
The product includes robust current limiting circuitry for protection at continuous overload. After ramp-up is complete the product can detect an output overload/short condition. The following OCP response options are available:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response from an over current fault is option 2. Note that delayed shutdown is not supported. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_OC_FAULT_LIMIT and MFR_IOUT_OC_FAULT_RESPONSE.

Under Current Protection (UCP)
The product includes robust current limiting circuitry for protection at continuous reversed current, due to a synchronous rectifier ability to sink current. Refer to section Over Current Protection for response configuration options and default setting. The UCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_UC_FAULT_LIMIT and MFR_IOUT_UC_FAULT_RESPONSE.

Switching Frequency

The default switching frequency is chosen as the best tradeoff between efficiency and thermal performance, output ripple and load transient performance. The switching frequency can be reconfigured in a certain range using the PMBus command FREQUENCY_SWITCH. Refer to Electrical Specification for default switching frequency and range. Changing the switching frequency will affect efficiency and power dissipation, load transient response (control loop characteristics) and output ripple.

Note that since the product has two phases the effective switching frequency will be twice the configured value.

Synchronization

Two or more products may be synchronized with an external clock to eliminate beat frequencies reflected back to the input supply rail. Eliminating the slow beat frequencies (usually <10 kHz) eases the filtering requirements. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC output, working as a source of synchronization signal for other products connected to the same synchronization line. The SYNC pin of products being synchronized must be configured as SYNC Input. Default configuration is using the internal clock, independently of signal at the SYNC pin. Synchronization is configured using PMBus command MFR_USER_CONFIG.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized using the SYNC pin.

The phase offset is measured from the rising edge of the applied external clock to the rising edge of the PWM pulse as illustrated below.

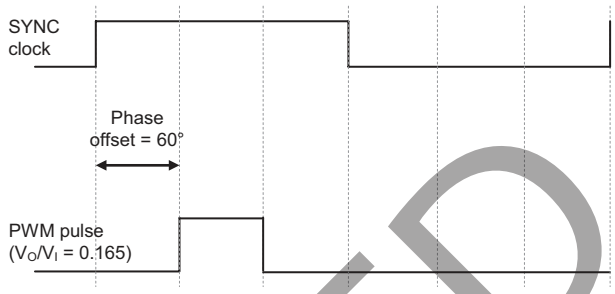


Illustration of phase offset.

The phase offset is configured using the PMBus command INTERLEAVE and is defined as:

$$Phase\_offset(°) = 360° \times \frac{Interleave\_order}{Number\_in\_group}$$

Interleave_order is in the range 0-15. *Number_in_group* is in the range 0-15 where a value of 0 means 16. The set resolution for the phase offset is 360° / 16 = 22.5°.
By default *Number_in_group* = 0 and *Interleave_order* = Four LSB's of set PMBus address (see section PMBus Addressing).

Soft-start and Soft-stop

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.
The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The off delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

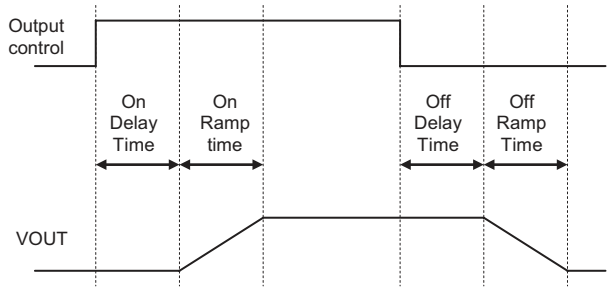


Illustration of Soft-Start and Soft-Stop.

By default soft-stop is disabled and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another.

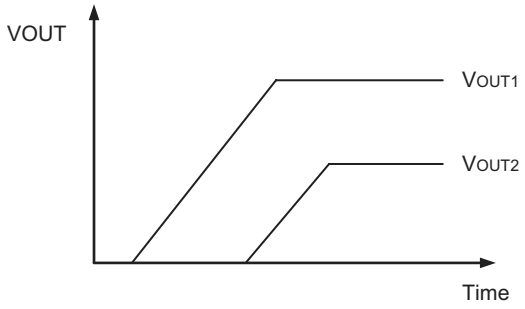


Illustration of Output Voltage Sequencing.

Different types of multi-product sequencing are supported:

1. Time based sequencing. Configuring the start delay and rise time of each module through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.
2. Event based sequencing. Routing the PG pin signal of one module to the CTRL pin of the next module in the sequence.
3. DDC based sequencing. Power Good triggered sequencing with the same flexibility as time based sequencing. Configured through the PMBus interface and uses the DDC bus, see section Digital-DC bus.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.

The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

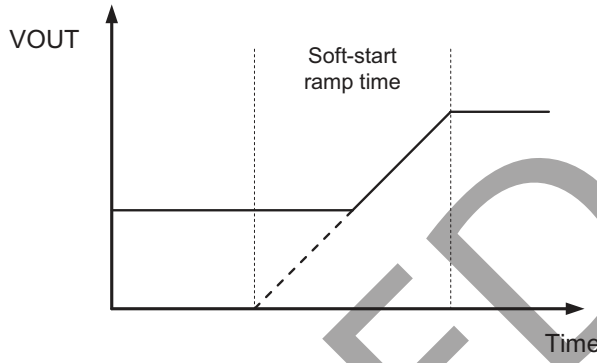


Illustration of Pre-Bias Startup.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

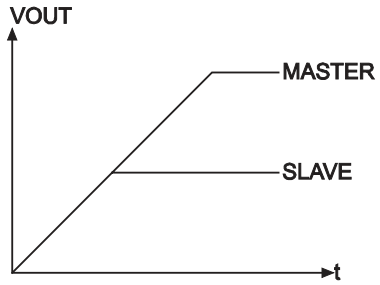


Illustration of Coincident Voltage Tracking.

2. Ratiometric. This mode configures the product to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but a different tracking ratio may be set by an external resistive voltage divider.

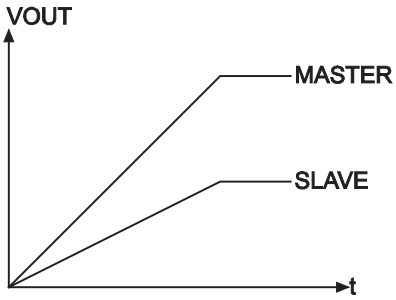


Illustration of Ratiometric Voltage Tracking.

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. Any device configured in tracking mode will ignore its soft-start/stop settings and take on the turn-on/turn-off characteristics of the voltage present at the VTRK pin.
All of the CTRL pins in the tracking group must be connected and driven by a single logic source. Tracking is configured using the PMBus command TRACK_CONFIG.

Digital-DC Bus
The Digital-DC Bus, DDC, is used to communicate between products. This dedicated single wire bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The DDC solves the PMBus data rate limitation. The DDC pin on all devices in an application should be connected together. A pullup resistor is required on the common DDC in order to guarantee the rise time as follows:

$T = R_{DDC}C_{DDC} \leq 1\mu s$

Where R_{DDC} is the pull up resistor value and C_{DDC} is the bus loading. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up.
The DDC is an internal bus, such that it is only connected across the modules and not the PMBus system host. DDC addresses are assigned on a rail level, i.e. modules within the same current sharing group share the same DDC address. Addressing rails across the DDC is done with a 5 bit DDC ID, yielding a theoretical total of 32 rails that can be shared with a single DDC bus.
By default the DDC ID is set to the five LSB's of set PMBus address (see section PMBus Addressing).

Parallel Operation (Current Sharing)
Paralleling multiple products can be used to increase the output current capability of a single power rail. By connecting the DDC and SYNC pins of each device and configuring the devices as a current sharing rail, the units will share the current equally, enabling up to 100% utilization of the current capability for each device in the current sharing rail. The product uses a low bandwidth, first-order digital current sharing by aligning the output voltage of the slave devices to deliver the same current as the master device. Artificial droop resistance is added to the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PWB layout. Up to 4 devices can be configured in a given current sharing group.

Broadcast Control
The product can be configured to broadcast output voltage enable or setting of output voltage level over the DDC bus to other devices in the group. If configured to do so, a device receiving a PMBus OPERATION command or VOUT_COMMAND command will broadcast the same command over the DDC bus, and other devices on the DDC bus will respond to the same commands. Broadcast control is configured using the PMBus command DDC_GROUP.

Fault Spreading
The product can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a nondestructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so. Fault spreading is configured using the PMBus command DDC_GROUP and LEGACY_FAULT_GROUP.

THERMAL CONSIDERATION

General

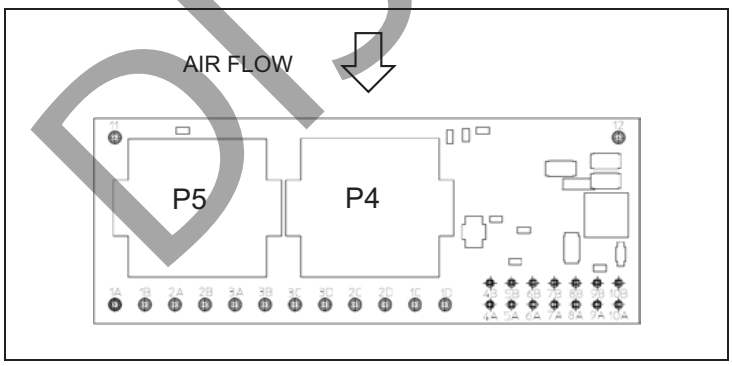
The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified V_I. The product is tested on a 254 x 254 mm, 35 µm (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 16 layers.

Definition of Product Operating Temperature

The temperature at positions P1, P2, P3, P4 and P5 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal designs and topologies. Temperatures above specified maximum measured at the specified positions are not allowed and may cause permanent damage.
Note that the max values are the absolute maximum rating (non destruction) and that the provided Electrical Specification data is guaranteed up to TP1 = +95°C.

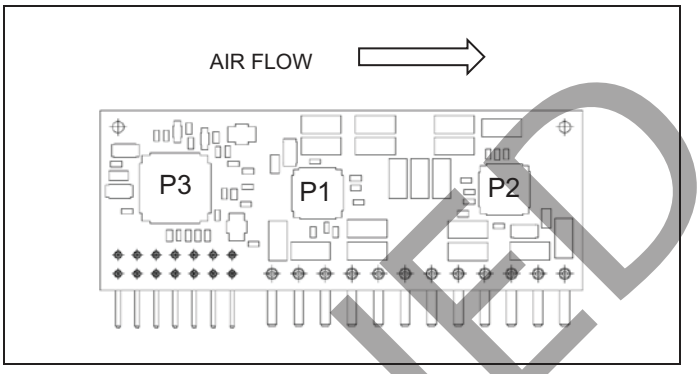
Position	Description	Max. Temperature
P1	power switch	130°C
P2	power switch	130°C
P3	VR controller	125°C
P4	power inductor	125°C
P5	power inductor	125°C

NDM3Z-90HT



Temperature positions and air flow direction (top view).

NDM3Z-90V



Temperature positions and air flow direction.

Note that the same PCB is used for both the NDM3Z-90HT and the NDM3Z-90V. Thus, the positions indicated in the pictures apply to both versions.

Definition of Reference Temperature T_{P1}

The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Over Temperature Protection (OTP)

The products are protected from thermal overload by dual internal over temperature shutdown functions:

1. Temperature in VR controller, located in position P3.
2. The highest temperature of power switches, located in positions P1 and P2.

These temperatures are continously monitored and when a temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the temperature is above the warning threshold. Operation resumes automatically and the output is enabled when the temperature has fallen below the warning threshold, i.e. there is a hysteresis defined by the difference between the fault threshold and the warning threshold.

Default response is option 2. The default OTP thresholds and hysteresis are specified in Electrical Characteristics. The OTP limit, hysteresis and response for temperature in position P3 is configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and

OT_FAULT_RESPONSE. The OTP limit, hysteresis and response for highest temperature of positions P1 and P2 are configured using the PMBus commands MFR_VMON_OV_FAULT_LIMIT and VMON_OV_FAULT_RESPONSE.

PCB Layout Considerations

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

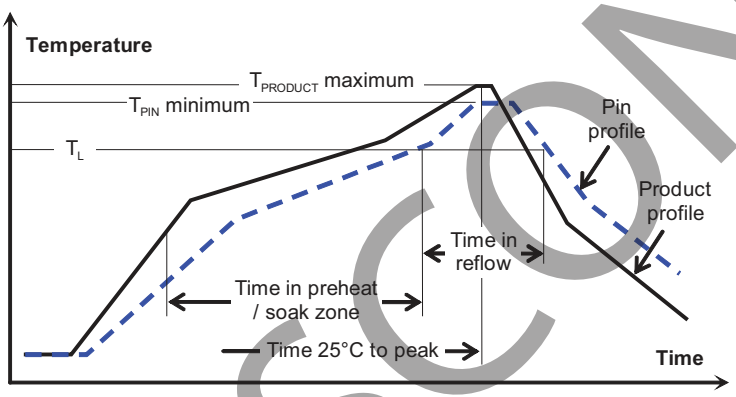
Further layout recommendations are listed below.

- The pin strap resistors, RSET, and RSA should be placed as close to the product as possible to minimize loops that may pick up noise.
- Avoid current carrying planes under the pin strap resistors and the PMBus signals.
- The capacitors CIN should be placed as close to the input pins as possible.
- The capacitors COUT should be placed close to the load.
- The point of output voltage sense should be "down stream" of COUT.
- Care should be taken in the routing of the connections from the sensed output voltage to the +S and –S terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields.
- If possible use planes on several layers to carry VIN, VOUT and GND. There should be a large number of vias close to the VIN, VOUT and GND pads in order to lower input and output impedances and improve heat spreading between the product and the host board.

SOLDERING INFORMATION - Surface Mounting and Through-Hole Mount Pin in Paste Assembly

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes. The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.
A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long term reliability and isolation voltage.

General reflow process specifications	SnPb eutectic	Pb-free
average ramp up ($T_{PRODUCT}$)	3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature (T_L)	183°C	221°C
Minimum reflow time above T_L	60s	60s
Minimum pin temperature (T_{PIN})	210°C	235°C
Peak product temperature ($T_{PRODUCT}$)	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)	6°C/s max	6°C/s max
Maximum time 25°C to peak	6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 3C is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 220°C is recommended to ensure a reliable solder joint. For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PWB near pin 10A is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

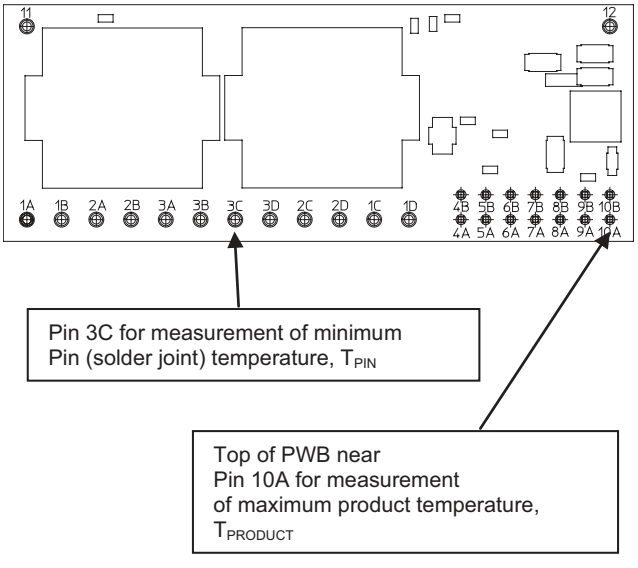
SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C. During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices). Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocoupler Attachment



SOLDERING INFORMATION - Hole Mounting

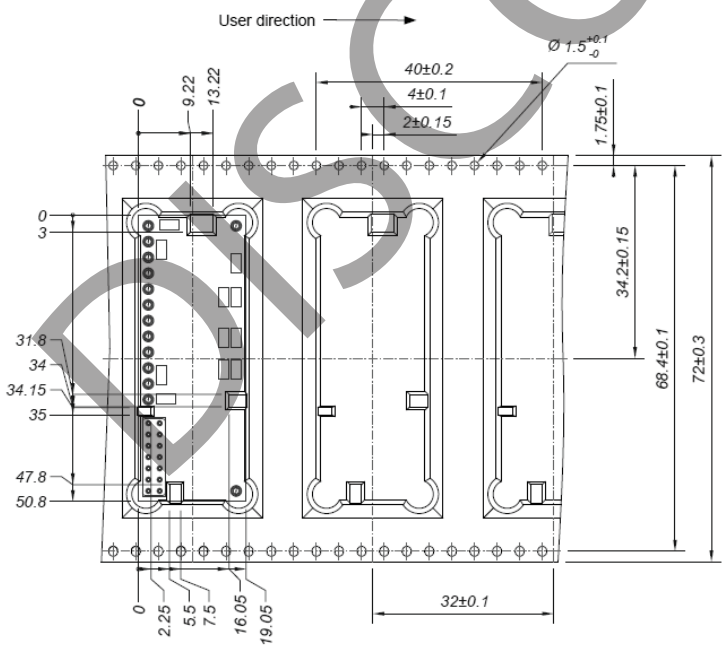
The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds. A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

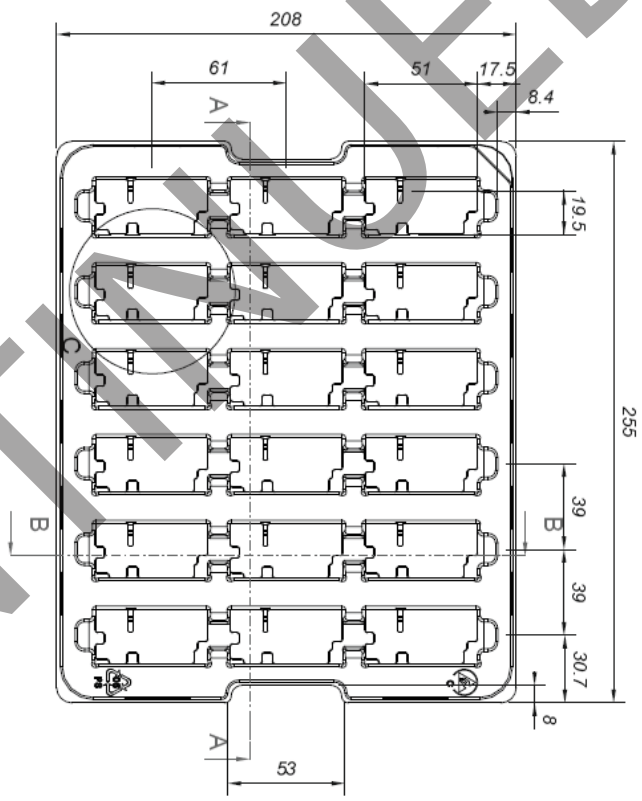
Delivery Package Information

The products are delivered in antistatic trays and in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
material	antistatic PS
surface resistance	10^5 < Ohm/square < 10^{10}
bakeability	the tape is not bakeable
tape width, W	72 mm [2.83 inch]
pocket pitch, P_1	32 mm [1.26 inch]
pocket depth, K_0	14.6 mm [0.575 inch]
reel diameter	330 mm [13 inch]
reel capacity	130 products/reel
reel weight	TBD



Tray Specifications	
material	antistatic PS
surface resistance	10^1 < Ohm/square < 10^6
bakeability	the trays are not bakeable
tray thickness	18 mm [0.724 inch]
box capacity	90 products (5 full trays/box)
tray weight	TBD



PRODUCT QUALIFICATION SPECIFICATIONS

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature TA Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity[1]	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat[2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td 1 IEC 60068-2-20 test Ta 2	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g2/Hz 10 min in each direction

Notes: 1. Only for products intended for reflow soldering (surface mount products).
2. Only for products intended for wave soldering (plated through hole products)

General Information

The calculations for CUI module failure rate (λ) and mean time between failures (MTBF) are calculated at maximum output power and operating ambient temperature (TA) of + 40ºC. The Telcordia SR-332 Issue 2 Method 1 (parts count method) is used to calculate the mean steady-state failure rate and standard deviation (σ). The MTBF is defined as 1/ λ.

For the NDM3Z-90:

λ	36 nFailures/h
σ	7 nFailures/h
MTBF	27 Mh
MTBF at 90% confidence level	22 Mh

Compatibility with RoHS Requirements

CUI NDM modules are compatible with the relevant clauses and requirements of RoHS directive 2011/65/EU. They have a maximum concentration of 0.01% by weight of cadmium and 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE.

The Statement of Compliance document notes exemptions to the RoHS directive present in CUI Novum modules. CUI Novum modules meet and will continue to meet the obligations under regulation (EC) No 1907/2006 addressing the registration, evaluation, authorization and restriction of chemicals (REACH) as they become applicable. CUI will utilize the product materials declarations to communicate information on substances in the products.

Quality Statement

High quality of CUI products are achieved through conservative design rules, numerous design reviews and product qualifications. Products are designed and manufactured with a philosophy where quality systems and methods such as ISO 9000, Six Sigma and SPC are employed to ensure continuous improvements. Modules with early failures are screened out and parts are subjected to ATE-based final testing.

Safety

CUI NDM modules are designed in accordance with safety standards IEC/EN/UL 60950-1 Safety of Information Technology Equipment.

On-board DC/DC converters and DC/DC regulators are defined as component power supplies and thus cannot fully comply with the provisions of any safety requirements without "conditions of acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information and Safety Certificate for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

CUI NDM modules are certified in accordance with EN 60950-1 and UL 60950-1 recognized. All parts of the CUI NDM modules meet the flammability rating requirements for V-0 class material according to IEC 60695-11-10, Fire hazard testing, test flames – 50 W horizontal and vertical flame test methods.

A slow blow fuse is recommended to be placed at the input of each DC/DC converter. The fuse should be placed in front of the input filter if such a filter is used. The fuse will provide the following functions in the rare event of a component problem that imposes a short circuit on the input source:

- Isolate the fault from the input power source so as to isolate the fault from the other parts of the system
- Protect the distribution wiring from excessive current thus preventing hazardous overheating

The DC/DC regulator output is SELV if the input source meets the requirements for SELV circuits according to IEC/EN/UL 60950-1.

REVISION HISTORY

rev.	date
1.02	09/03/2015
1.03	12/21/2015
1.04	09/21/2016

The revision history provided is for informational purposes only and is believed to be accurate.

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