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NTE74HC125 & NTE74HC126
Integrated Circuit
TTL – High Speed CMOS,
Quad Bus Buffer with 3–State Outputs

Description:

The NTE74HC125 and NTE74HC126 are high speed CMOS quad bus buffers in a 14–Lead plastic DIP type package fabricated in silicon gate C^2MOS technology. The have the same high speed performance of LS–TTL combined with true CMOS low power consumption.

These devices require the same 3–State control input G to be taken high to make the output go into the high impedance state.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- High Speed: t_{PD} = 8ns (typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (max) at +25°C
- Output Drive Capability: 15 LS–TTL Loads
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Symmetrical Output Impedance: $I_{OL} = |I_{OH}|$ = 6mA (min)
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Wide Operating Voltage range: V_{CC}(opr) = 2V to 6V

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Voltage, V_I, V_O . . . . . –0.5 to V_{CC} +0.5
DC Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Source Sink Current (Per Pin), I_O . . . . . ±35mA
DC V_{CC} or GND Current, I_{CC} or I_{GND} . . . . . ±70mA
Power Dissipation (Note 2), P_D 500mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note 2. 500mW: ≅ +65°C derate to 300mW by 10mW/°C: +65° to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
High Level Input Voltage	V_{IH}		2.0	1.5	–	–	1.5	–	1.5	–	V
			4.5	3.15	–	–	3.15	–	3.15	–	V
			6.0	4.2	–	–	4.2	–	4.2	–	V
Low Level Input Voltage	V_{IH}		2.0	–	–	0.5	–	0.5	–	0.5	V
			4.5	–	–	1.35	–	1.35	–	1.35	V
			6.0	–	–	1.8	–	1.8	–	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IN} = V_{IH} or V_{IL}, I_O = –20μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			4.5	4.4	4.5	–	4.4	–	4.4	–	V
			6.0	5.9	6.0	–	5.9	–	5.9	–	V
TTL Loads		V_I = V_{IH} or V_{IL}, I_O = –6mA	4.5	4.18	4.31	–	4.13	–	4.10	–	V
		V_I = V_{IH} or V_{IL}, I_O = –7.8mA	6.0	5.68	5.80	–	5.63	–	5.60	–	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IN} = V_{IH} or V_{IL}, I_O = 20μA	2.0	–	0.0	0.1	–	0.1	–	0.1	V
			4.5	–	0.0	0.1	–	0.1	–	0.1	V
			6.0	–	0.0	0.1	–	0.1	–	0.1	V
TTL Loads		V_{IN} = V_{IH} or V_{IL}, I_O = 6mA	4.5	–	0.17	0.26	–	0.33	–	0.4	V
		V_{IN} = V_{IH} or V_{IL}, I_O = –7.8mA	6.0	–	0.18	0.26	–	0.33	–	0.4	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	μA
3–State Output Off–State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_O = V_{CC} or GND	6.0	–	–	±0.5	–	±5.0	–	±10	μA
Quiescent Device Current	I_{CC}	V_{IN} = V_{CC} or GND, I_O = 0mA	6.0	–	–	4.0	–	40	–	80	μA

AC Electrical Characteristics: (t_r = t_f = 6ns)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	20	60	–	75	–	90	ns
			4.5	–	6	12	–	15	–	18	ns
			6.0	–	5	10	–	13	–	15	ns

AC Electrical Characteristics (Cont'd): ($t_r = t_f = 6ns$)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay Time	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	36	75	–	95	–	110	ns
			4.5	–	9	15	–	19	–	22	ns
			6.0	–	8	13	–	16	–	19	ns
		C_L = 150pF	2.0	–	52	105	–	130	–	160	ns
			4.5	–	13	21	–	26	–	32	ns
			6.0	–	11	18	–	22	–	27	ns
3−State Output Enable Time	t_{PZL}, t_{PZH}	C_L = 50pF, R_L = 1KΩ	2.0	–	36	75	–	95	–	110	ns
			4.5	–	9	15	–	19	–	22	ns
			6.0	–	8	13	–	16	–	19	ns
		C_L = 150pF, R_L = 1KΩ	2.0	–	52	105	–	130	–	160	ns
			4.5	–	13	21	–	26	–	32	ns
			6.0	–	11	18	–	22	–	27	ns
3−State Output Disable Time	t_{PLZ}, t_{PHZ}	C_L = 50pF, R_L = 1KΩ	2.0	–	48	80	–	100	–	120	ns
			4.5	–	12	16	–	20	–	24	ns
			6.0	–	10	14	–	17	–	20	ns
Input Capacitance	C_{IN}		–	–	5	10	–	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	Note 3	–	–	35	–	–	–	–	–	pF

Note 3. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation: $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$.

Truth Tables:

NTE74HC125

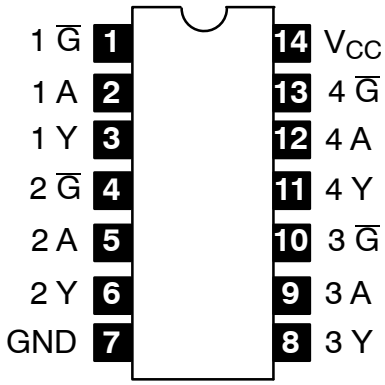
A	$\overline{G}$	Y
X	H	Z
L	L	L
H	L	H

NTE74HC126

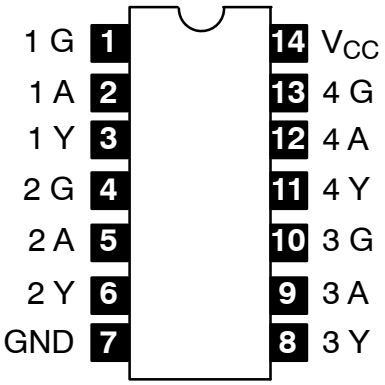
A	G	Y
X	L	Z
L	H	L
H	H	H

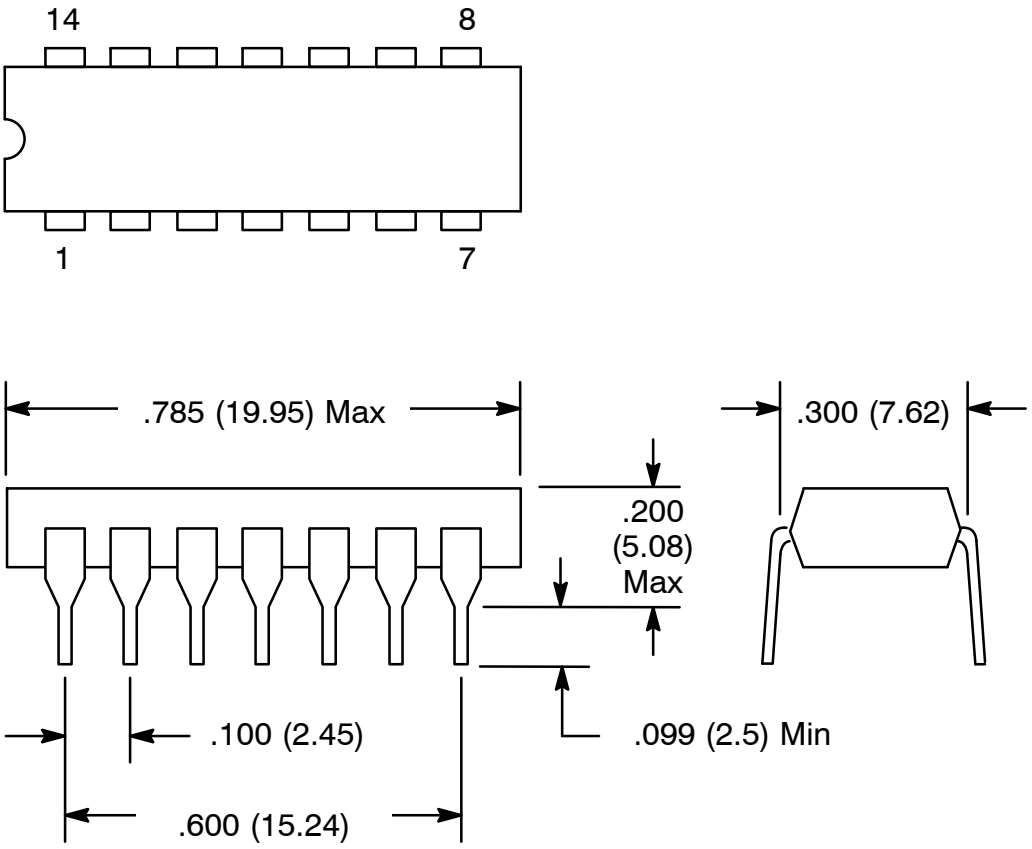
Pin Connection Diagram

NTE74HC125



NTE74HC126




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)